Current Feedback Amplifier Theory and Applications

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Introduction

Current feedback amplifiers (CFA) have sacrificed the DC precision of voltage feedback amplifiers (VFA) in a trade-off for increased slew rate and a bandwidth that is relatively independent of the closed loop gain. Although CFAs do not have the DC precision of their VFA counterparts, they are good enough to be DC coupled in video applications without sacrificing too much dynamic range. The days when high frequency amplifiers had to be AC coupled are gone forever, because some CFAs are approaching the GHz gain bandwidth region. The slew rate of CFAs is not limited by the linear rate of rise that is seen in VFAs, so it is much faster and leads to faster rise/fall times and less intermodulation distortion.

The general feedback theory used in this paper is developed in Intersil Application Note Number AN9415 entitled “Feedback, Op Amps and Compensation.” The approach to the development of the circuit equations is the same as in the referenced application note, and the symbology/terminology is the same with one exception. The impedance connected from the negative op amp input to ground, or to the source driving the negative input, will be called Z_G rather than Z_1 or Z_I, because this has become the accepted terminology in CFA papers.

Development of the General Feedback Equation

Referring to the block diagram shown in Figure 1, Equation 1, Equation 2 and Equation 3 can be written by inspection if it is assumed that there are no loading concerns between the blocks. This assumption is implicit in all block diagram calculations, and requires that the output impedance of a block be much less than input impedance of the block it is driving. This is usually true by one or two orders of magnitude. Algebraic manipulation of Equation 1, Equation 2 and Equation 3 yields Equation 4 and Equation 5 which are the defining equations for a feedback system.

$$V_O = EA \quad \text{(EQ. 1)}$$

$$E = V_I - \beta V_O \quad \text{(EQ. 2)}$$

$$E = V_O/A \quad \text{(EQ. 3)}$$

$$V_O/V_I = A/(1 + A\beta) \quad \text{(EQ. 4)}$$

$$E/V_I = 1/(1 + A\beta) \quad \text{(EQ. 5)}$$

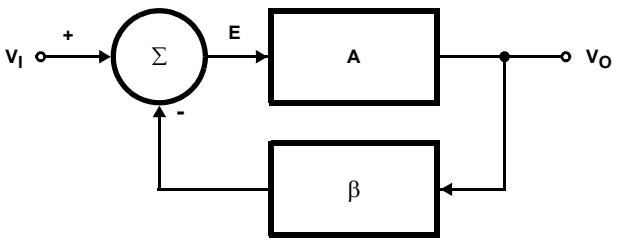

FIGURE 1. FEEDBACK SYSTEM BLOCK DIAGRAM

In this analysis the parameter A, which usually includes the amplifier and thus contains active elements, is called the direct gain. The parameter β, which normally contains only passive components, is called the feedback factor. Notice that in Equation 4 as the value of A approaches infinity the quantity Aβ, which is called the loop gain, becomes much larger than one; thus, Equation 4 can be approximated by Equation 6.

$$V_O/V_I = 1/\beta \quad \text{for } A\beta >> 1 \quad \text{(EQ. 6)}$$

V_O/V_I is called the closed loop gain. Because the direct gain, or amplifier response, is not included in Equation 6, the closed loop gain (for A >> 1) is independent of amplifier parameter changes. This is the major benefit of feedback circuits.

Equation 4 is adequate to describe the stability of any feedback circuit because these circuits can be reduced to this generic form through block diagram reduction techniques [1]. The stability of the feedback circuit is determined by setting the denominator of Equation 4 equal to zero.

$$1 + A\beta = 0 \quad \text{(EQ. 7)}$$

$$A\beta = -1 = |1| \angle -180 \quad \text{(EQ. 8)}$$

Observe from Equation 4 and Equation 8, that if the magnitude of the loop gain can achieve a magnitude of one while the phase shift equals -180 degrees, the closed loop gain becomes undefined because of division by zero. The undefined state is unstable, causing the circuit to oscillate at the frequency where the phase shift equals -180 degrees. If the loop gain at the frequency of oscillation is slightly greater than one, it will be reduced to one by the reduction in gain suffered by the active elements as they approach the limits of saturation. If the value of Aβ is much greater than one, gross nonlinearities can occur and the circuit may cycle between saturation limits. Preventing instability is the essence of feedback circuit design, so this topic will be touched lightly here and covered in detail later in this application note.

A good starting point for discussing stability is finding an easy method to calculate it. Figure 2 shows that the loop gain can be calculated from a block diagram by opening current inputs, shorting voltage inputs, breaking the circuit and calculating the response (V_{TO}) to a test input signal (V_{TI}).

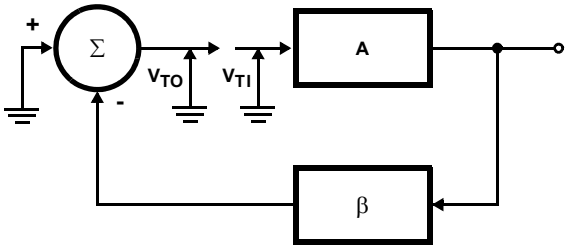

FIGURE 2. BLOCK DIAGRAM FOR COMPUTING THE LOOP GAIN

$V_{TO}/V_{TI} = A\beta$ (EQ. 9)

Current Feedback Stability Equation Development

The CFA model is shown in Figure 3. The non-inverting input connects to the input of a buffer, so it is a very high impedance on the order of a bipolar transistor VFA's input impedance. The inverting input ties to the buffer output; Z_B models the buffer output impedance, which is usually very small, often less than 50Ω. The buffer gain, G_B, is nearly but always less than one because modern integrated circuit design methods and capabilities make it easy to achieve. G_B is overshadowed in the transfer function by the transimpedance, Z, so it will be neglected in this analysis.

The output buffer must present a low impedance to the load. Its gain, G_{OUT}, is one, and is neglected for the same reason as the input buffer's gain is neglected. The output buffer's impedance, Z_{OUT}, affects the response when there is some output capacitance; otherwise, it can be neglected unless DC precision is required when driving low impedance loads.

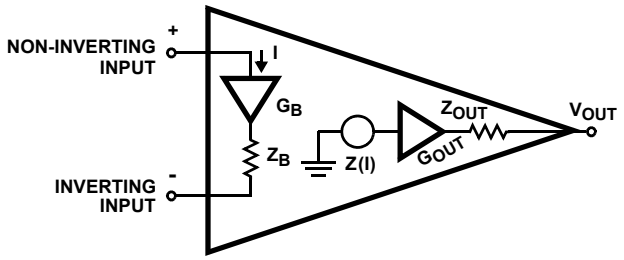

FIGURE 3. CURRENT FEEDBACK AMPLIFIER MODEL

Figure 4 is used to develop the stability equation for the inverting and non-inverting circuits. Remember, stability is a function of the loop gain, Aβ, and does not depend on the placement of the amplifier's inputs or outputs.

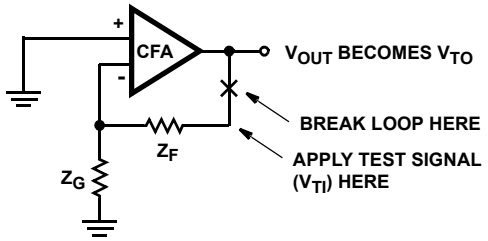

FIGURE 4. BLOCK DIAGRAM FOR STABILITY ANALYSIS

Breaking the loop at point X, inserting a test signal, V_{TI}, and calculating the output signal, V_{TO}, yields the stability equation. The circuit is redrawn in Figure 5 to make the calculation more obvious. Notice that the output buffer and its impedance have been eliminated because they are insignificant in the stability calculation. Although the input buffer is shown in the diagram, it will be neglected in the stability analysis for the previously mentioned reasons.

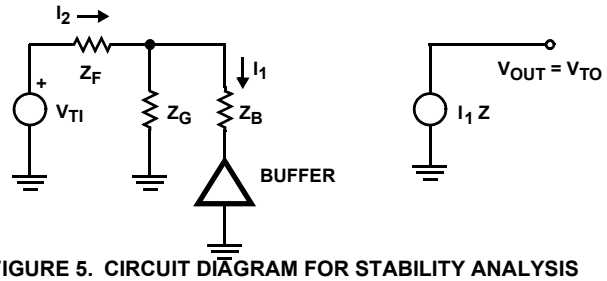

FIGURE 5. CIRCUIT DIAGRAM FOR STABILITY ANALYSIS

The current loop equations for the input loop and the output loop are given below along with the equation relating I_1 to I_2.

$V_{TI} = I_2(Z_F + Z_G||Z_B)$ (EQ. 10)

$V_{TO} = I_1 Z$ (EQ. 11)

$I_2(Z_G||Z_B) = I_1 Z_B$; For $G_B = 1$ (EQ. 12)

Equation 10 and Equation 12 are combined to obtain Equation 13.

$$V_{TI} = I_1(Z_F + Z_G||Z_B)(1 + Z_B/Z_G) = I_1 Z_F \ (1+Z_B/Z_F||Z_G) \quad \text{(EQ. 13)}$$

Dividing Equation 11 by Equation 13 yields Equation 14 which is the defining equation for stability. Equation 14 will be examined in detail later, but first the circuit equations for the inverting and non-inverting circuits must be developed so that all of the equations can be examined at once.

$$A\beta = V_{TO}/V_{TI} = Z/(Z_F(1 + Z_B/Z_F||\ Z_G)) \quad \text{(EQ. 14)}$$

Developing the Non-Inverting Circuit Equation and Model

Equation 15 is the current equation at the inverting input of the circuit shown in Figure 6. Equation 16 is the loop equation for the input circuit, and Equation 17 is the output circuit equation. Combining these equations yields Equation 18, in the form of Equation 4, which is the non-inverting circuit equation.

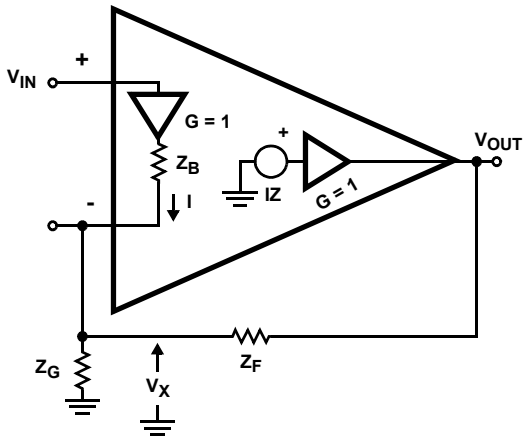

FIGURE 6. NON-INVERTING CIRCUIT DIAGRAM

$I = (V_X/Z_G) - (V_{OUT} - V_X)/Z_F$ (EQ. 15)

$V_X = V_{IN} - IZ_B$ (EQ. 16)

$V_{OUT} = IZ$ (EQ. 17)

(EQ. 18)

$$\frac{V_{OUT}}{V_{IN}} = \frac{\dfrac{Z(1+Z_F/Z_G)}{Z_F(1+Z_B/Z_F \| Z_G)}}{1+\dfrac{Z}{Z_F(1+Z_B/Z_F \| Z_G)}}$$

The block diagram equivalent for the non-inverting circuit is shown in Figure 7.

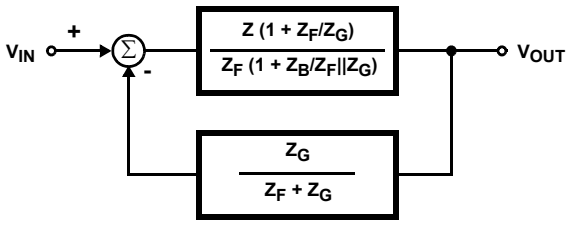

FIGURE 7. BLOCK DIAGRAM OF THE NON-INVERTING CFA

Developing the Inverting Circuit Equation and Model

Equation 19 is the current equation at the inverting input of the circuit shown in Figure 8. Equation 20 defines the dummy variable V_X, and Equation 21 is the output circuit equation. Equation 22 is developed by substituting Equation 20 and Equation 21 into Equation 19, simplifying the result, and manipulating it into the form of Equation 4.

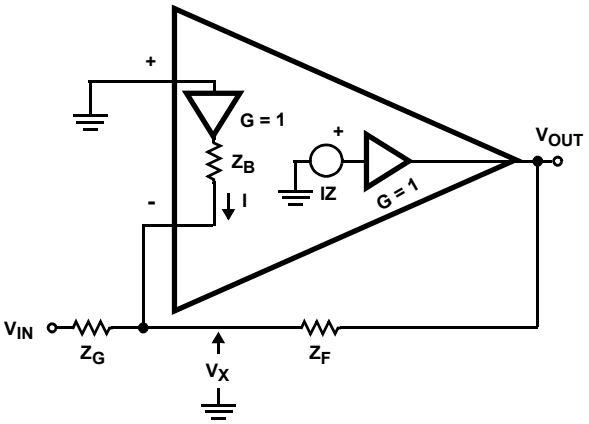

FIGURE 8. INVERTING CIRCUIT DIAGRAM

$$\frac{V_{IN}-V_X}{Z_G} + I = \frac{V_X - V_{OUT}}{Z_F} \quad \text{(EQ. 19)}$$

$$IZ_B = -V_X \quad \text{(EQ. 20)}$$

$$IZ = V_{OUT} \quad \text{(EQ. 21)}$$

$$\frac{V_{OUT}}{V_{IN}} = -\frac{\dfrac{Z}{Z_G(1+Z_B/Z_F \| Z_G)}}{1+\dfrac{Z}{Z_F(1+Z_B/Z_F \| Z_G)}} \quad \text{(EQ. 22)}$$

The block diagram equivalent for the inverting circuit is given in Figure 9.

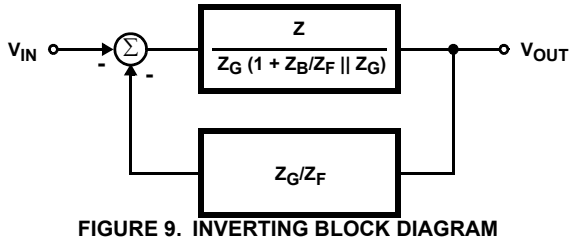

FIGURE 9. INVERTING BLOCK DIAGRAM

Stability

Equation 8 states the criteria for stability, but there are several methods for evaluating this criteria. The method that will be used in this paper is called the Bode plot [2] which is a log plot of the stability equation. A brief explanation of the Bode plot procedure is given in “Feedback, Op Amps and Compensation” [3]. The magnitude and phase of the open loop transfer function are both plotted on logarithmic scales, and if the gain decreases below zero dB before the phase shift reaches 180 degrees the circuit is stable. In practice the phase shift should be ≤140 degrees, i.e., greater than 40 degrees phase margin, to obtain a well behaved circuit. A sample Bode plot of a single pole circuit is given in Figure 10.

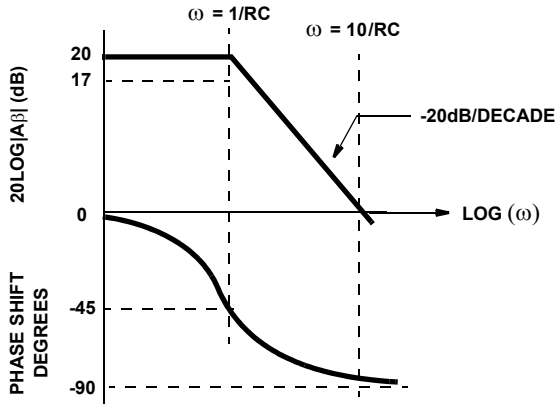

FIGURE 10. SAMPLE BODE PLOT

Referring to Figure 10, notice that the DC gain is 20dB, thus the circuit gain must be equal to 10. The amplitude is down 3dB at the break point, $\omega = 1/RC$, and the phase shift is -45 degrees at this point. The circuit can not become unstable with only a single pole response because the maximum phase shift of the response is -90 degrees.

CFA circuits often oscillate, intentionally or not, so there are at least two poles in their loop gain transfer function. Actually, there are multiple poles in the loop gain transfer function, but the CFA circuits are represented by two poles for two reasons: a two pole approximation gives satisfactory correlation with laboratory results, and the two pole mathematics are well known and easy to understand. Equation 14, the stability equation for the CFA, is given in logarithmic form as Equation 23 and Equation 24.

$$20\text{LOG}|A\beta| = 20\text{LOG}|Z/(Z_F(1+Z_B/Z_F||Z_G))| \quad \text{(EQ. 23)}$$

$$\phi = \text{TANGENT}^{-1}(Z/(Z_F(1+Z_B/Z_F||Z_G))) \quad \text{(EQ. 24)}$$

The answer to the stability question is found by plotting these functions on log paper. The stability equation, 20log|Aβ|, has the form 20logx/y which can be written as 20logx/y = 20logx - 20logy. The numerator and denominator of Equation 23 will be operated on separately, plotted independently and then added graphically for analysis. Using this procedure the independent variables can be manipulated separately to show their individual effects. Figure 11 is the plot of Equation 23 and Equation 24 for a typical CFA where $Z = 1M\Omega/(\tau_1 s + 1)(\tau_2 s + 1)$, $Z_F = Z_G = 1k\Omega$, and $Z_B = 70\Omega$.

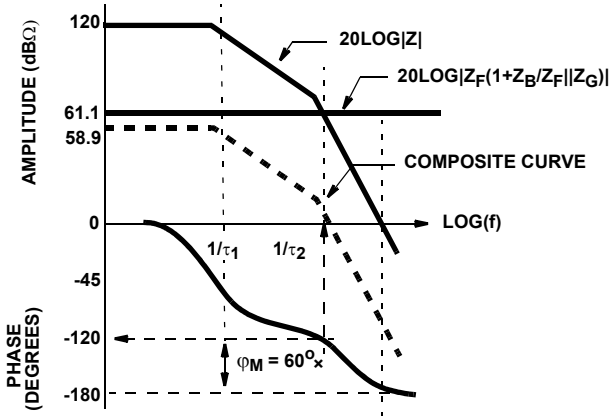

FIGURE 11. CFA TRANSIMPEDANCE PLOT

If $20\log|Z_F(1+Z_B/Z_F||Z_G)|$ were equal to 0dB the circuit would oscillate because the phase shift of Z reaches -180 degrees before 20log|Z| decreases below zero. Since $20\log|Z_F(1 + Z_B/Z_F||Z_G)| = 61.1dB\Omega$, the composite curve moves down by that amount to 58.9dBΩ where it is stable because it has 120 degrees phase shift or 60 degrees phase margin. If $Z_B = 0\Omega$ and $Z_F = R_F$, then $A\beta = Z/R_F$. In this special case, stability is dependent on the transfer function of Z and R_F, and R_F can always be specified to guarantee stability. The first conclusion drawn here is that $Z_F(1+Z_B/Z_F||Z_G)$ has an impact on stability, and that the feedback resistor is the dominant part of that quantity so it has the dominant impact on stability. The dominant selection criteria for R_F is to obtain the widest bandwidth with an accepted amount of peaking; 60 degrees phase margin is equivalent to approximately 10% or, 0.83dB, overshoot. The second conclusion is that the input buffer's output impedance, Z_B, will have a minor effect on stability because it is small compared to the feedback resistor, even though it is multiplied by $1/Z_F||Z_G$ which is related to the closed loop gain. Rewriting Equation 14 as $A\beta = Z/(Z_F+Z_B(1+R_F/R_G))$ leads to the third conclusion which is that the closed loop gain has a minor effect on stability and bandwidth because it is multiplied by Z_B which is a small quantity relative to Z_F. It is because of the third conclusion that many people claim closed loop gain versus bandwidth independence for the CFA, but that claim is dependent on the value of Z_B relative to Z_F.

CFAs are usually characterized at a closed loop gain (G_{CL}) of one. If the closed loop gain is increased then the circuit becomes more stable, and there is the possibility of gaining some bandwidth by decreasing Z_F. Assume that $A\beta_1 = A\beta_N$ where $A\beta_1$ is the loop gain at a closed loop gain of one and $A\beta_N$ is the loop gain at a closed loop gain of N; this insures that stability stays constant. Through algebraic manipulation, Equation 14 can be rewritten in the form of Equation 25 and solved to yield Equation 27 and a new Z_{FN} value.

$$\frac{Z}{Z_{F1} + Z_B(1 + Z_{F1}/Z_{G1})} = \frac{Z}{Z_{FN} + Z_B(1 + Z_{FN}/Z_{GN})} \quad \text{(EQ. 25)}$$

$$\frac{Z}{Z_{F1} + Z_B G_{CL1}} = \frac{Z}{Z_{FN} + Z_B G_{CLN}} \quad \text{(EQ. 26)}$$

$$Z_{FN} = Z_{F1} + Z_B(G_{CL1} - G_{CLN}) \quad \text{(EQ. 27)}$$

For the HA5020 at a closed loop gain of 1, if $Z = 6M\Omega$, $Z_{F1} = 1k\Omega$, and $Z_B = 75\Omega$, then $Z_{F2} = 925\Omega$. Experimentation has shown, however, that $Z_{F2} = 681\Omega$ yields better results. The difference in the predicted versus the measured results is that Z_B is a frequency dependent term which adds a zero in the loop gain transfer function that has a much larger effect on stability. The equation for Z_B[5] is given below.

$$Z_B = h_{IB} + \frac{R_B}{\beta_0 + 1}\left(\frac{1 + S\beta_0/\omega_T}{1 + S\beta_0/(\beta_0 + 1)\omega_T}\right) \quad \text{(EQ. 28)}$$

At low frequencies $h_{IB} = 50\Omega$ and $R_B/(\beta_o+1) = 25\Omega$ which corresponds to $Z_B = 75\Omega$, but at higher frequencies Z_B will vary according to Equation 28. This calculation is further complicated because β_0 and ω_T are different for NPN and PNP transistors, so Z_B also is a function of the polarity of the output. Refer to Figure 12 and Figure 13 for plots of the transimpedance (Z) and Z_B for the HA5020 [5]. Notice that Z starts to level off at 20MHz which indicates that there is a zero in the transfer function. Z_B also has a zero in its transfer function located at about 65MHz. The two curves are related, and it is hard to determine mathematically exactly which parameter is affecting the performance, thus considerable lab work is required to obtain the maximum performance from the device.

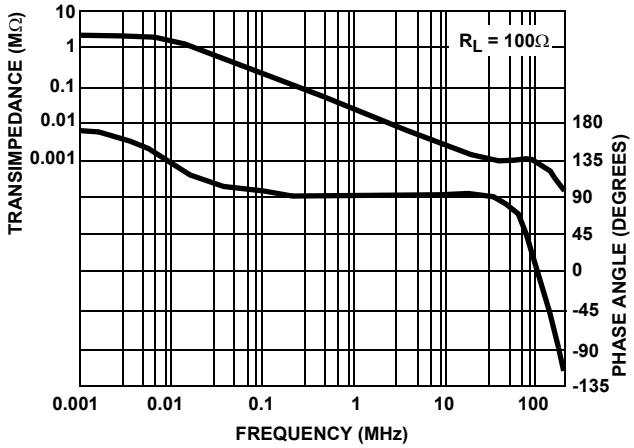

FIGURE 12. HA5020 TRANSIMPEDANCE vs FREQUENCY

Equation 27 yields an excellent starting point for designing a circuit, but strays and the interaction of parameters can make an otherwise sound design perform poorly. After the math analysis an equal amount of time must be spent on the circuit layout if an optimum design is going to be achieved. Then the design must be tested in detail to verify the performance, but more importantly, the testing must determine that unwanted anomalies have not crept into the design.

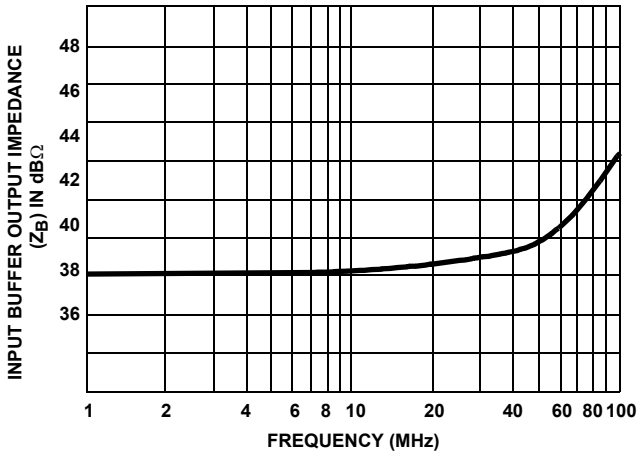

FIGURE 13. HA5020 INPUT BUFFER OUTPUT RESISTANCE vs FREQUENCY

Performance Analysis

Table 1 shows that the closed loop equations for both the CFA and VFA are the same, but the direct gain and loop gain equations are quite different. The VFA loop gain equation contains the ratio Z_F/Z_I, where Z_I is equivalent to Z_G, which is also contained in the closed loop gain equation. Because the loop gain and closed loop equations contain the same quantity, they are interdependent. The amplifier gain, a, is contained in the loop gain equation so the closed loop gain is a function of the amplifier gain. Because the amplifier gain decreases with an increase in frequency, the direct gain will decrease until at some frequency it equals the closed loop gain. This intersection always happens on a constant -20dB/decade line in a single pole system, which is why the VFA is considered to be a constant gain bandwidth device.

TABLE 1. SUMMARY OF OP AMP EQUATIONS

CIRCUIT CONFIGURATION	CURRENT FEEDBACK AMPLIFIER	VOLTAGE FEEDBACK AMPLIFIER
NON-INVERTING		
Direct Gain	$\frac{Z(1 + Z_F/Z_G)}{Z_F(1 + Z_B/Z_F \,\|\|Z_G)}$	a
Loop Gain	$Z/Z_F(1 + Z_B/Z_F\|\|Z_G)$	$aZ_G/(Z_G + Z_F)$
Closed Loop Gain	$1 + Z_F/Z_G$	$1 + Z_F/Z_G$
INVERTING		
Direct Gain	$\frac{Z}{Z_G(1 + Z_B/Z_F\|\|Z_G)}$	$aZ_F/(Z_F + Z_G)$
Loop Gain	$Z/Z_F(1 + Z_B/Z_F\|\|Z_G)$	$aZ_G/(Z_G + Z_F)$
Closed Loop Gain	$-Z_F/Z_G$	$-Z_F/Z_G$

The CFA's transimpedance, which is also a function of frequency, shows up in both the loop gain and closed loop gain equations, Equations 18 and 22. The gain setting impedances, Z_F and Z_G, do not appear in the loop gain as a ratio unless they are multiplied by a secondary quantity, Z_B, so Z_F can be adjusted independently for maximum bandwidth. This is why the bandwidth of CFA's are relatively independent of closed loop gain. When Z_B becomes a significant portion of the loop gain the CFA becomes more of a constant gainbandwidth device.

Equation 5, which is rewritten here as Equation 29, expresses the error signal as a function of the loop gain for any feedback system. Consider a VFA non-inverting configuration where the closed loop gain is +1; then the loop gain, Aβ, is a. It is not uncommon to have VFA amplifier gains of 50,000 in high frequency op amps, such as the HA2841 [6], so the DC precision is then 100% (1/50,000) = 0.002%. In a good CFA the transimpedance is Z = 6MΩ, but Z_F =1kΩ so the DC precision is 100% (1075Ω/6MΩ) = 0.02%. The CFA often sacrifices DC precision for stability.

$$\text{Error} = V_I/(1 + A\beta) \qquad \text{(EQ. 29)}$$

The DC precision is the best accuracy that an op amp can obtain, because as frequency increases the gain, a, or the transimpedance, Z, decreases causing the loop gain to decrease. As the frequency increases the constant gainbandwidth VFA starts to lose gain first, then the CFA starts to lose gain. There is a crossover point, which is gain dependent, where the AC accuracy for both op amps is equal. Beyond this point the CFA has better AC accuracy.

The VFA input structure is a differential transistor pair, and this configuration makes it is easy to match the input bias currents, so only the offset current generates an offset error voltage. The time honored method of inserting a resistor, equal to the parallel combination of the input and feedback resistors, in series with the non-inverting input causes the bias current to be converted to a common mode voltage. VFAs are very good at rejecting common mode voltages, so the bias current error is cancelled. One input of a CFA is the base terminal of a transistor while the other input is the output of a low impedance buffer. This explains why the input currents don't cancel, and why the non-inverting input impedance is high while the inverting input impedance is low. Some CFAs, such as the HFA1120 [7], have input pins which enable the adjustment of the offset current. Newer CFAs are finding solutions to the DC precision problem.

Stability Calculations for Input Capacitance

When there is a capacitance from the inverting input to ground, the impedance Z_G becomes $R_G/(R_GC_Gs+1)$, and Equation 14 can be written in the form of Equation 30. Then the new values for Z_G are put into the equation to yield Equation 31. Notice that the loop gain has another pole in it: an added pole might cause an oscillation if it gets too close to the pole(s) included in Z. Since Z_B is small it will dominate the added pole location and force the pole to be at very high frequencies. When C_G becomes large the pole will move in towards the poles in Z, and the circuit may become unstable.

$$A\beta = Z/(Z_B + Z_F/Z_G(Z_G + Z_B)) \qquad \text{(EQ. 30)}$$

If $Z_B = R_B$, $Z_F = R_F$, and $Z_G = R_G||C_G$, Equation 30 becomes:

$$A\beta = \frac{Z}{R_F(1 + R_B/R_F||R_G)(R_B||R_F||R_GC_Gs + 1)} \qquad \text{(EQ. 31)}$$

Stability Calculations for Feedback Capacitance

When a capacitor is placed in parallel with the feedback resistor, the feedback impedance becomes $Z_F = R_F/(R_FC_Fs + 1)$. After the new value of Z_F is substituted into Equation 30, and with considerable algebraic manipulation, it becomes Equation 32.

$$A\beta = \frac{Z(R_FC_Fs + 1)}{R_F(1 + (R_B/R_F||R_G)(R_B||R_F||R_GC_Fs + 1)} \quad \text{(EQ. 32)}$$

The new loop gain transfer function now has a zero and a pole; thus, depending on the placement of the pole relative to the zero oscillations can result.

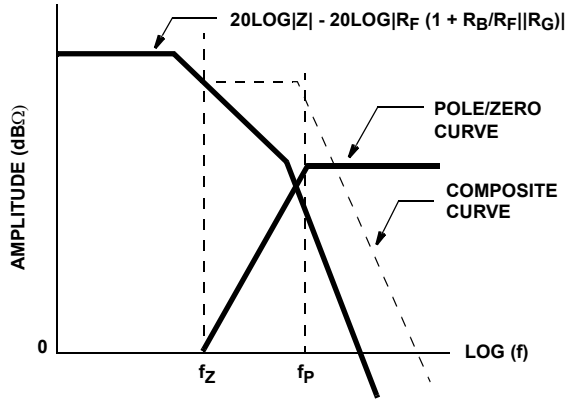

FIGURE 14. EFFECT OF C_F ON STABILITY

The loop gain plot for a CFA with a feedback capacitor is shown in Figure 14. The composite curve crosses the 0dBΩ axis with a slope of -40dB/decade, and it has more time to accumulate phase shift, so it is more unstable than it would be without the added poles and zeros. If the pole occurred at a frequency much beyond the highest frequency pole in Z then the Z pole would have a chance to roll off the gain before any phase shift from Z could add to the phase shift from the pole. In this case, C_F would be very small and the circuit would be stable. In practice almost any feedback capacitance will cause ringing and eventually oscillation if the capacitor gets large enough. There is the case where the zero occurs just before the Aβ curve goes through the 0dBΩ axis. In this case the positive phase shift from the zero cancels out some of the negative phase shift from the second pole in Z: thus, it makes the circuit stable, and then the pole occurs after the composite curve has passed through 0dBΩ.

Calculations and Compensation for C_G and C_F

Z_G and Z_F are modified as they were in the previous two sections, and the results are incorporated into Equation 30, yielding Equation 33.

$$A\beta = \frac{Z(R_FC_Fs + 1)}{R_F(1 + R_B/R_F||R_G)(R_B||R_F||R_G(C_F + C_G)s + 1)} \quad \text{(EQ. 33)}$$

Notice that if the zero cancelled the pole in equation that the circuit AC response would only depend on Z, so Equation 34 is arrived at by doing this. Equation 35 is obtained by algebraic manipulation.

$$(R_FC_Fs + 1) = (R_B||R_F||R_G(C_F + C_G)s + 1) \quad \text{(EQ. 34)}$$

$$R_FC_F = C_GR_GR_B/(R_G + R_B) \quad \text{(EQ. 35)}$$

Beware, R_B is a frequency sensitive parameter, and the capacitances may be hard to hold constant in production, but the concept does work with careful tuning. As Murphy's law predicts, any other combination of these components tends to cause ringing and instability, so it is usually best to minimize the capacitances.

Summary

The CFA is not limited by the constant gain bandwidth phenomena of the VFA, thus the feedback resistor can be adjusted to achieve maximum performance for any given gain. The stability of the CFA is very dependent on the feedback resistor, and an excellent starting point is the device data sheet which lists the optimum feedback resistor for various gains. Decreasing R_F tends to cause ringing, possible instability, and an increase in bandwidth, while increasing R_F has the opposite effect. The selection of R_F is critical in a CFA design; start with the data sheet recommendations, test the circuit thoroughly, modify R_F as required and then test some more. Remember, as Z_F approaches zero ohms, the stability decreases while the bandwidth increases; thus, placing diodes or capacitors across the feedback resistor will cause oscillations in a CFA.

The laboratory work cannot be neglected during CFA circuit design because so much of the performance is dependent on the circuit layout. Much of this work can be simplified by starting with the manufacturers recommended layout; Intersil appreciates the amount of effort it takes to complete a successful CFA design so they have made evaluation boards available. The layout effort has already been expended in designing the evaluation board, so use it in your breadboard; cut it, patch it, solder to it, add or subtract components and change the layout in the search for excellence. Remember ground planes and grounding technology! These circuits will not function without good grounding techniques because the oscillations will be unending. Coupled with good grounding techniques is good decoupling. Decouple the IC at the IC pins with surface mount parts, or be prepared to fight phantoms and ghosts.

Several excellent equations have been developed here, and they are all good design tools, but remember the assumptions. A typical CFA has enough gain bandwidth to ridicule most assumptions under some conditions. All of the CFA parameters are frequency sensitive to a degree, and the art of circuit design is to push the parameters to their limit.

Although CFAs are harder to design with than VFAs, they offer more bandwidth, and the DC precision is getting better. They are found in many different varieties; clamped outputs, externally compensated, singles, duals, quads and many special functions so it is worth the effort to learn to design with them.

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