Introduction

Computers and telecom equipment are steadily becoming more complex, providing ever higher levels of performance. Simultaneously, the selling price for this equipment is being driven ever lower by market competition. Integral to all of this equipment is a power conversion system which converts the incoming unregulated power from the utility, or other source, to the multiple regulated voltages required by the equipment. In present designs the power subsystem constitutes a significant part of the equipment cost and volume.

The development of a unique power converter(s) for each new system is a substantial cost item in the equipment development. Frequently the equipment will have a variety of configurations with differing power requirements. To save development cost only a single design is often used to cover a range of loads. The result is that many users have to pay for capability not needed in their particular configuration.

One means to reduce power subsystem over capacity and cost is to use a distributed power system where the power processing functions are distributed within the system and more power processing capacity is added as required when more capability is installed. A typical distributed system will have a central power processor which converts the raw input power into a regulated DC bus. The central power processor is relatively simple but it does provide for line isolation and the safety requirements for the system. The central processor may be modular to allow for power scaling as the loads change. Each board or group of boards within the equipment has a small power processor which converts the DC bus to the voltages required by that particular section of the equipment. In general these board level converters are quite simple and efficient. Frequently no DC isolation is required at the board level which further simplifies the converters.

The use of multiple small power converters allows a custom system to be designed using high volume, low cost, standardized modules. In a complex system there can be substantial cost savings.

Board space is always at a premium and the localized power converters take up space. In general height is severely constrained and the power converter has a low profile geometry which tends to increase the board area required. In order to minimize the area required, the switching frequency (fs) of the converter is pushed as high as possible. The latest generation of systems use converters with fs in the low MHz.

In addition to minimizing board area there are other requirements placed on these converters. The components must be small enough for automated insertion and be low cost. All of this has to be achieved without seriously reducing conversion efficiency. Poor efficiency would increase the size and cost of the input converter and create thermal problems within the unit.

Overall these “simple” converters represent a significant design challenge.

Converter Circuits For MHz Switching

Many possible circuit topologies exist which could be used. They fall into three general categories: switchmode, resonant and quasi-resonant. At the power levels typical of board mounted converters (1 to 100W) single switch topologies are usually preferred for their lower cost. Examples of typical single switch, PWM converters are shown in Figure 1. A comparison of the switch, diode and capacitor voltages for these circuits is given in Table 1. In general circuits with the switch referenced to the ground node are preferred to simplify the switch drive circuits. The boost, Cuk and SEPIC circuits are non-isolated circuits with ground referenced switches. The flyback and forward converters provide isolation as well as multiple outputs with a single, ground referenced switch. The price paid for using an isolating transformer is higher cost and the increasing difficulty of designing a high performance transformer as the frequency is raised. The simpler non-isolated topologies are usually preferred in a distributed system unless there are compelling reasons to provide isolation.

Table 1. Component Voltage Stress for Various Topologies

<table>
<thead>
<tr>
<th>CIRCUIT</th>
<th>V_SWITCH</th>
<th>V_DIODE</th>
<th>V_COUPLING</th>
</tr>
</thead>
<tbody>
<tr>
<td>Buck</td>
<td>V_I</td>
<td>V_I</td>
<td>N/A</td>
</tr>
<tr>
<td>Forward</td>
<td>V_I/(1-D)</td>
<td>V_O/(1-D)</td>
<td>N/A</td>
</tr>
<tr>
<td>Boost</td>
<td>V_O</td>
<td>V_O</td>
<td>N/A</td>
</tr>
<tr>
<td>Flyback</td>
<td>V_I/(1-D)</td>
<td>V_O/D</td>
<td>N/A</td>
</tr>
<tr>
<td>Buck-Boost</td>
<td>V_I + V_O</td>
<td>V_I + V_O</td>
<td>N/A</td>
</tr>
<tr>
<td>SEPIC</td>
<td>V_I + V_O</td>
<td>V_I + V_O</td>
<td>V_I</td>
</tr>
<tr>
<td>Cuk</td>
<td>V_I + V_O</td>
<td>V_I + V_O</td>
<td>V_I + V_O</td>
</tr>
</tbody>
</table>

NOTE: V_I = Input Voltage, V_O = Output Voltage, D = Duty Cycle
output voltage ratios are needed or a large variation in input voltage is present.

When implemented with discrete components the high frequency performance of switchmode circuits is limited by the parasitic inductance and capacitance normally present. This is due to the very fast voltage and current transitions required for efficient power conversion. One way to get around these problems is to modify the circuit such that it exploits the parasitic elements as part of normal operation. A boost version of a zero voltage switching quasi-resonant converter (ZVS-QRC) is shown in Figure 3. This is a typical example of this class of circuit. Many others exist [6, 7, 8, 9] and most switchmode topologies can be implemented as ZVS-QRC. This circuit operates quasi-resonant; i.e. during a portion of the switching cycle the waveforms are sinusoidal like a resonant converter and during other portions of the switching cycle the waveforms are essentially straight line segments like a non-resonant switchmode converter.

![Converter Circuits Diagram](image)

**FIGURE 1. CONVERTER CIRCUITS, M = \( \frac{V_o}{V_i} \)**

![Quadratic Converters Diagram](image)

**FIGURE 2. QUADRATIC CONVERTERS**
The primary advantage of this topology is that the switch turns on and off while the voltage across the switch is zero. This translates to essentially zero switching loss and very low stress during switching transitions. The inherent junction capacitance of the switch is utilized as an active component as well as the series package inductance. This enables the switch to operate efficiently at very high frequencies (10MHz+). A price has to be paid for this performance. The converter can only be controlled by varying frequencies (fs). This is a relatively simple control scheme to implement but sometimes leads to EMI problems, particularly if the range of variation of fs is large. If fixed frequency operation is desired another switch must be added to the circuit. An additional disadvantage is that the switch voltage will be much higher than the input or output voltages. Peak switch voltages of 3 to 5 times the input voltage are typical. There are also restrictions on the acceptable load ranges and the switching frequency range can be large under some conditions.

Some improvement in performance can be obtained by operating the converter in a ZVS-multiresonant mode [10, 11]. Two examples are given in Figure 4. In this topology both the switch and the diode operate with low switching stress. This circuit does however, still have many of the disadvantages of the ZVS-QRC.

MOSFETs are inherently fast switching devices. If the input capacitance can be charged quickly enough they are capable of sub-nanosecond switching. However, in discrete or even hybrid circuits, the parasitic inductance in the gate and source connections limits the charge rate, increasing the switching transition time. The parasitic inductance and capacitance associated with the drain circuit causes voltage and current ringing which can over stress the switch and associated components, increase the switching loss and create VHF radiated and conducted EMI.

For power levels typically used in distributed power systems, a power IC manufactured with the Intersil PASIC [12] (Power Applications Specific Integrated Circuit) process is an excellent way to minimize the parasitic elements that limit circuit performance and increase the level of integration. Other advantages of the PASIC technology is that the IC design can provide on-chip temperature monitoring and high speed, on-chip, current sensing. Moreover, on chip gate drivers help reduce and confine gate drive current and parasitic capacitance associated with external power transistors. Because the switch and its drive circuitry can be integrated onto a very small area, nanosecond switching times are readily achieved. For volume production the IC has the advantage of much smaller size and lower cost than discrete equivalents.

Some external power components will still be needed, but they can be arranged to minimize parasitics. In the SEPIC converter shown in Figure 5, C1 would be a chip ceramic capacitor and D1 would be a surface mounted Schottky diode. Both of these components would be placed immediately adjacent to the IC. Efficient and economical 1MHz designs using this concept are presently in volume production.

Using Switchmode Circuits at MHz Frequencies
One of the primary motivations for developing resonant and quasi-resonant topologies has been to overcome the problems associated with switchmode converters when they are operated with high fs. While these approaches have been helpful, in general some price must be paid. This often takes the form of higher conduction losses, higher voltage stress, more numerous and larger components, loss of PWM control and limited load and input voltage ranges.

If the problems associated with high frequency operation can be overcome then switchmode circuits are advantageous. The limitations of switchmode converters for MHz operation stem primarily from the difficulty of switching rapidly enough and the effect of parasitic components on the circuit behavior. An example of the parasitics present in a typical power stage is shown in Figure 5.
It is possible to have floating or “high side” switches in the PASIC process for use with the buck topology shown in Figure 1. However, by using the SEPIC topology, the power DMOS transistor source may be returned to ground. This results in much simplified and efficient gate driving circuits. Moreover, a shorted or open power transistor is not detrimental to the load in the SEPIC topology. Because of the load coupling capacitor and the switch being returned to ground in the SEPIC topology, a shorted or open power transistor will not place the full high voltage input voltage on the load as in the buck topology. Besides the SEPIC topology, there is a host of topologies that may be implemented with a grounded source device, among them is the boost, forward, flyback, Cuk, and quadratic topologies.

The SEPIC Converter

The boost, Cuk, flyback and forward converters are well known to power supply designers and information on their design is widely available[13, 14 and 15]. The SEPIC topology has however, not been widely used. The following information is provided to familiarize designers with this circuit and its characteristics.

The name SEPIC is an acronym for Single-Ended Primary Inductance Converter. The circuit was first developed at AT&T Bell laboratories [16] in the mid 1970s. The intent of the developers was to create a new topology with properties not available in contemporary topologies. Of particular interest is the ability to buck or boost the input voltage without inverting voltage polarity.

A typical SEPIC circuit is shown in Figure 6A. This circuit has three dynamic energy storage elements, L1, L2 and C1. The behavior of any switchmode circuit is strongly dependent on the continuity of the currents in the inductors and the voltages on the capacitors. A number of different operating modes are possible depending whether the inductor currents and capacitor voltages are continuous or discontinuous. As shown in Table 2, there are six possible inductor current operating modes. The -C entries are for conditions where one inductor current goes to zero before the other causing that inductor current to reverse direction. The inductor current is still continuous but the circuit behavior is different. The -D entries are for conditions where one inductor current goes negative and then a state exists where the two inductor currents are constant. The modes shown in Table 2 assume the voltage on C1 is constant (small ripple). An additional set of modes is possible if the voltage on C1 is discontinuous. While all modes are possible, the usual operating mode is to have the voltage on C1 continuous and either both L1 and L2 in continuous conduction or both L1 and L2 in discontinuous conduction. These two modes will be the only ones for which the circuit behavior will be derived in this applications note and will be referred to as the CCM and DCM modes, respectively. There is a brief discussion of four other modes which may be encountered.

CCM Circuit Operation

For this analysis it is assumed that both C1 and C2 are sufficiently large that the voltage ripple across them is small. By tracing the DC path from V1 through C1, L1, L2 and back to V1 we see that VC1 = V1. By inspection it can be seen that VC2 = VO.

When S1 is on, D1 is off and when S1 is off, D1 is on. This means there are two circuit states during each switching cycle. The two states are shown in Figures 6B and 6C.

When S1 is closed, L1 is directly across V1 and I1 is increasing. Energy is being stored in L1. C1 is connected across L2 and I2 is increasing. The energy in C1 is being transferred to L2. IO is being maintained by C2.

When S1 is opened, the energy in L1 is discharged into C1 and C2. The energy in L2 is discharged into C2. For CCM operation some energy remains in L1 and L2 (I1 and I2 ≠ 0). At the end of the switching sequence S1 is again closed and the cycle repeated.

To make the following discussion easier to follow, the details of the circuit analysis have been omitted. The equation derivations can be found in the appendix.

The ratio of the output voltage to the input voltage and the duty cycle are defined as:

\[ M = \frac{V_O}{V_I} \]  \hspace{1cm} \text{Equation 1} \\

\[ D = \frac{t_{ON}}{T} \]  \hspace{1cm} \text{Equation 2}

Where tON is the on time of S1 and T = 1/fs, the switching period.
D as a function of M is:

\[ D = \frac{M}{M + 1} \] Equation 3

And M as a function of D is:

\[ M = \frac{D}{1 - D} \] Equation 4

A graph of Equation 4 is given in Figure 7 with comparisons to the buck, boost, Cuk and buck-boost converters. The large signal input-to-output voltage ratio for the SEPIC is identical to the Cuk and buck boost circuits except that there is no polarity inversion. \( V_O \) may be either less than or greater than \( V_I \) depending on D.

### TABLE 3. SEPIC CCM VOLTAGES AND CURRENTS

<table>
<thead>
<tr>
<th>M</th>
<th>( \frac{V_O}{V_I} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>D</td>
<td>( \frac{M}{M + 1} )</td>
</tr>
<tr>
<td>M</td>
<td>( \frac{D}{1 - D} )</td>
</tr>
<tr>
<td>(I1)RMS</td>
<td>( M I_O )</td>
</tr>
<tr>
<td>(I2)RMS</td>
<td>( I_O \sqrt{M + 1} )</td>
</tr>
<tr>
<td>V_L1</td>
<td>( V_O, M \geq 1 ) and ( V_O/M, M \leq 1 )</td>
</tr>
<tr>
<td>V_S1</td>
<td>( \frac{M + 1}{M} V_O = V_O + V_I )</td>
</tr>
<tr>
<td>(I_S1)AVG</td>
<td>( M I_O )</td>
</tr>
<tr>
<td>(I_S1)RMS</td>
<td>( I_O \sqrt{M^2 + M} )</td>
</tr>
<tr>
<td>V_C1</td>
<td>( V_O/M = V_I )</td>
</tr>
<tr>
<td>(I_C1)RMS</td>
<td>( I_O \sqrt{M} )</td>
</tr>
<tr>
<td>V_L2</td>
<td>( V_O, M \geq 1 ) and ( V_O/M, M \leq 1 )</td>
</tr>
<tr>
<td>(I2)RMS</td>
<td>( I_O )</td>
</tr>
<tr>
<td>V_D1</td>
<td>( \frac{M + 1}{M} V_O = V_O + V_I )</td>
</tr>
<tr>
<td>(I_D1)AVG</td>
<td>( I_O )</td>
</tr>
<tr>
<td>(I_D1)RMS</td>
<td>( I_O \sqrt{M + 1} )</td>
</tr>
<tr>
<td>V_C2</td>
<td>( V_O )</td>
</tr>
<tr>
<td>(I_C2)RMS</td>
<td>( I_O \sqrt{M} )</td>
</tr>
</tbody>
</table>

Expressions for the voltages and currents in other circuit elements as a function of \( M, V_O \) and \( I_O \) are given in Table 3. Note that the expressions for the peak value for \( V_{L1} \) and \( V_{L2} \) depend on whether \( M > 1 \) or \( M < 1 \). The expressions in Table 3 assume that \( L_1 \) and \( L_2 \) are large with only small current ripple. For the case where the inductors are operating close the CCM-DCM boundary, the current waveforms will be triangular rather than rectangular and the RMS values will be approximately 15% higher.

The boundary between CCM and DCM modes will depend on several variables. For a given load resistance \( (R_L = V_O/I_O) \), \( f_s \) and \( M \), the values for the critical inductances of \( L_1 \) and \( L_2 \) are:

\[ L_{1C} = \left[ \frac{1}{2 f_s (M^2 + M)} \right] R_L \] Equation 5

\[ L_{2C} = \left[ \frac{1}{2 f_s (M + 1)} \right] R_L \] Equation 6

If the inductor values are higher than critical, then the converter will operate in CCM. If the values for the inductors are less than critical then the converter will operate in DCM.

The ratio of \( L_{2C} \) to \( L_{1C} \) is:

\[ \frac{L_{2C}}{L_{1C}} = M \] Equation 7

A very important point here is that the currents in \( L_1 \) and \( L_2 \) go to zero simultaneously only if \( L_2/L_1 = M \)! If \( V_O \) is held constant and \( V_I \) is varied then the CCM-DCM transition will occur at some other point and will involve an intermediate mode.

In distributed power systems \( V_I \) is the DC bus and is normally relatively well regulated so the \( M \) varies only over a small range. In that type of an application, a smooth transition from both inductors in CCM to both in DCM will be possible. If \( L_2/L_1 \) does not equal \( M \) then the circuit behavior will be quite different.
During this state (t_2 to T) the inductor currents are constant (ideally) because the voltage across \( C_1 \) cancels the input voltage. The conduction mode shown in Figure 8 is a continuous conduction mode but different from the continuous conduction mode where the current is unidirectional in both inductors. In the mode shown in Figure 9 the inductor currents are continuous but because of the period of time where \( \frac{di}{dt} = 0 \) (t_2 to T) the circuit will operate in a discontinuous mode. This mode corresponds to the C, -D mode in Table 2.

Both of these modes, C, -C and C, -D, have different characteristics from those mentioned in the previous discussion of continuous mode operation. The conditions where the current in \( L_1 \) reaches zero before the current in \( L_2 \) will be similar.

**CCM Circuit Example**

The following numerical example is provided to give a feeling for the component sizes and stresses in a typical application for the SEPIC converter.

Let:
\[
V_I = 35V \\
V_O = 12V \\
P_O = 50W \\
f_s = 1MHz
\]

From this it can be seen that:
\[
I_O = 4.2A \\
R_L = 2.88\Omega \\
M = 0.34
\]

From Equations 5 and 6:
\[
L_{1C} = 3.2\mu H \\
L_{2C} = 1.1\mu H
\]

To operate well within CCM and minimize the RMS currents let:
\[
L_1 = 5\mu H \\
L_2 = 1.7\mu H
\]

These inductors could be a single layer, wound on small powdered iron or NiZn ferrite cores. From the equations in Table 3:
\[
V_{S1} = 47V \\
(I_{S1})_{RMS} = 2.8A \text{ RMS}
\]

A MOSFET with \( BV_{DSS} = 60V \) would be appropriate for \( S_1 \).
\[
V_{D1} = 47V \\
(I_{D1})_{AVG} = 4.2A
\]

A 60V Schottky diode could be used for \( D_1 \).
\[
V_{C1} = 35V \\
(I_{C1})_{RMS} = 2.4A \text{ RMS}
\]

For \( C_1 \) a 50V, 0.47 to 1\( \mu \text{F} \), multilayer, ceramic chip capacitor would be appropriate.
\[
V_{C2} = 12V \\
(I_{C2})_{RMS} = 2.4A \text{ RMS}
\]

For \( C_2 \) a 25V, 1\( \mu \text{F} \), ceramic chip capacitor would be appropriate.
DCM Circuit Operation

The following discussion assumes that \( L_2/L_1 = M \) and that both inductors go into discontinuous conduction simultaneously. Operation in the DCM mode adds an additional circuit state as shown in Figure 10. At \( t = 0 \), the point at which \( S_1 \) is turned on, \( I_1 \) and \( I_2 = 0 \). The current in both inductors will rise until \( S_1 \) turns off (Figure 10A) and the energy in the inductors is discharged into the output (Figure 10B). When the inductor currents reach zero, \( D_1 \) stops conducting and the final state is assumed (Figure 10C). No current flows in the inductors because the voltage on \( C_1 \) cancels \( V_I \). The expressions for \( D \) and \( M \) are:

\[
D = \sqrt{2 \tau_L \left[ \frac{M^3}{M + 1} \right]} \quad \text{Equation 8}
\]

Where:

\[
\tau_L = \frac{f_s L_1}{R_L} \quad \text{Equation 9}
\]

Equation 8 is only valid for \( D < 1 \). This sets an upper limit on \( \tau_L \) of:

\[
(\tau_L)_{\text{MAX}} = \frac{M + 1}{2M^3} \quad \text{Equation 10}
\]

Values of \( \tau_L \) greater than this limit mean that the converter is operating in CCM for the particular value of \( M \).

Graphs of Equation 8 are given in Figures 11 and 12. These graphs illustrate the effect of varying load on the output voltage for \( M > 1 \) and \( M < 1 \).

### Coupled Inductor Operation

Referring to Figure 6, when \( S_2 \) is closed, the voltage across both \( L_1 \) and \( L_2 \) is equal to \( V_I \). Figure 6B shows that for the remainder of the switching cycle the voltage across \( L_1 \) and \( L_2 \) is equal to \( V_O \). Because these two voltages are equal and in phase, \( L_1 \) and \( L_2 \) may be integrated into a single magnetic structure with only one magnetic path, this is referred to as a coupled inductor. A coupled inductor version of the SEPIC topology[14] is shown in Figure 13. This topology has several advantages. The leakage inductance of the coupled inductor can be arranged to effect zero current ripple on the input with finite value of \( L \). Because the turns ratio

\[
\frac{L_2}{L_1} = M
\]
References


Appendix

SEPIC Equation Derivations for CCM and DCM Operation

CCM Operation

The following calculations are referenced to Figure 6.

For C1 and C2 large: \( V_{C1} = V_L \) and \( V_{C2} = V_O \)

When \( S_1 \) is closed: \( V_{L1} = V_{L2} = V_L \)

When \( S_1 \) is open: \( V_{L1} = V_{L2} = -V_O \)

By conservation of flux in the inductors:

\[
V_L t_{ON} = V_O (T - t_{ON})
\]

For \( D = t_{ON}/T \) and \( M = V_O/V_L \) Equation A1 reduces to:

\[
M = D/(1 - D)
\]

Equation A2 can be inverted:

\[
D = M/(M + 1)
\]

Assuming that \( L_1 \) and \( L_2 \) are sufficiently large that the current ripple is small and substituting A3

\[
I_O = (I_1 + I_2)(1 - D) = (I_1 + I_2)(1/(M + 1))
\]

For Power In = Power Out:

\[
V_L I_1 = V_O I_O, \quad M = V_O/V_L = I_1/I_O
\]

Combining Equations A4 and A5:

\[
I_2 = I_O
\]

S1 Voltage and Current

For \( S_1 \) open:

\[
V_{S1} = V_{C1} + V_O = V_L + V_O
\]

Restating in terms of \( M \) and \( V_O \):

\[
V_{S1} = \left(1 + 1/M\right)V_O
\]

For \( S_1 \) closed:

\[
(I_{S1})_{RMS} = (I_1 + I_2)/\sqrt{D}
\]

Which reduces to:

\[
(I_{S1})_{RMS} = I_O\sqrt{\left(M + M^2\right)}
\]

D1 Voltage and Current

By inspection:

\[
(I_{D1})_{AVG} = I_O
\]

When \( S_1 \) is closed:

\[
V_{D1} = V_L + V_O = \left(1 + 1/M\right)V_O
\]

Note the switch and diode have the same peak voltage.
Inductor Currents

\((l_1)_{\text{RMS}} = I_1 = MIO\) \hspace{1cm} (A13)

\((l_2)_{\text{RMS}} = I_O\) \hspace{1cm} (A14)

This assumes small current ripple. If smaller inductors are used such that the inductor currents are nearly triangular (near the DCM-CCM boundary) the RMS current values will be approximately 15% higher.

Capacitor Currents

\([(l_{C1})_{\text{RMS}} = \sqrt{\frac{2}{l_1}}(1-D)+l_2^2}\) \hspace{1cm} (A15)

Which reduces to: \([(l_{C1})_{\text{RMS}} = I_O \sqrt{M}\) \hspace{1cm} (A16)

\([(l_{C2})_{\text{RMS}} = \sqrt{\frac{2}{l_2}}D + (l_1 + l_2 - l_O)^2}\) \hspace{1cm} (A17)

Which reduces to: \([(l_{C2})_{\text{RMS}} = I_O \sqrt{M}\) \hspace{1cm} (A18)

Values for the Critical Inductances of \(L_1\) and \(L_2\)

For a given current, the critical inductance is the value for the inductor that allows the current to just reach zero at the end of the switching cycle. This is a special case of CCM.

\(L_1\) Critical

The input current will be triangular. \(I_{1P}\) = peak value of the current:

\(I_{1P} = V/I_{1ON}/L_1\) \hspace{1cm} (A20)

\(I_{1ON} = DT\) \hspace{1cm} (A21)

\(fs = 1/T\) \hspace{1cm} (A22)

Combining Equations A19 - A22:

\(L_{1C} = \frac{1}{2fsM(M+1)}R_L\) \hspace{1cm} (A23)

A similar calculation for \(L_2\) yields:

\(L_{2C} = R_L/(2fs(M + 1))\) \hspace{1cm} (A24)

DCM Analysis

For this analysis it will be assumed that:

\(L_{2C}/L_{1C} = M\) \hspace{1cm} (A25)

This means \(I_1\) and \(I_2\) go to zero simultaneously. The circuit states shown in Figure 10 will be used for this analysis.

\(t_1 = t_{ON} = \text{on time of } S_1\)

\(t_2 = \text{the current fall time in the inductors}\)

From conservation of flux in \(L_1\) and \(L_2\):

\(V_{I_1} = V_{I_2}\) \hspace{1cm} (A26)

From conservation of charge in \(C_1\)

\(I_{1AVG}l_2 = I_{2AVG}l_1\) \hspace{1cm} (A27)

From conservation of power:

\(V_{I_1AVG} = V_{I_2}\) \hspace{1cm} (A28)

Derivation of Expressions for \(M\) and \(D\)

\(I_{1P} = V/I_{1ON}/L_1\)

\(I_{1AVG} = I_{1P} \left[ \frac{l_1 + l_2}{2T} \right]\)

\(D = \sqrt{\frac{2fsL_1}{R_L}} \left[ \frac{M^3}{M+1} \right]\)
Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any damages and losses incurred by you or third parties arising from the use of these circuits, software, or information.

2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.

3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.

4. You shall not alter, modify, copy, or reengineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any damages and losses incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.

5. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality.” The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.

   “Standard” : Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment, industrial robots, etc.

   “High Quality”: Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations, etc.), or may cause serious property damage (space systems; underwater repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.

6. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.

7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to, redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.

8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.

9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.

10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.

11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.

12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.