Application of Intersil Digitally Controlled Potentiometers (XDCP™) as Hybrid Analog/Digital Feedback System Control Elements

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For the most part, the universe of feedback system design separates neatly into two fundamental design paradigms: analog-based designs and digital-based designs. Both design strategies are characterized by advantages and liabilities that generally make one or the other a clearly superior choice for any given application. Pure analog designs, for example, tend to display design simplicity and low development costs that play well in the context of smaller system applications. Digital-based designs, by contrast, have essentially unlimited flexibility in computation of the feedback function and therefore dominate in more complex feedback applications in which higher development costs (generally including software implementation) can be justified. Sometimes, a feature of particular utility in digital designs is the availability of digital memory with its ability to store feedback parameters for arbitrary lengths of time without drift. This makes possible a variety of system solutions including multiple system operating modes in which feedback values can be acquired in some modes and then applied in others.

But what about feedback systems that lie in between these clear opposites? What about, relatively simple cost-sensitive applications that would benefit from functions that are difficult to implement in analog circuits and would therefore require digital techniques?

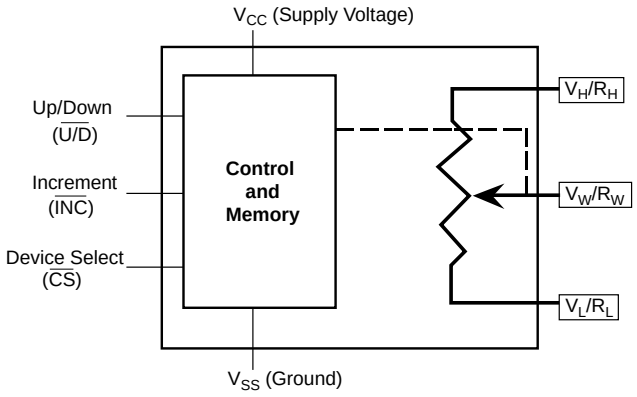

FIGURE 1. DIGITALLY-CONTROLLED POTENTIOMETER

A basis for a useful middle ground between the extremes of pure analog or pure digital feedback designs is offered by an inexpensive component: the Intersil 3-wire digitally controlled potentiometer. Figure 1 illustrates the architecture of the 3-wire XDCP. The 3-wire XDCP is seen to comprise a digital input and an analog output interface. The 3-wire XDCP digital input interface consists of a bidirectional counter controlled by (direction [U/D], clock [INC] inputs, and chip select/EEPROM-store [CS] logic signals). The XDCP analog output interface consists of the digitally controlled variable resistance potentiometer element.

A generalized basic conceptual topology representative of feedback control systems based on the 3-wire XDCP is illustrated in Figure 2. It comprises six design elements:

A. The XDCP Error Integrator. During the feedback process, the XDCP closes the feedback loop by accumulating successive samples of the system state in its up/down control counter.

B. Clocking Oscillator. The oscillator controls the rate of feedback sampling. Therefore, selection of the oscillator period must be based on consideration of both the minimum response time of the XDCP (< 500µs for typical Intersil parts) and of the rest of the feedback system as determined by such factors as the gain-bandwidth products of the op amp and comparator. Appropriate oscillator periods will typically lie in the range of 1 to 100 milliseconds.

C. Analog/Digital Feedback (Voltage Comparator). Conversion between the analog state of the output node and the digital U/D XDCP input is the traditional role of the analog comparator. However, the flexibility of the CMOS logic inputs of Intersil XDCPs often makes it possible to substitute a simple passive voltage-translation network, as illustrated in the design applications to follow.

D. Digital/Analog Feedback (Resistance Element Circuitry). Closure of the feedback loop is achieved by incorporation of the variable resistance element of the XDCP into the active circuitry of the rest of the feedback system.

E. Intermittent Feedback Control Circuitry (Selectable Operating Modes). Some uniquely versatile XDCP-based feedback control applications derive their utility from the ability to implement multiple operation modes in which circuit setpoints (e.g. precision op amp offset null) derived from one operating mode (e.g. autonull mode) are retained in XDCP memory and used in a subsequently selected system mode (e.g. DC amplification). Control and selection of such system operating modes is easily achieved through the use of inexpensive, logic-compatible, CMOS analog switch elements such as the 74HC4053.

F. Operational Amplifier. Essentially all precision analog systems that can benefit from XDCP-based feedback designs will incorporate at least one monolithic op amp. Selection of a suitable (e.g. adequate gain, bandwidth, DC accuracy) op amp is therefore an important step in the feedback system design process.

Figure 2's conceptual topology has been utilized to advantage in a variety of real-life applications. Examples include:

Auto-Nulling Delta-T Thermometer

Some precision temperature measurement applications, such as acquiring the temperature rise of a heatsink in response to a thermal load, are inherently concerned with temperature change relative to an initial value rather than absolute temperature. In such applications, important improvement in measurement resolution can be gained from the scale expansion made possible by acquisition of the initial baseline temperature and subtracting it from subsequent measurements before analog to digital conversion. Figure 3 presents an auto-nulling thermometric circuit that performs this function automatically using digitally controlled potentiometers as the baseline temperature memory.

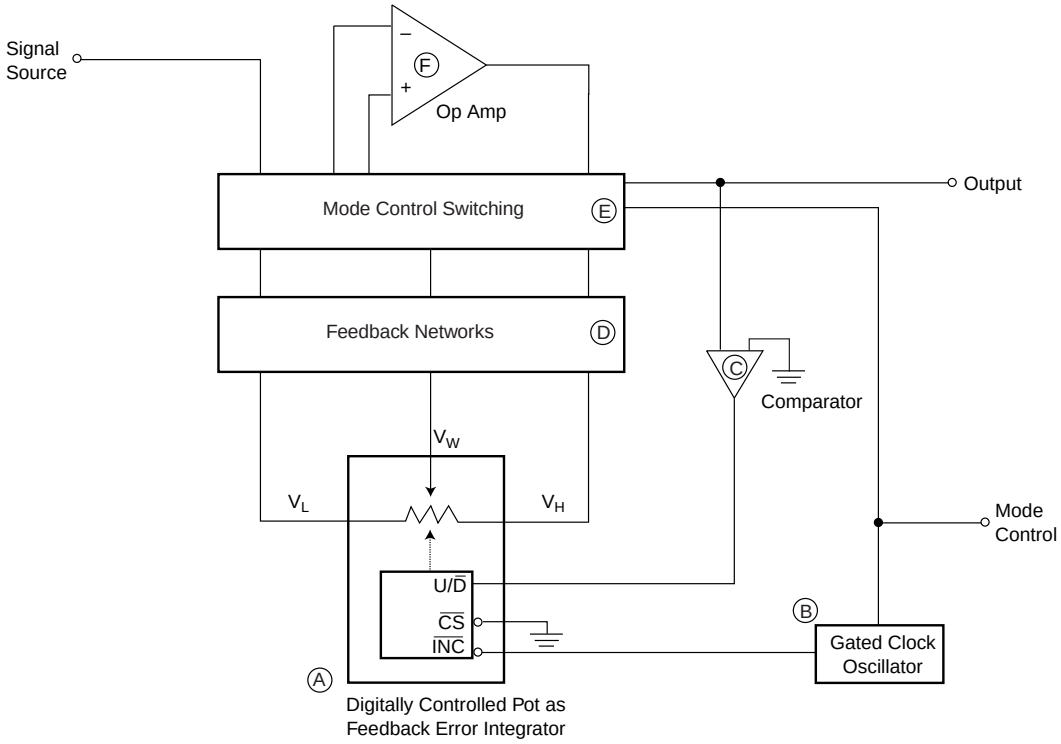

FIGURE 2. BASIC XDCP-BASED FEEDBACK CONTROL LOOP

The basis for temperature sensing in this circuit is Rt, a standard 100Ω @ 25°C Pt RTD. Such devices have a highly stable and accurate tempco of +0.385Ω/°C. Therefore the -lmA of excitation current provided by R1 leads to a temperature-dependent signal of ~385uV/1°C.

R2, P1, and R3 complete a ratiometric bridge with A1 as the bridge amplifier. The feature of the circuit that utilizes the ability of digitally-controlled-pot's to act as feedback elements is the process that automatically captures and holds the initial reference temperature that is subtracted from subsequent readings. Acquisition of a reference temperature is initiated by bringing the 5V logic signal ACQUIRE high. This causes S3 to open the feedback loop around A1 and simultaneously enables the S1-S2 multivibrator. The result is to cause P1 to sample A1's output at a 100Hz rate and drive A1 toward null.

The 100Hz sampling rate is determined by the R8, R9, C1 timing components in the S1-S2 multivibrator with the oscillator period approximately equal to C1(R8 + R9). The relatively long (~10ms) period is dictated by the operation of A1 as an open-loop comparator while in null mode. Op amps such as A1 make relatively good comparators in terms of ultimate DC accuracy, but they have much slower response times (multiple millisecond slew times) than true comparators, especially when the differential input voltage is near null. Because the AD822 op amp has a gain-bandwidth product of ~3MHz, the time required for a 5V output slew is approximately 5V/(3MHz* Vin) = 1.7ms/mV. Therefore, allowing ~10ms settling time between output-state samples implies a null-point resolution of +/-170µV = +/-0.50°C.

If ACQUIRE is held low long enough (1 second will always suffice), the result will be for P1 to be driven to the setting that causes A1 to dither around zero output, indicating that P1's setting is alternating between the two values that bracket optimum T0 null.

When ACQUIRE is returned to logic "1", P1 will retain the bridge-ratio needed to cancel the temperature present at Rt during the nulling process and cause the thermometric signal presented to scaling op amp A2 to be referenced to this initial T0. Because P1 setpoint memory is digital, it will hold this ratio forever unless ACQUIRE is deliberately put through another 0/1 cycle to acquire a new T0, or power is removed from the thermometer.

A2 applies the necessary gain, digitally fine-adjusted by P2, of 01/.000385 = 25.97 to achieve an output scale factor of 10mV/°C.

Op Amp Offset Nulling

Op amp applications that need the highest possible DC accuracy are generally best served by CMOS chopper-stabilized amplifiers such as the LTC1050. But high-speed, low-noise applications may require high-performance rockets such as the 700-MHz LT1226. So what to do for applications that need it *all*? Sometimes a composite topology in which a bipolar amplifier provides gain-bandwidth and a CMOS chopper acts as an offset-nulling service can do the job. Such arrangements can successfully null out offset-voltage errors. But these circuits can get messy if you also need bias-current-related error correction. The circuit in Figure 4 offers an error-cancellation method that handles both error sources.

The circuit consists of op amp IC1 (e.g., Linear Technology's LT1226), CMOS multiplexer SC (one-third of an HC4053), and digital potentiometer P1 (Intersil's X9C103). The topology supports two modes of operation as selected by the TTL/CMOS-compatible NADJ signal. NADJ = 0 connects IC1 as a standard noninverting gain block. The circuit values shown, combined with the impressive specs of the frequency-compensated LT1226, provide a gain of 1001 with bandwidth extending from DC to beyond 500 kHz and input-related noise of approximately 2 nV/$\sqrt{Hz}$.

Null-adjustment mode occurs when NADJ = 1 disconnects the input source and effectively causes IC1's output to run open-loop. IC1's output then slews to one rail or the other, as determined by the sign of its net offset error. If R3 = RS - R1||R2, where RS is the DC source resistance, then IC1's output reflects the sum of both voltage *and* current bias errors. The circuit level shifts and filters IC1's output and applies it to the up/down control input of P1. This action sets up P1's internal up/down-counter logic to increment of decrement one step, depending on the state of IC1's output and thus on the sign of IC1's offset. The counter step occurs on the subsequent NADJ = 0 transition.

The connection of the VL, VW, and VH terminals of P1 to the nulling terminals of IC1 closes a feedback loop that tends to push IC1 one step toward null for every 10 cycles of NADJ. Because the X9C103 has 100 resolved settings, the technique requires a maximum of 99 NADJ pulses to complete the nulling process. After nulling, P1 retains the final null setting in digital memory as long as the 5V supply remains connected or until the nulling process repeats. Observed performance reveals that using an OP37 consistently achieves residual-offset errors of less than 5 µV.

If it is inconvenient to provide an external NADJ clock source in a given application, you can add the SA/SB multivibrator at Node 1. This 1-kHz clock circuit receives its gating from the CMOS-compatible anull signal, such that anull = 1 enables continuous null adjustment, and anull = 0 enables normal amplifier operation. The maximum anull duration required to achieve initial null is 100msec. If desired, you can also include D1, R8, and C3 at Node 2 to provide an automatic null on each power-up cycle.

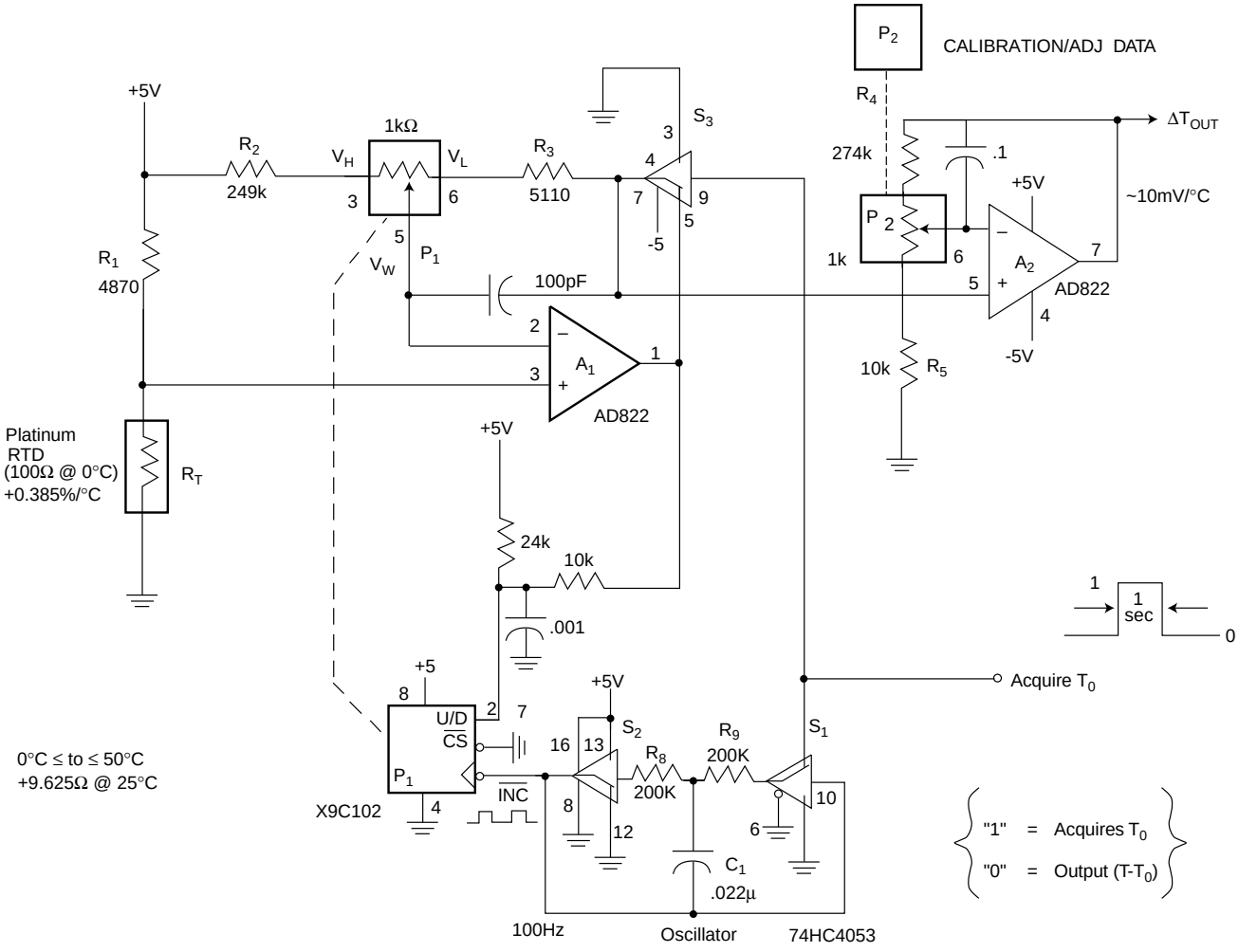

FIGURE 3. AUTONULLING 'ΔT" THERMOMETER—DETAILED

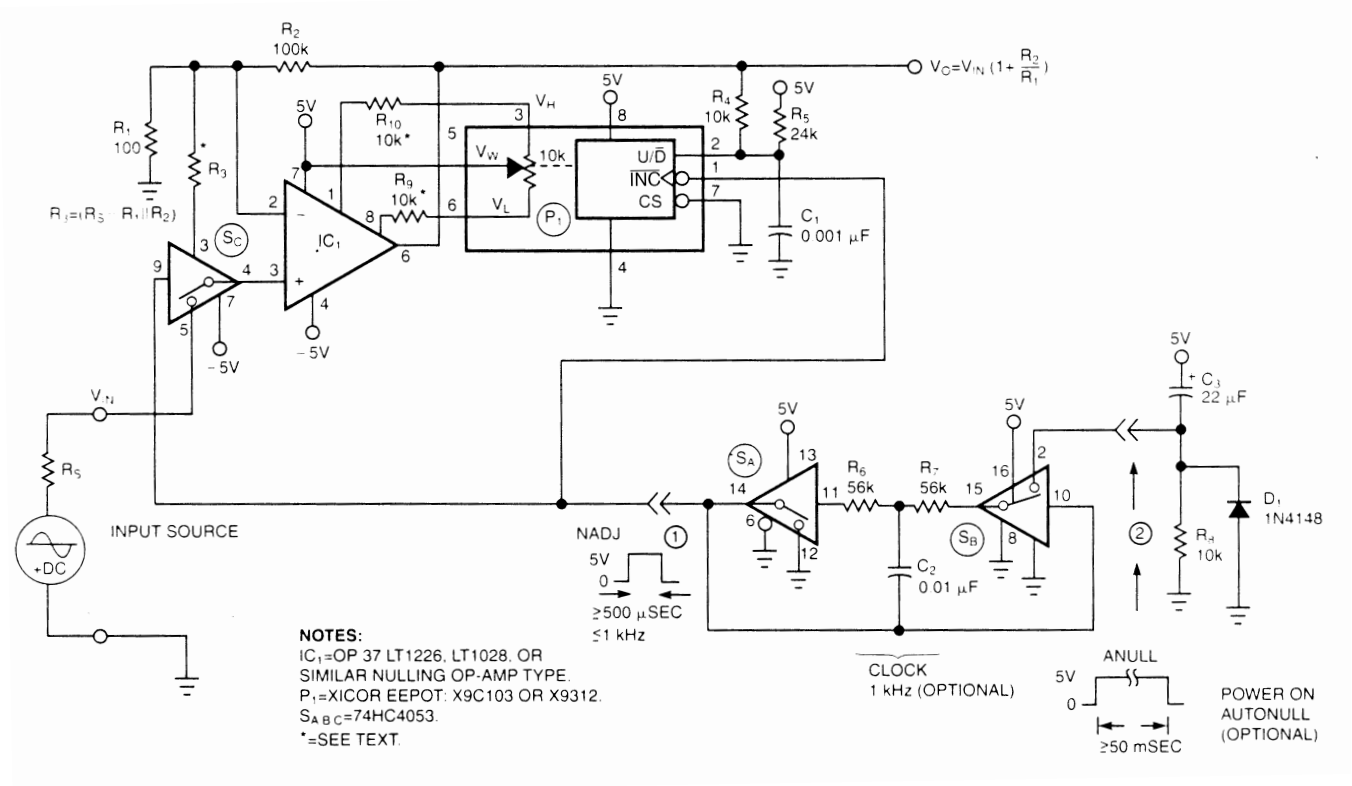

FIGURE 4. HAVE YOUR CAKE (HIGH SPEED) AND EAT IT (LOW DC ERRORS) TOO, WITH THIS AUTONULLING CIRCUIT, USING A DIGITALLY CONTROLLED POTENTIOMETER

Although Figure 4 shows an LT1226, the circuit works without modification with an OP37 and LT1028. The circuit is also pin-compatible with the popular LT1128, OP07, OP77, OP177, and µ725 op amps. With these op amps, however, the circuit may require a slower NADJ clock rate and a longer nulling interval (increase C2 and C3), because of the lower gain-bandwidth product of these compensated types. The circuit can accommodate many other op-amp types with a simple change of pin connections. The circuit can handle 15V positive-rail operations by substituting an X9312 for the X9C103 with no other changes.

Power Amplifier Biasing

The day may be near when every amplifier application can be served simply by finding the right off-the-shelf stand-alone chip. But for now, many jobs require that even the best monolithic devices be supplemented with a sprinkling of active discrete devices. One such category of application is the high-output-current, high-frequency buffer amplifier in Figure 5.

Of course it's simplicity in itself to add an arbitrary amount of muscle to a "milquetoast" op amp by following it with a class AB complementary bipolar emitter-follower or FET source follower pair like Q1 and Q2 in Figure 5. Many successful driver designs are based on just this elementary topology. But all such designs must confront the problem of stable DC biasing of the follower while avoiding unconscionable amounts of quiescent power draw and unbearable levels of harmonic distortion. This is a problem fraught with the classic twin-design-bogeymen of thermal runaway and cross-over distortion.

The new solution to this old puzzle described here comprises an automatic bias adjustment loop consisting of a Intersil digital potentiometer P1, International Rectifier photovoltaic optoisolator O1, CMOS switches S1-S3, and Linear Technology op amps A2-3. The resulting adjustment loop includes two modes of operation selected by the CMOS/TTL-compatible ADJ input.

When ADJ = 0, S3 closes a normal feedback loop around A1 and the Q1/Q2 pair thus forcing the circuit to become a fairly normal gain of -5 amplifier with a bandpass of DC to 10 MHz, full power bandwidth (limited by A1 slew) of 5 MHz, and output limits of ±10V and ±10A. Harmonic distortion over the full operating range is minimized by the impressive GBW of capacitive-load-compatible A1 combined with stable quiescent biasing of the Q1/Q2 pair to a thrifty no signal value of 50 mA. The trick behind these performance numbers is the way an appropriate bias level for the follower is achieved, one that's independent of temperature and component tolerance variations.

To understand how this is done, consider how the circuit rearranges itself when ADJ = 1 causes S3 to disconnect A1's input from the signal source and substitute a ground reference. Simultaneously, the S1/S2, 20-Hz multivibrator is enabled and begins clocking P1. In response, P1 begins to vary the input to A3, which then services the control current into O1 and thus the net gate bias voltage at the follower MOSFETs.

This action combines with A2 to establish a feedback loop, which tends to drive the follower pair to the desired zero-signal bias. This action occurs because if the follower bias current IQ is less than 50 mA, then the drop across R3 will be less than the drop across R4. As a result, A2 drives the Up/Down input of P1 high (up). Therefore, on the next negative transition of the clock, the VW terminal of P1 will make one step toward the VH terminal. This increases the drive to C1 which ups the follower bias.

If IQ is more than 50 mA, then A2's output state will reverse, causing P1 to step VW toward VL and decrease the follower quiescent bias. Consequently, after a maximum of 5 seconds and 99 multivibrator cycles, the follower bias will have been forced to converge to the bias level set by the R4/R3 ratio. ADJ may then be reset to zero for normal amplifier operation; the final bias setting will be retained by P1 until either power is removed or a new ADJ cycle initiated. Thermal coupling between D1/Q1 and D2/Q2 improves overall bias stability between adjustment cycles.

Although illustrated with ±15-V supplies, the unique "Over-The-Top" input topology of A2 is compatible with V+ voltages as high as 36 V (but be careful to observe A1 limitations). Also, there is no requirement that the V+ and V- voltages be symmetrical. Many variations are possible when selecting A1 and the follower MOSFETs to achieve different combination of output capabilities.

Proportional-Integral Thermostat

A classic scheme for precision temperature control is the proportional-integral or "P/I" algorithm. In this method, the heater control equation consists of two terms. One term (P) is proportional to the instantaneous error differential between sensor and setpoint temperatures. The other (I) is proportional to the time integral of the error. P/I controllers characteristically have reasonably good dynamic response due to the proportional feedback term, nominally zero steady-state error thanks to the error integration term, and relatively simple loop optimization because only three adjustments (setpoint, proportional gain, and integrator time-constant) are involved in the setup process.

The simplicity of the P/I feedback algorithm argues for a similarly simple analog-based controller design. But some temperature-control applications involve long time-constants (running to minutes and hours) and often must live in hostile (hot and contaminated) industrial environments. These gremlins combine to make analog long-time-constant circuits problematic with their high impedances and nano-ampere signal currents. This is so because nasty ambients exaggerate the leakage and bias currents of op amps, integrator capacitors, and even circuit boards.

The controller shown in Figure 6 achieves adequate time-constants without the delicate high-impedance analog circuits. It uses Intersil's X9C103 digitally controlled potentiometers as feedback elements together with the Linear Technology LTC1040 sampled comparator.

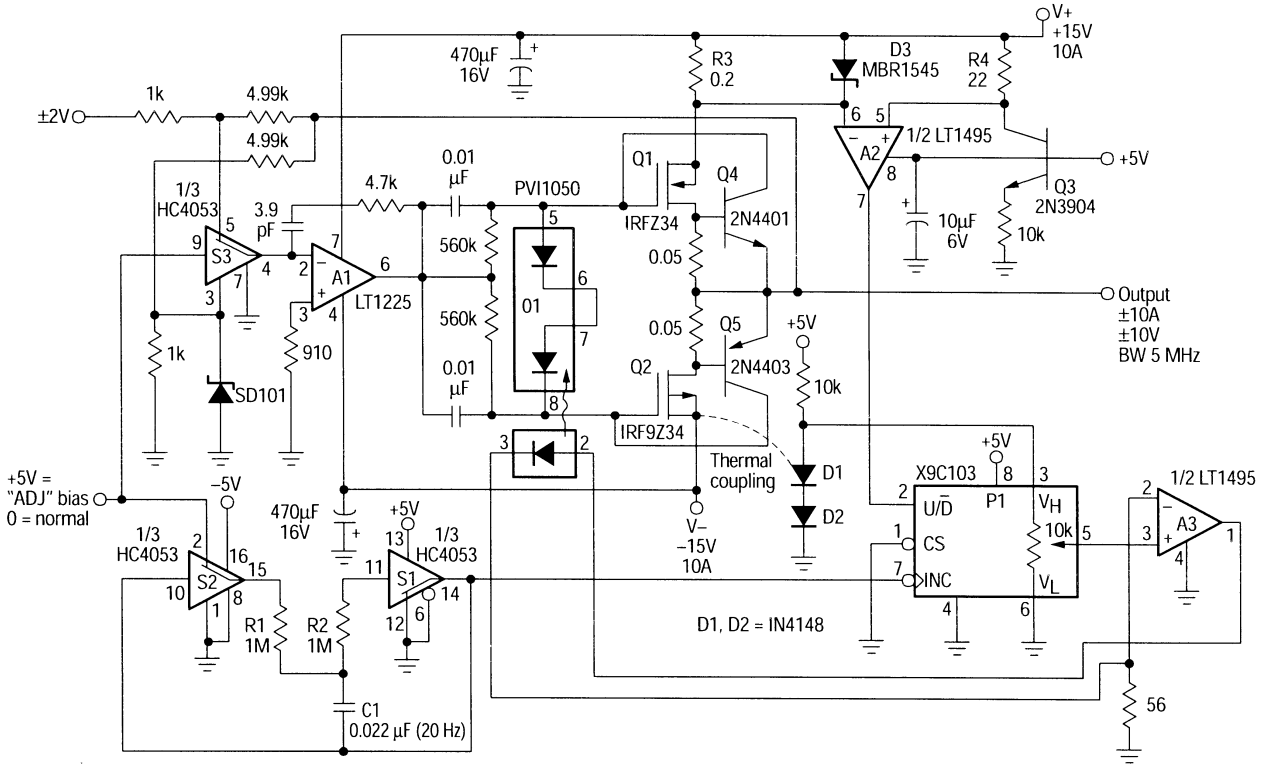

FIGURE 5. THIS HIGH-OUTPUT-CURRENT, HIGH-FREQUENCY BUFFER AMPLIFIER USES AN AUTOMATIC BIAS ADJUSTMENT LOOP, UTILIZING A INTERSIL DIGITAL POTENTIOMETER P1, TO MINIMIZE HARMONIC DISTORTION WHILE DRAWING A THRIFTY NO-SIGNAL SUPPLY CURRENT OF ONLY 50 mA

Controller operation is based upon a positive-temperature-coefficient (3850 ppm/°C) platinum RTD sensor arranged in a standard ratiometric bridge with reference resistors R1, R3, and R5, and setpoint pot R4. Aiding controller stability and precision is high level (≈5 mA) bridge excitation. It produces a relatively large 1.7 mV/°C RTD output signal that competes well against noise pickup and thermal-EMF error sources. Typically, such a high RTD drive level would threaten to produce large and unacceptable sensor self-heating errors. But in this case, sensor excitation is pulsed (80µs) under control of the LTC1040. This keeps average sensor dissipation duty factors low (≈1%) and self-heating error inconsequential.

On each measurement cycle, A1's lower input pair samples the bridge output. Depending on the result of the comparison, they tend to drive the pin 4 output bit to 0 or 1, as the bridge reports an RTD-setpoint differential that's negative or positive. Thus the solid-state relay (SSR) and heater will most likely turn on when the temperature is low and off when it is high.

To make the resulting on/off heater drive have an average duty-factor that is nicely proportional to the magnitude of the temperature error signal and not just a simple "bang-bang" relationship, the bridge output voltage is summed with a triangular dither signal produced by P2. The combination of P2 and U2 causes P2 to output one full triangular dither waveform every 128 measurement cycles.

Thermal inertia of the hearer and the thermal load averages over the heater cycle rate (1 Hz in this example). Consequently, suitable selection of the R6-C1 oscillator RC will avoid significant temperature ripple. R2 adjusts the amplitude of the P2 dither signal and thereby sets the effective controller P-term gain that relates heater duty factor to temperature error to get adequate control loop "stiffness" without oscillation.

Meanwhile, error integrator A2 + P1 also samples the temperature difference signal. The integration sampling frequency, and, therefore, the integrator time constant, is set by the choice of which U2 output bit is connected to P1's clock. This arrangement causes the integrator to take one step in the direction of zero setpoint error every 1, 2, 4, 8, 16, 32, 64, or 128 heater dither cycles. As a result, it gradually converges on zero temperature error.

Selecting the right U2 bit sets the integrator time constant anywhere from one minute to more than two hours, and can thus accommodate even the longest generally encountered control-loop thermal time delays.

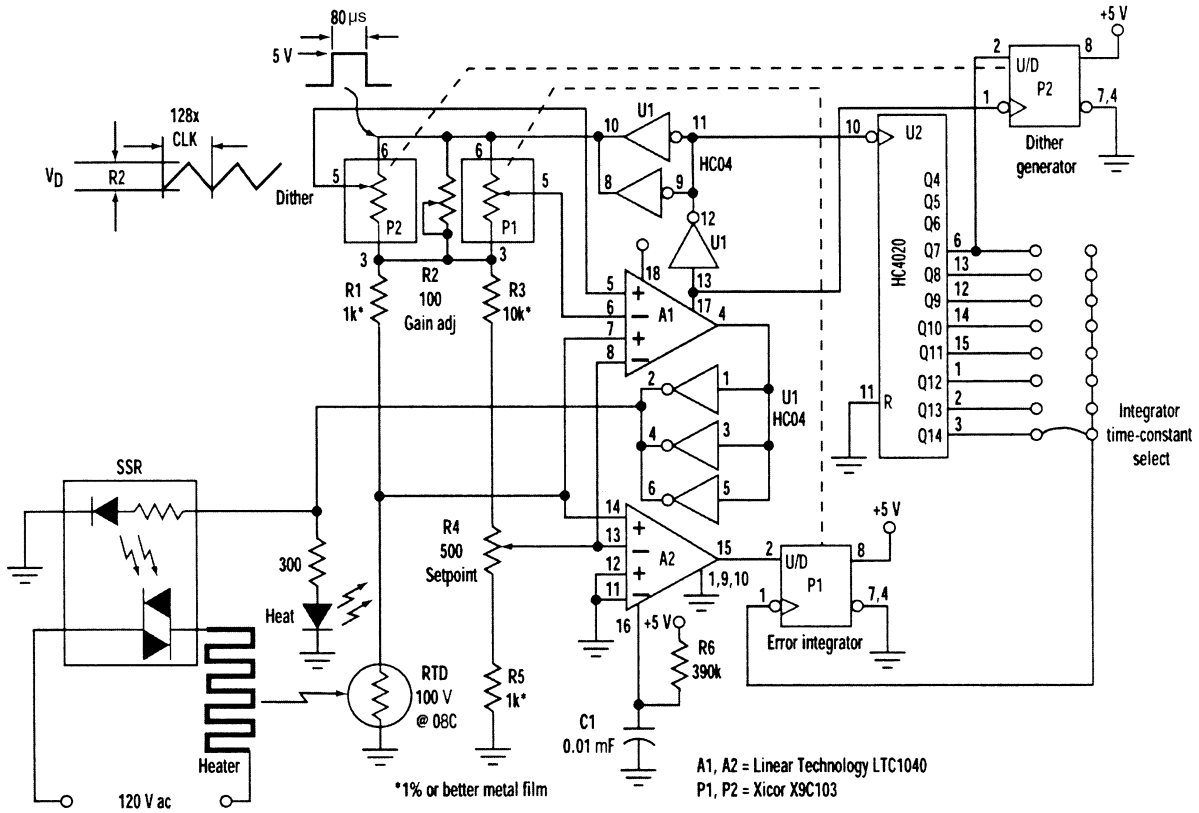

FIGURE 6. THIS CONTROLLER ACHIEVES EXTENDED TIME CONSTANTS WITHOUT DELICATE HIGH-IMPEDANCE ANALOG CIRCUITS BY USING INTERSIL'S X9C103 DIGITALLY-CONTROLLED POTENTIOMETERS AS FEEDBACK ELEMENTS, COMBINED WITH LINEAR TECHNOLOGY'S LTC1040 SAMPLED COMPARATOR

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