Principles of Data Acquisition and Conversion

Introduction

Data acquisition and conversion systems interface between the real world of physical parameters, which are analog, and the artificial world of digital computation and control. With current emphasis on digital systems, the interfacing function has become an important one; digital systems are used widely because complex circuits are low cost, accurate, and relatively simple to implement. In addition, there is rapid growth in use of minicomputers and microcomputers to perform difficult digital control and measurement functions.

Computerized feedback control systems are used in many different industries today in order to achieve greater productivity in our modern industrial society. Industries which presently employ such automatic systems include steel making, food processing, paper production, oil refining, chemical manufacturing, textile production, and cement manufacturing.

The devices which perform the interfacing function between analog and digital worlds are analog-to-digital (A/D) and digital-to-analog (D/A) converters, which together are known as data converters. Some of the specific applications in which data converters are used include data telemetry systems, pulse code modulated communications, automatic test systems, computer display systems, video signal processing systems, data logging systems, and sampled data control systems. In addition, every laboratory digital multimeter or digital panel meter contains an A/D converter.

Besides A/D and D/A converters, data acquisition and distribution systems may employ one or more of the following circuit functions:

Basic Data Distribution Systems

- Transducers
- Amplifiers
- Filters
- Nonlinear analog functions
- Analog multiplexers
- Sample-holds

The interconnection of these components is shown in the diagram of the data acquisition portion of a computerized feedback control system in Figure 1.

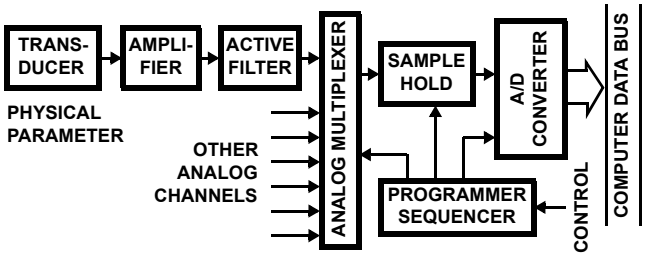


FIGURE 1. DATA ACQUISITION SYSTEM

The input to the system is a physical parameter such as temperature, pressure, flow, acceleration, and position, which are analog quantities. The parameter is first converted into an electrical signal by means of a transducer, once in electrical form, all further processing is done by electronic circuits.

Next, an amplifier boosts the amplitude of the transducer output signal to a useful level for further processing. Transducer outputs may be microvolt or millivolt level signals which are then amplified to 1 to 10V levels. Furthermore, the transducer output may be a high impedance signal, a differential signal with common-mode noise, a current output, a signal superimposed on a high voltage, or a combination of these. The amplifier, in order to convert such signals into a high level voltage, may be one of several specialized types.

The amplifier is frequently followed by a low pass active filter which reduces high frequency signal components, unwanted electrical interference noise, or electronic noise from the signal. The amplifier is sometimes also followed by a special nonlinear analog function circuit which performs a nonlinear operation on the high level signal. Such operations include squaring, multiplication, division, RMS conversion, log conversion, or linearization.

The processed analog signal next goes to an analog multiplexer which sequentially switches between a number of different analog input channels. Each input is in turn connected to the output of the multiplexer for a specified period of time by the multiplexer switch. During this connection time a sample-hold circuit acquires the signal voltage and then holds its value while an analog-to-digital converter converts the value into digital form. The resultant digital word goes to a computer data bus or to the input of a digital circuit.

Thus the analog multiplexer, together with the sample-hold, time shares the A/D converter with a number of analog input channels. The timing and control of the complete data acquisition system is done by a digital circuit called a programmer-sequencer, which in turn is under control of the computer. In some cases the computer itself may control the entire data acquisition system.

While this is perhaps the most commonly used data acquisition system configuration, there are alternative ones. Instead of multiplexing high-level signals, low-level multiplexing is sometimes used with the amplifier following the multiplexer. In such cases just one amplifier is required, but its gain may have to be changed from one channel to the next during multiplexing. Another method is to amplify and convert the signal into digital form at the transducer location and send the digital information in serial form to the computer. Here the digital data must be converted to parallel form and then multiplexed onto the computer data bus.

Basic Data Acquisition System

The data distribution portion of a feedback control system, illustrated in Figure 2, is the reverse of the data acquisition system. The computer, based on the inputs of the data acquisition system, must close the loop on a process and control it by means of output control functions. These control outputs are in digital form and must therefore be converted into analog form in order to drive the process. The conversion is accomplished by a series of digital-to-analog converters as shown. Each D/A converter is coupled to the computer data bus by means of a register which stores the digital word until the next update. The registers are activated sequentially by a decoder and control circuit which is under computer control.

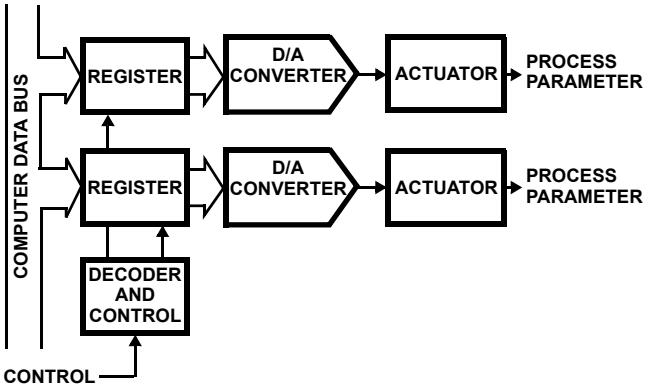


FIGURE 2. DATA DISTRIBUTION SYSTEM

The D/A converter outputs then drive actuators which directly control the various process parameters such as temperature, pressure, and flow. Thus the loop is closed on the process and the result is a complete automatic process control system under computer control.

Quantizing Theory

Introduction

Analog-to-digital conversion in its basic conceptual form is a two-step process: quantizing and coding. Quantizing is the process of transforming a continuous analog signal into a set of discrete output states. Coding is the process of assigning a digital code word to each of the output states. Some of the early A/D converters were appropriately called quantizing encoders.

Quantizer Transfer Function

The nonlinear transfer function shown in Figure 3 is that of an ideal quantizer with 8 output states; with output code words assigned, it is also that of a 3-bit A/D converter. The 8 output states are assigned the sequence of binary numbers from 000 through 111. The analog input range for this quantizer is 0 to +10V.

There are several important points concerning the transfer function of Figure 3. First, the resolution of the quantizer is defined as the number of output states expressed in bits; in this case it is a 3-bit quantizer. The number of output states for a binary coded quantizer is 2^n, where n is the number of bits. Thus, an 8-bit quantizer has 256 output states and a 12-bit quantizer has 4096 output states.

As shown in the diagram, there are 2^n-1 analog decision points (or threshold levels) in the transfer function. These points are at voltages of +0.625, +1.875, +3.125, +4.375, +5.625, +6.875, and +8.125. The decision points must be precisely set in a quantizer in order to divide the analog voltage range into the correct quantized values.

The voltages +1.25, +2.50, +3.75, +5.00, +6.25, +7.50, and +8.75 are the center points of each output code word. The analog decision point voltages are precisely halfway between the code word center points. The quantizer staircase function is the best approximation which can be made to a straight line drawn through the origin and full scale point; notice that the line passes through all of the code word center points.

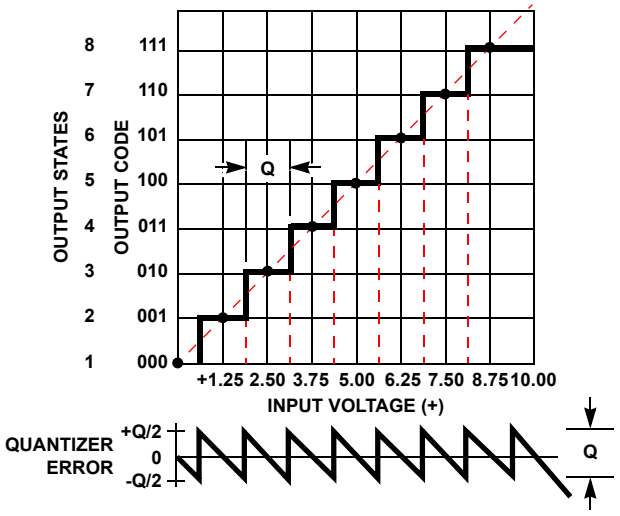


FIGURE 3. TRANSFER FUNCTION OF IDEAL 3-BIT QUANTIZER

Quantizer Resolution and Error

At any part of the input range of the quantizer, there is a small range of analog values within which the same output code word is produced. This small range is the voltage difference between any two adjacent decision points and is known as the analog quantization size, or quantum, Q. In Figure 3, the

quantum is 1.25V and is found in general by dividing the full scale analog range by the number of output states. Thus

$$Q = \frac{FSR}{2^n} \quad \text{(EQ. 1)}$$

where FSR is the full scale range, or 10V in this case. Q is the smallest analog difference which can be resolved, or distinguished, by the quantizer. In the case of a 12-bit quantizer, the quantum is much smaller and is found to be

$$Q = \frac{FSR}{2^n} = \frac{10V}{4096} = 2.44mV \quad \text{(EQ. 2)}$$

If the quantizer input is moved through its entire range of analog values and the difference between output and input is taken, a sawtooth error function results, as shown in Figure 3. This function is called the quantizing error and is the irreducible error which results from the quantizing process. It can be reduced only by increasing the number of output states (or the resolution) of the quantizer, thereby making the quantization finer.

For a given analog input value to the quantizer, the output error will vary anywhere from 0 to ±Q/2; the error is zero only at analog values corresponding to the code center points. This error is also frequently called quantization uncertainty or quantization noise.

The quantizer output can be thought of as the analog input with quantization noise added to it. The noise has a peak-to-peak value of Q but, as with other types of noise, the average value is zero. Its RMS value, however, is useful in analysis and can be computed from the triangular waveshape to be $Q/2\sqrt{3}$.

Sampling Theory

Introduction

An analog-to-digital converter requires a small, but significant, amount of time to perform the quantizing and coding operations. The time required to make the conversion depends on several factors; the converter resolution, the conversion technique, and the speed of the components employed in the converter. The conversion speed required for a particular application depends on the time variation of the signal to be converted and on the accuracy desired.

Aperture Time

Conversion time is frequently referred to as aperture time. In general, aperture time refers to the time uncertainty (or time window) in making a measurement and results in an amplitude uncertainty (or error) in the measurement if the signal is changing during this time.

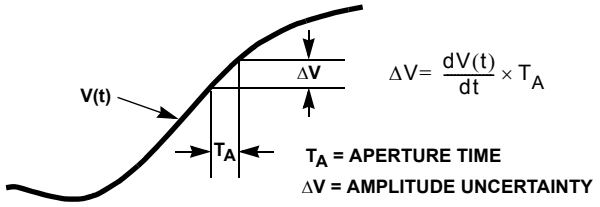


FIGURE 4. APETURE TIME AND AMPLITUDE UNCERTAINTY

As shown in Figure 4, the input signal to the A/D converter changes by ΔV during the aperture time T_A in which the conversion is performed. The error can be considered an amplitude error or a time error, the two are related as follows:

$$\Delta V = T_A \frac{dV(t)}{dt} \quad \text{(EQ. 3)}$$

where dV(t)/dt is the rate of change with time of the input signal.

It should be noted that ΔV represents the maximum error due to signal change, since the actual error depends on how the conversion is done. At some point in time within T_A, the signal amplitude corresponds exactly with the output code word produced.

For the specific case of a sinusoidal input signal, the maximum rate of change occurs at the zero crossing of the waveform, and the amplitude error is

$$\Delta V = T_A \frac{d}{dt}(A\sin\omega t)t = 0 = T_A A\omega \quad \text{(EQ. 4)}$$

The resultant error as a fraction of the peak to peak full scale value is

$$\varepsilon = \frac{\Delta V}{2A} = \pi f T_A \quad \text{(EQ. 5)}$$

From this result the aperture time required to digitize a 1kHz signal to 10 bits resolution can be found. The resolution required is one part in 2^{10} or 0.001.

$$T_A = \frac{\varepsilon}{\pi f} = \frac{0.001}{3.14 \times 10^3} = 320 \times 10^{-9} \quad \text{(EQ. 6)}$$

The result is a required aperture time of just 320ns!

One should appreciate the fact that 1kHz is not a particularly fast signal, yet it is difficult to find a 10-bit A/D converter to perform this conversion at any price! Fortunately, there is a relatively simple and inexpensive way around this dilemma by using a sample-hold circuit.

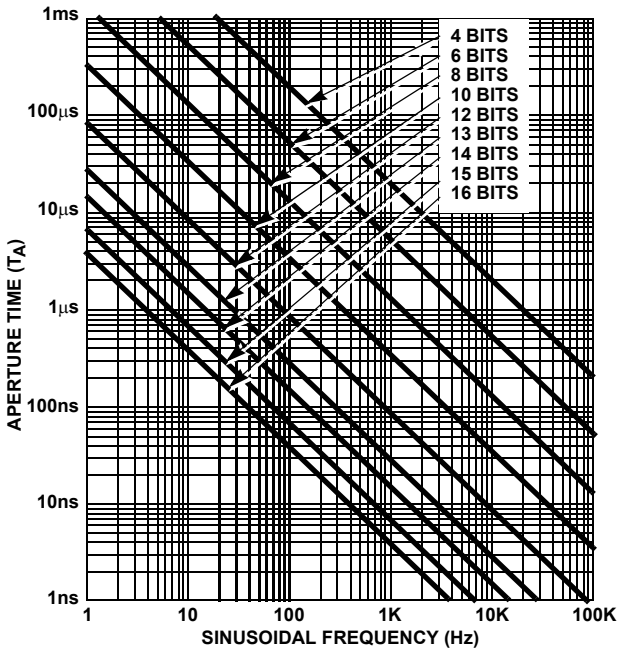


FIGURE 5. GRAPH FOR APERTURE ERROR FOR SINUSOIDAL SIGNALS

Sample-Holds and Aperture Error

A sample-hold circuit samples the signal voltage and then stores it on a capacitor for the time required to perform the A/D conversion. The aperture time of the A/D converter is therefore greatly reduced by the much shorter aperture time of the sample-hold circuit. In turn, the aperture time of the sample-hold is a function of its bandwidth and switching time.

Figure 5 is a useful graph of Equation 5. It gives the aperture time required for converting sinusoidal signals to a maximum error less than one part in 2^n where n is the resolution of the converter in bits. The peak to peak value of the sinusoid is assumed to be the full scale range of the A/D converter. The graph is most useful in selecting a sample-hold by aperture time or an A/D converter by conversion time.

Sampled-Data Systems and the Sampling Theorem

In data acquisition and distribution systems, and other sampled-data systems, analog signals are sampled on a periodic basis as illustrated in Figure 6. The train of sampling pulses in Figure 6B represents a fast-acting switch which connects to the analog signal for a very short time and then disconnects for the remainder of the sampling period.

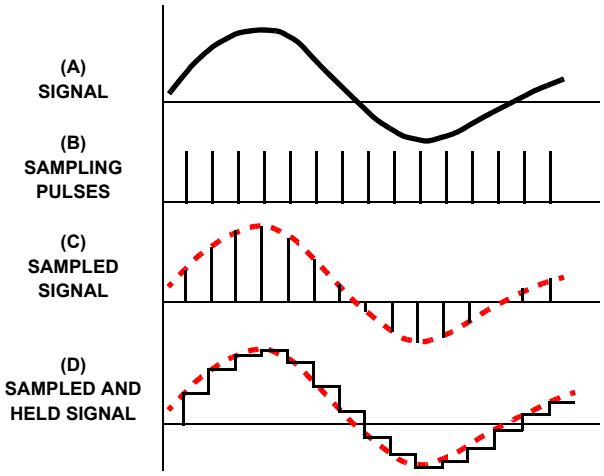


FIGURE 6. SIGNAL SAMPLING

The result of the fast-acting sampler is identical with multiplying the analog signal by a train of sampling pulses of unity amplitude, giving the modulated pulse train of Figure 6C. The amplitude of the original signal is preserved in the modulation envelope of the pulses. If the switch type sampler is replaced by a switch and capacitor (a sample-hold circuit), then the amplitude of each sample is stored between samples and a reasonable reconstruction of the original analog signal results, as shown in Figure 6D.

The purpose of sampling is the efficient use of data processing equipment and data transmission facilities. A single data transmission link, for example, can be used to transmit many different analog channels on a sampled basis, where-as it would be uneconomical to devote a complete transmission link to the continuous transmission of a single signal.

Likewise, a data acquisition and distribution system is used to measure and control the many parameters of a process control system by sampling the parameters and updating the control inputs periodically. In data conversion systems it is common to use a single, expensive A/D converter of high speed and precision and then multiplex a number of analog inputs into it.

An important fundamental question to answer about sample-data systems is this: “How often must I sample an analog signal in order not to lose information from it?” It is obvious that all useful information can be extracted if a slowly varying signal is sampled at a rate such that little or no change takes place between samples. Equally obvious is the fact that information is being lost if there is a significant change in signal amplitude between samples.

The answer to the question is contained in the well known Sampling Theorem which may be stated as follows: If a continuous bandwidth-limited signal contains no frequency components higher than f_C, then the original signal can be recovered without distortion if it is sampled at a rate of at least 2 f_C samples per second.

Frequency Folding and Aliasing

The Sampling Theorem can be demonstrated by the frequency spectra illustrated in Figure 7. Figure 7A shows the frequency spectrum of a continuous bandwidth-limited analog signal with frequency components out to f_C. When this signal is sampled at a rate f_S, the modulation process shifts the original spectrum out of f_S, $2f_S$, $3f_S$, etc. in addition to the one at the origin. A portion of this resultant spectrum is shown in Figure 7B.

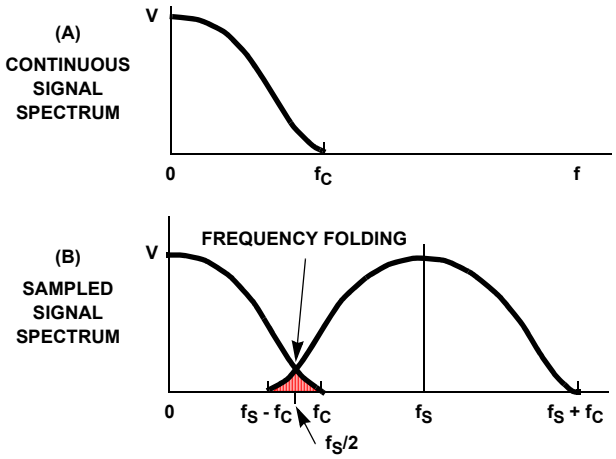


FIGURE 7. FREQUENCY SPECTRA DEMONSTRATING THE SAMPLING THEOREM

If the sampling frequency f_S is not high enough, part of the spectrum centered about f_S will fold over into the original signal spectrum. This undesirable effect is called frequency folding. In the process of recovering the original signal, the folded part of the spectrum causes distortion in the recovered signal which cannot be eliminated by filtering the recovered signal.

From the figure, if the sampling rate is increased such that $f_S - f_C > f_C$, then the two spectra are separated and the original signal can be recovered without distortion. This demonstrates the result of the Sampling Theorem that $f_S > 2f_C$. Frequency folding can be eliminated in two ways: first by using a high enough sampling rate, and second by filtering the signal before sampling to limit its bandwidth to $f_S/2$.

One must appreciate the fact that in practice there is always some frequency folding present due to high frequency signal components, noise and non-ideal pre-sample filtering. The effect must be reduced to negligible amounts for the particular application by using a sufficiently high sampling rate. The required rate, in fact, may be much higher than the minimum indicated by the Sampling Theorem.

The effect of an inadequate sampling rate on a sinusoid is illustrated in Figure 8; an alias frequency in the recovered signal results. In this case, sampling at a rate slightly less than twice per cycle gives the low frequency sinusoid shown by the dotted line in the recovered signal. This alias frequency can be significantly different from the original frequency. From the figure it is easy to see that if the sinusoid is sampled at least twice per cycle, as required by the Sampling Theorem, the original frequency is preserved.

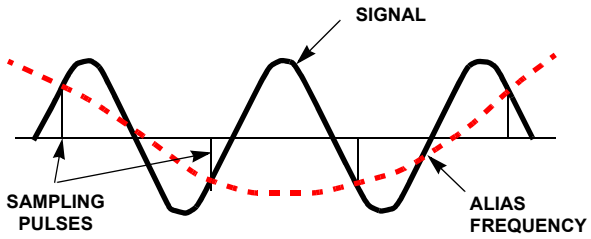


FIGURE 8. ALIAS FREQUENCY CAUSED BY INADEQUATE SAMPLING RATE

Coding for Data Converters

Natural Binary Code

A/D and D/A converters interface with digital systems by means of an appropriate digital code. While there are many possible codes to select, a few standard ones are almost exclusively used with data converters. The most popular code is natural binary, or straight binary, which is used in its fractional form to represent a number

$$N = a_1 2^{-1} + a_2 2^{-2} + a_3 2^{-3} + \ldots + a_n 2^{-n} \quad \text{(EQ. 7)}$$

where each coefficient “a” assumes a value of zero or one. N has a value between zero and one.

A binary fraction is normally written as 0.110101, but with data converter codes the decimal point is omitted and the code word is written 110101. This code word represents a fraction of the full scale value of the converter and has no other numerical significance.

The binary code word 110101 therefore represents the decimal fraction (1x0.5)+(1x0.25)+(1x0.125)+(1x0.0625)+(0x0.03125)+(1x0.015625)=0.828125 or 82.8125% of full scale for the converter. If full scale is +10V, then the code word represents +8.28125V. The natural binary code belongs to a class of codes known as positive weighted codes since each coefficient has a specific weight, none of which is negative.

The leftmost bit has the most weight, 0.5 of full scale, and is called the most significant bit, or MSB; the rightmost bit has the least weight, 2^{-n} of full scale, and is therefore called the least significant bit, or LSB. The bits in a code word are numbered from left to right from 1 to n.

The LSB has the same analog equivalent value as Q discussed previously, namely

$$\text{LSB (Analog Value)} = \frac{FSR}{2^n} \quad \text{(EQ. 8)}$$

Table 1 is a useful summary of the resolution, number of states, LSB weights, and dynamic range for data converters from one to twenty bits resolution.

TABLE 1. RESOLUTION NUMBER OF STATES, LSB WEIGHT, AND DYNAMIC RANGE FOR DATA CONVERTERS

RESOLUTION BITS (n)	NUMBER OF STATES (2^n)	LSB WEIGHT (2^{-n})	DYNAMIC RANGE (dB)
0	1	1	0
1	2	0.5	6
2	4	0.25	12
3	8	0.125	18.1
4	16	0.0625	24.1
5	32	0.03125	30.1
6	64	0.015625	36.1
7	128	0.0078125	42.1
8	256	0.00390625	48.2
9	512	0.001953125	54.2
10	1024	0.0009765625	60.2
11	2048	0.00048828125	66.2
12	4096	0.000244140625	72.2
13	8192	0.0001220703125	78.3
14	16384	0.00006103515625	84.3
15	32768	0.000030517578125	90.3
16	65536	0.0000152587890625	96.3
17	131072	0.00000762939453125	102.3
18	262144	0.000003814697265625	108.4
19	524288	0.0000019073486328125	114.4
20	1048576	0.00000095367431640625	120.4

The dynamic range of a data converter in dB is found as follows:

$$DR(dB) = 20\log 2^n = 20n\log 2 = 20n(0.301) = 6.02n \quad \text{(EQ. 9)}$$

where DR is a dynamic range, n is the number of bits, and 2^n the number of states of the converter. Since 6.02dB corresponds to a factor of two, it is simply necessary to multiply the resolution of a converter in bits by 6.02. A 12-bit converter, for example, has a dynamic range of 72.2dB.

An important point to notice is that the maximum value of the digital code, namely all 1's does not correspond with analog full scale, but rather with one LSB less than full scale, or f_S ($1-2^{-n}$). Therefore a 12-bit converter with a 0 to 10V analog range has a maximum code of 1111 1111 1111 and a maximum analog value of +10V ($1-2^{-12}$) = +9.99756V. In other words, the maximum analog value of the converter, corresponding to all one's in the code, never quite reaches the point defined as analog full scale.

Other Binary Codes

Several other binary codes are used with A/D and D/A converters in addition to straight binary. These codes are offset binary, two's complement, binary coded decimal (BCD), and their complemented versions. Each code has a specific advantage in certain applications. BCD coding for example is used where digital displays must be interfaced such as in digital panel meters and digital multimeters. Two's complement coding is used for computer arithmetic logic operations, and offset binary coding is used with bipolar analog measurements.

Not only are the digital codes standardized with data converters, but so are the analog voltage ranges. Most converters use unipolar voltage ranges of 0 to +5V and 0 to +10V although some devices use the negative ranges 0 to -5V and 0 to -10V. The standard bipolar voltage ranges are ±2.5V, ±5V and ±10V. Many converters today are pin-programmable between these various ranges.

TABLE 2. BINARY CODING FOR 8-BIT UNIPOLAR CONVERTERS

FRACTION OF f_S	+ 10V f_S	STRAIGHT BINARY	COMPLEMENTARY BINARY
$+f_S$-1 LSB	+9.961	1111 1111	0000 0000
$+3/4f_S$	+7.500	1100 0000	0011 1111
$+1/2f_S$	+5.000	1000 0000	0111 1111
$+1/4f_S$	+2.500	0100 0000	1011 1111
$+1/8f_S$	+1.250	0010 0000	1101 1111
+1 LSB	+0.039	0000 0001	1111 1110
0	0.000	0000 0000	1111 1111

Table 2 shows straight binary and complementary binary codes for unipolar 8-bit converter with a 0 to +10V analog f_S range. The maximum analog value of the converter is +9.961V, or one LSB less than +10V. Note that the LSB size is 0.039V as shown near the bottom of the table. The complementary binary coding used in some converters is simply the logic complement of straight binary.

When A/D and D/A converters are used in bipolar operation, the analog range is offset by half scale, or by the MSB value. The result is an analog shift of the converter transfer function as shown in Figure 9. Notice for this 3-bit A/D converter transfer function that the code 000 corresponds with -5V, 100 with 0V, and 111 with +3.75V. Since the output coding is the same as before the analog shift, it is now appropriately called offset binary coding.

FRACTION OF f_S	$\pm$5V f_S	OFFSET BINARY	COMP OFF BINARY	TWO'S COMPLEMENT	SIGN-MAG BINARY
$+f_S$-1 LSB	+4.9976	1111 1111	0000 0000	0111 1111	1111 1111
$+1/4f_S$	+3.7500	1110 0000	0001 1111	0110 0000	1110 0000
$+1/2f_S$	+2.5000	1100 0000	0011 1111	0100 0000	1100 0000
$+3/4f_S$	+1.2500	1010 0000	0101 1111	0010 0000	1010 0000
0	0.0000	1000 0000	0111 1111	0000 0000	1000 0000
$-1/4f_S$	-1.2500	0110 0000	1001 1111	1110 0000	0010 0000
$-1/2f_S$	-2.5000	0100 0000	1011 1111	1100 0000	0100 0000
$-3/4f_S$	-3.7500	0010 0000	1101 1111	1010 0000	0110 0000
$-f_S$+1 LSB	-4.9976	0000 0001	1111 1110	1000 0001	0111 1111
$-f_S$	-5.0000	0000 0000	1111 1111	1000 0000	--

NOTE: Sign Magnitude Binary has two code words for zero as shown here.

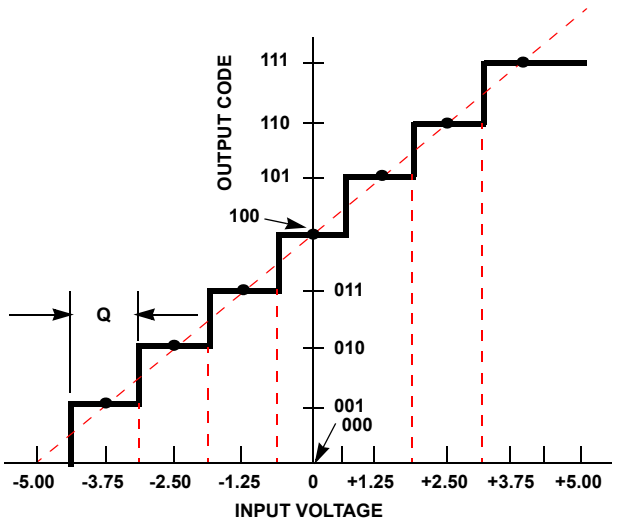


FIGURE 9. TRANSFER FUNCTION FOR BIPOLAR 3-BIT A/D CONVERTER

Table 3 shows the offset binary code together with complementary offset binary, two's complement, and sign-magnitude binary codes. These are the most popular codes employed in bipolar data converters.

TABLE 3. POPULAR BIPOLAR CODES USED WITH DATA CONVERTERS

	SIGN-MAG BINARY
0+	1000 0000 0000
0	0000 0000 0000

The two's complement code has the characteristic that the sum of the positive and negative codes for the same analog magnitude always produces all zero's and a carry. This characteristic makes the two's complement code useful in arithmetic computations. Notice that the only difference between two's complement and offset binary is the complementing of the MSB. In bipolar coding, the MSB becomes the sign bit.

The sign-magnitude binary code, infrequently used, has identical code words for equal magnitude analog values except that the sign bit is different. As shown in Table 3 this code has two possible code words for zero: 1000 0000 or 0000 0000. The two are usually distinguished as 0+ and 0-, respectively. Because of this characteristic, the code has maximum analog values of $\pm$ (f_S-1 LSB) and reaches neither analog $+f_S$ or $-f_S$.

BCD Codes

Table 4 shows BCD and complementary BCD coding for a 3 decimal digit data converter. These are the codes used with integrating type A/D converters employed in digital panel meters, digital multimeters, and other decimal display applications. Here four bits are used to represent each decimal digit. BCD is a positive weighted code but is relatively inefficient since in each group of four bits, only 10 out of a possible 16 states are utilized.

TABLE 4. BCD AND COMPLEMENTARY BCD CODING

FRACTION OF f_S	+10V f_S	BINARY CODED DECIMAL	COMPLEMENTARY BCD
$+f_S$-1 LSB	+9.99	1001 1001 1001	0110 0110 0110
$+3/4f_S$	+7.50	0111 0101 0000	1000 1010 1111
$+1/2f_S$	+5.00	0101 0000 0000	1010 1111 1111
$+1/4f_S$	+2.50	0010 0101 0000	1101 1010 1111
$+1/8f_S$	+1.25	0001 0010 0101	1110 1101 1010
+1 LSB	+0.01	0000 0000 0001	1111 1111 1110
0	0.00	0000 0000 0000	1111 1111 1111

The LSB analog value (or quantum, Q) for BCD is

$$\text{LSB (Analog Value)} = Q = \frac{FSR}{10^d} \qquad \text{(EQ. 10)}$$

where FSR is the full scale range and d is the number of decimal digits. For example if there are 3 digits and the full scale range is 10V, the LSB value is

$$\text{LSB (Analog Value)} = \frac{10\text{V}}{10^3} = 0.01\text{V} = 10\text{mV} \qquad \text{(EQ. 11)}$$

BCD coding is frequently used with an additional overrange bit which has a weight equal to full scale and produces a 100% increase in range for the A/D converter. Thus for a converter with a decimal full scale of 999, an overrange bit provides a new full scale of 1999, twice that of the previous one. In this case, the maximum output code is 1 1001 1001 1001. The additional range is commonly referred to as $^1/_2$ digit, and the resolution of the A/D converter in this case is $3^1/_2$ digits.

Likewise, if this range is again expanded by 100%, a new full scale of 3999 results and is called $3^3/_4$ digits resolution. Here two overrange bits have been added and the full scale output code is 11 1001 1001 1001. When BCD coding is used for bipolar measurements another bit, a sign bit, is added to the code and result is sign-magnitude BCD coding.

Amplifiers and Filters

Operational and Instrumentation Amplifiers

The front end of a data acquisition system extracts the desired analog signal from a physical parameter by means of a transducer and then amplifies and filters it. An amplifier and filter are critical components in this initial signal processing.

The amplifier must perform one or more of the following functions: boost the signal amplitude, buffer the signal, convert a signal current into a voltage, or extract a differential signal from common mode noise.

To accomplish these functions requires a variety of different amplifier types. The most popular type of amplifier is an operational amplifier which is a general purpose gain block with differential inputs. The op amp may be connected in many different closed loop configurations, of which a few are shown in Figure 10. The gain and bandwidth of the circuits shown depend on the external resistors connected around the amplifier. An operational amplifier is a good choice in general where a single-ended signal is to be amplified, buffered, or converted from current to voltage.

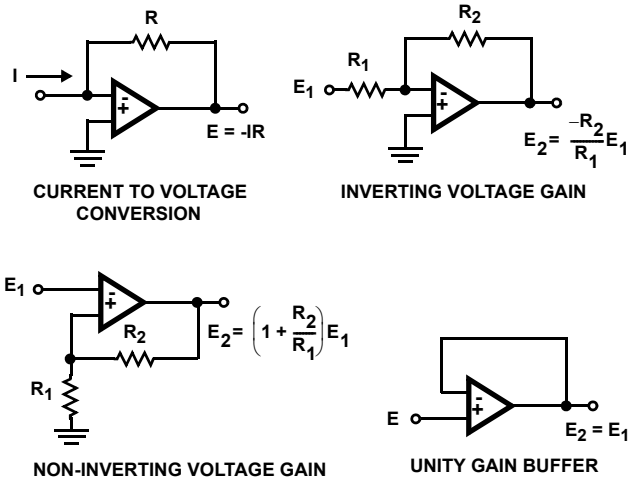


FIGURE 10. OPERATIONAL AMPLIFIER CONFIGURATIONS

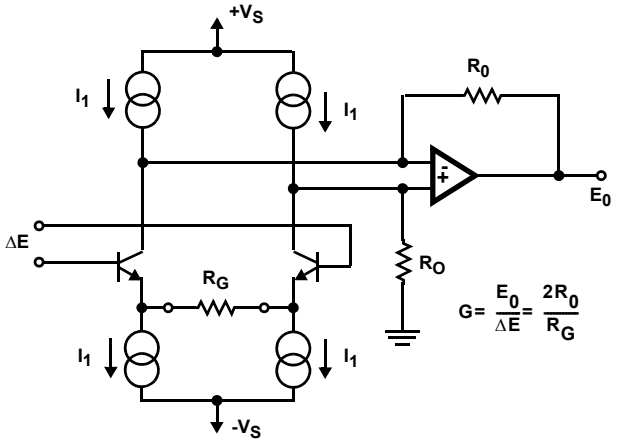


FIGURE 11. SIMPLIFIED INSTRUMENTATION AMPLIFIER CIRCUIT

In the case of differential signal processing, the instrumentation amplifier is a better choice since it maintains high impedance at both of its differential inputs and the gain is set by a resistor located elsewhere in the amplifier circuit. One type of instrumentation amplifier circuit is shown in Figure 11. Notice that no gain-setting resistors are connected to either of the input terminals. Instrumentation amplifiers have the following important characteristics.

1. High impedance differential inputs
2. Low input offset voltage drift
3. Low input bias currents
4. Gain easily set by means of one or two external resistors
5. High common-mode rejection ratio

Common Mode Rejection

Common-mode rejection ratio is an important parameter of differential amplifiers. An ideal differential input amplifier responds only to the voltage difference between its input terminals and does not respond at all to any voltage that is common to both input terminals (common-mode voltage). In nonideal amplifiers, however, the common-mode input signal

causes some output response even though small compared to the response to a differential input signal.

The ratio of differential and common-mode responses is defined as the common-mode rejection ratio. Common-mode rejection ratio of an amplifier is the ratio of differential voltage gain to common-mode voltage gain and is generally expressed in dB.

$$CMRR = 20\log_{10}\frac{A_D}{A_{CM}} \quad \text{(EQ. 12)}$$

where Ad is differential voltage gain and Acm is common-mode voltage gain. CMRR is a function of frequency and therefore also a function of the impedance balance between the two amplifier input terminals. At even moderate frequencies CMRR can be significantly degraded by small unbalances in the source series resistance and shunt capacitance.

Other Amplifier Types

There are several other special amplifiers which are useful in conditioning the input signal in a data acquisition system. An isolation amplifier is used to amplify a differential signal which is superimposed on a very high common-mode voltage, perhaps several hundred or even several thousand volts. The isolation amplifier has the characteristics of an instrumentation amplifier with a very high common-mode input voltage capability.

Another special amplifier, the chopper stabilized amplifier, is used to accurately amplify microvolt level signals to the required amplitude. This amplifier employs a special switching stabilizer which gives extremely low input offset voltage drift. Another useful device, the electrometer amplifier, has ultra-low input bias currents, generally less than 1pA and is used to convert extremely small signal currents into a high level voltage.

Filters

A low pass filter frequently follows the signal processing amplifier to reduce signal noise. Low pass filters are used for the following reasons: to reduce man-made electrical interference noise, to reduce electronic noise, and to limit the bandwidth of the analog signal to less than half the sampling frequency in order to eliminate frequency folding. When used for the last reason, the filter is called a pre-sampling filter or anti-aliasing filter.

Man-made electrical noise is generally periodic, as for example in power line interference, and is sometimes reduced by means of a special filter such as a notch filter. Electronic noise, on the other hand, is random noise with noise power proportional to bandwidth and is present in transducer resistances, circuit resistances, and in amplifiers themselves. It is reduced by limiting the bandwidth of the system to the minimum required to pass desired signal components.

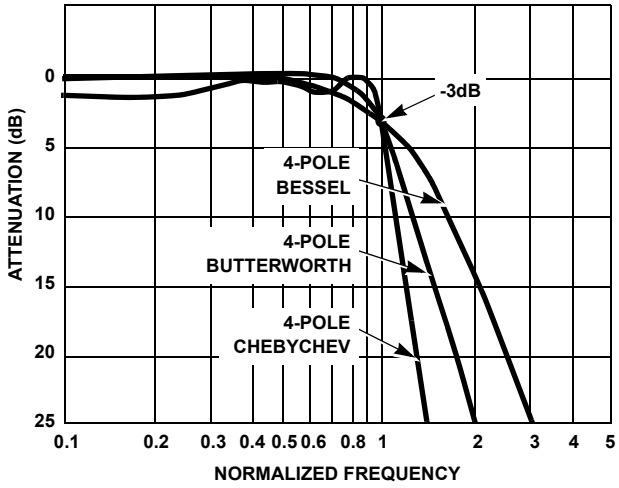


FIGURE 12. SOME PRACTICAL LOW PASS FILTER CHARACTERISTICS

No filter does a perfect job of eliminating noise or other undesirable frequency components, and therefore the choice of a filter is always a compromise. Ideal filters, frequently used an analysis examples, have flat passband response with infinite attenuation at the cutoff frequency, but are mathematical filters only and not physically realizable.

In practice, the systems engineer has a choice of cutoff frequency and attenuation rate. The attenuation rate and resultant phase response depend on the particular filter characteristic and the number of poles in the filter function. Some of the more popular filter characteristics include Butterworth, Chebychev, Bessel, and elliptic. In making this choice, the effect of overshoot and nonuniform phase delay must be carefully considered. Figure 12 illustrates some practical low pass filter response characteristics.

Passive RLC filters are seldom used in signal processing applications today due chiefly to the undesirable characteristics of inductors. Active filters are generally used now since they permit the filter characteristics to be accurately set by precision, stable resistors and capacitors. Inductors, with their undesirable saturation and temperature drift characteristics, are thereby eliminated. Also, because active filters use operational amplifiers, the problems of insertion loss and output loading are also eliminated.

Settling Time

Definition

A parameter that is specified frequently in data acquisition and distribution systems is settling time. The term settling time originates in control theory but is now commonly applied to amplifiers, multiplexers, and D/A converters.

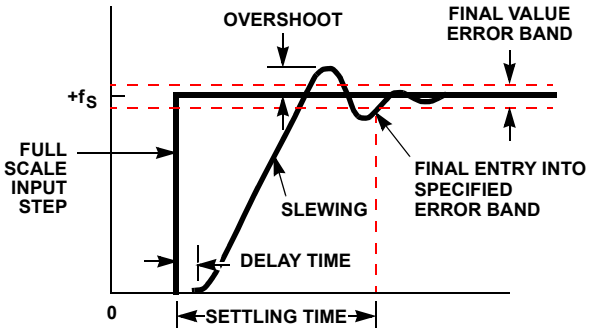


FIGURE 13. AMPLIFIER SETTLING TIME

Settling time is defined as the time elapsed from the application of a full scale step input to a circuit to the time when the output has entered and remained within a specified error band around its final value. The method of application of the input step may vary depending on the type of circuit, but the definition still holds. In the case of a D/A converter, for example, the step is applied by changing the digital input code whereas in the case of an amplifier the input signal itself is a step change.

The importance of settling time in a data acquisition system is that certain analog operations must be performed in sequence, and one operation may have to be accurately settled before the next operation can be initiated. Thus a buffer amplifier preceding an A/D converter must have accurately settled before the conversion can be initiated.

Settling time for an amplifier is illustrated in Figure 13. After application of a full scale step input there is a small delay time following which the amplifier output slews, or changes at its maximum rate. Slew rate is determined by internal amplifier currents which must charge internal capacitances.

As the amplifier output approaches final value, it may first overshoot and then reverse and undershoot this value before finally entering and remaining within the specified error band. Note that settling time is measured to the point at which the amplifier output enters and remains within the error band. This error band in most devices is specified to either ±0.1% or ±0.01% of the full scale transition.

Amplifier Characteristics

Settling time, unfortunately, is not readily predictable from other amplifier parameters such as bandwidth, slew rate, or overload recovery time, although it depends on all of these. It is also dependent on the shape of the amplifier open loop gain characteristics, its input and output capacitance, and the dielectric absorption of any internal capacitances. An amplifier must be specifically designed for optimized settling time, and settling time is a parameter that must be determined by testing.

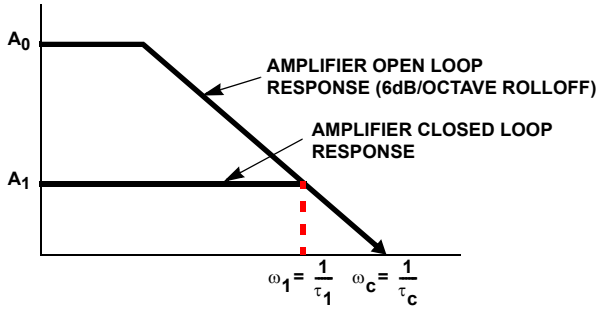


FIGURE 14. AMPLIFIER SINGLE-POLE OPEN LOOP GAIN CHARACTERISTIC

One of the important requirements of a fast settling amplifier is that it have a single-pole open loop gain characteristic, i.e., one that has a smooth 6dB per octave gain roll-off characteristic to beyond the unity gain crossover frequency. Such a desirable characteristic is shown in Figure 14.

It is important to note that an amplifier with a single-pole response can never settle faster than the time indicated by the number of closed loop time constants to the given accuracy. Figure 15 shows output error as a function of the number of time constants τ where

$$\tau = \frac{1}{\omega} = \frac{1}{2\pi f} \qquad \text{(EQ. 13)}$$

and f is the closed loop 3dB bandwidth of the amplifier.

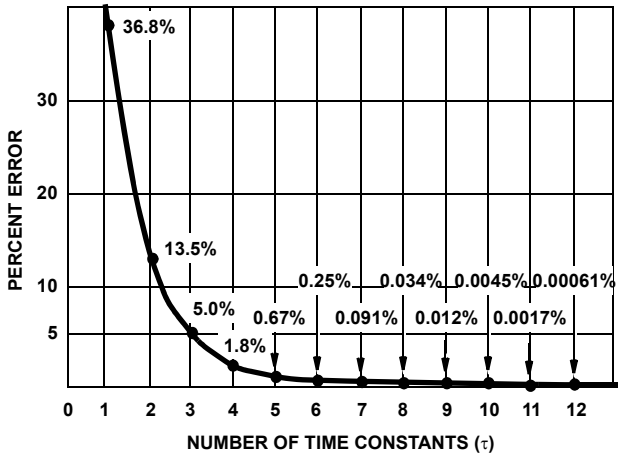


FIGURE 15. OUTPUT SETTLING ERROR AS A FUNCTION OF NUMBER OF TIME CONSTANTS

Actual settling time for a good quality amplifier may be significantly longer than that indicated by the number of closed loop time constants due to slew rate limitation and overload recovery time. For example, an amplifier with a closed loop bandwidth of 1MHz has a time constant of 160ns which indicates a settling time of 1.44µs (9 time constants) to 0.01% of final value. If the slew rate of this amplifier is 1V/µs, it will take more than 10µs to settle to 0.01% for a 10V change.

If the amplifier has a nonuniform gain roll-off characteristic, then its settling time may have one of two undesirable qualities. First, the output may reach the vicinity of the error band quickly but then take a long time to actually enter it; second, it may overshoot the error band and then oscillate back and forth through it before finally entering and remaining inside it.

Modern fast settling operational amplifiers come in many different types including modular, hybrid, and monolithic amplifiers. Such amplifiers have settling times to 0.1% or 0.01% of 2μs down to 100ns and are useful in many data acquisition and conversion applications.

Digital-to-Analog Converters

Introduction

Digital-to-analog converters are the devices by which computers communicate with the outside world. They are employed in a variety of applications from CRT display systems and voice synthesizers to automatic test systems, digitally controlled attenuators, and process control actuators. In addition, they are key components inside most A/D converters. D/A converters are also referred to as DACs and are termed decoders by communications engineers.

The transfer function of an ideal 3-bit D/A converter is shown in Figure 16. Each input code word produces a single, discrete analog output value, generally a voltage. Over the output range of the converter 2^n different values are produced including zero; and the output has a one-to-one correspondence with input, which is not true for A/D converters.

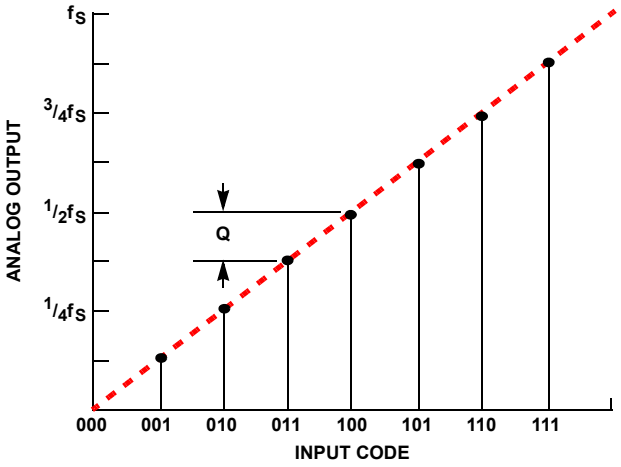


FIGURE 16. TRANSFER FUNCTION OF IDEAL 3-BIT D/A CONVERTER

There are many different circuit techniques used to implement D/A converters, but a few popular ones are widely used today. Virtually all D/A converters in use are of the parallel type where all bits change simultaneously upon application of an input code word; serial type D/A converters, on the other hand, produce an analog output only after receiving all digital input data in sequential form.

Weighted Current Source D/A Converter

The most popular D/A converter design in use today is the weighted current source circuit illustrated in Figure 17. An array of switched transistor current sources is used with binary weighted currents. The binary weighting is achieved by using emitter resistors with binary related values of R, 2R, 4R, 8R, ...2^nR. The resulting collector currents are then added together at the current summing line.

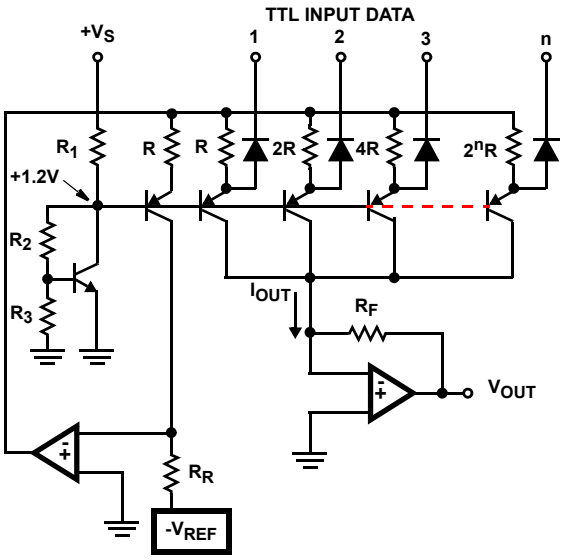


FIGURE 17. WEIGHTED CURRENT SOURCE D/A CONVERTER

The current sources are switched on or off from standard TTL inputs by means of the control diodes connected to each emitter. When the TTL input is high the current source is on; when the input is low it is off, with the current flowing through the control diode. Fast switching speed is achieved because there is direct control of the transistor current, and the current sources never go into saturation.

To interface with standard TTL levels, the current sources are biased to a base voltage of +1.2V. The emitter currents are regulated to constant values by means of the control amplifier and a precision voltage reference circuit together with a bipolar transistor.

The summed output currents from all current sources that are on go to an operational amplifier summing junction; the amplifier converts this output current into an output voltage. In some D/A converters the output current is used to directly drive a resistor load for maximum speed, but the positive output voltage in this case is limited to about +1V.

The weighted current source design has the advantages of simplicity and high speed. Both PNP and NPN transistor current sources can be used with this technique although the TTL interfacing is more difficult with NPN sources. This technique is used in most monolithic, hybrid, and modular D/A converters in use today.

A difficulty in implementing higher resolution D/A converters designs is that a wide range of emitter resistors are required, and very high value resistors cause problems with both temperature stability and switching speed. To overcome these problems, weighted current sources are used in identical groups, with the output of each group divided down by a resistor divider as shown in Figure 18.

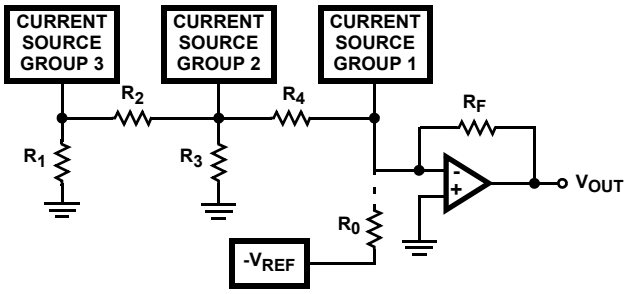


FIGURE 18. CURRENT DIVIDING THE OUTPUTS OF WEIGHTED CURRENT SOURCE GROUPS

The resistor network, R_1 through R_4, divides the output of Group 3 down by a factor of 256 and the output of Group 2 down by a factor of 16 with respect to the output of Group 1. Each group is identical, with four current sources of the type shown in Figure 17, having binary current weights of 1, 2, 4, 8. Figure 18 also illustrates the method of achieving a bipolar output by deriving an offset current from the reference circuit which is then subtracted from the output current line through resistor R_0. This current is set to exactly one half the full scale output current.

R-2R D/A Converter

A second popular technique for D/A conversion is the R-2R ladder method. As shown in Figure 19, the network consists of series resistors of value R and shunt resistors of value 2R. The bottom of each shunt resistor has a single-pole double-throw electronic switch which connects the resistor to either ground or the output current summing line.

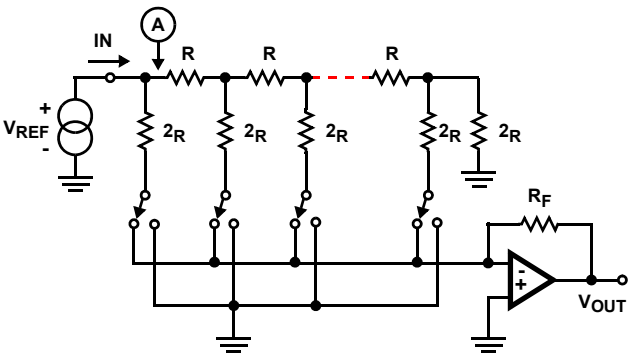


FIGURE 19. R-2R LADDER D/A CONVERTER

The operation of the R-2R ladder network is based on the binary division of current as it flows down the ladder. Examination of the ladder configuration reveals that at point A looking to the right, one measures a resistance of 2R; therefore the reference input to the ladder has a resistance of R. At the reference input the current splits into two equal parts since it sees equal resistances in either direction. Likewise, the current flowing down the ladder to the right continues to divide into two equal parts at each resistor junction.

The result is binary weighted currents flowing down each shunt resistor in the ladder. The digitally controlled switches direct the currents to either the summing line or ground. Assuming all bits are on as shown in the diagram, the output current is

$$I_{OUT} = \frac{V_{REF}}{R}\left[1/2 + 1/4 + 1/8 \ldots \frac{1}{2^n}\right] \quad \text{(EQ. 14)}$$

which is a binary series. The sum of all currents is then

$$I_{OUT} = \frac{V_{REF}}{R}(1 - 2^{-n}) \quad \text{(EQ. 15)}$$

where the 2^n term physically represents the portion of the input current flowing through the 2R terminating resistor to ground at the far right.

As in the previous circuit, the output current summing line goes to an operational amplifier which converts current to voltage.

The advantage of the R-2R ladder technique is that only two values of resistors are required, with the resultant ease of matching or trimming and excellent temperature tracking. In addition, for high speed applications relatively low resistor values can be used. Excellent results can be obtained for high resolution D/A converters by using laser-trimmed thin film resistor networks.

Multiplying and Deglitched D/A Converters

The R-2R ladder method is specifically used for multiplying type D/A converters. With these converters, the reference voltage can be varied over the full range of $\pm V_{MAX}$ with the output the product of the reference voltage and the digital input word. Multiplication can be performed in 1, 2, or 4 algebraic quadrants.

If the reference voltage is unipolar, the circuit is a one-quadrant multiplying DAC; if it is bipolar, the circuit is a two-quadrant multiplying DAC. For four-quadrant operation the two current summing lines shown in Figure 19 must be subtracted from each other by operational amplifiers.

In multiplying D/A converters, the electronic switches are usually implemented with CMOS devices. Multiplying DACs are commonly used in automatic gain controls, CRT character generation, complex function generators, digital attenuators, and divider circuits.

Another important D/A converter design takes advantage of the best features of both the weighted current source technique and the R-2R ladder technique. This circuit, shown in Figure 20, uses equal value switched current sources to drive the junctions of the R-2R ladder network. The advantage of the equal value current sources is obvious since all emitter resistors are identical and switching speeds are also identical.

This technique is used in many ultra-high speed D/A converters.

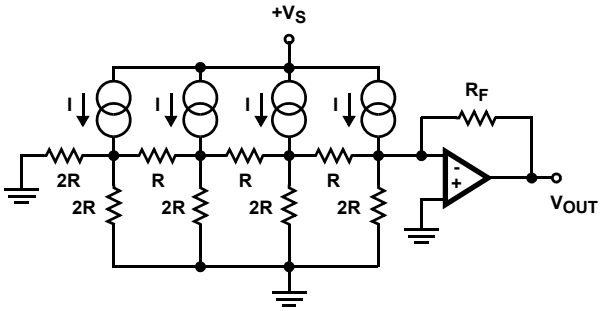


FIGURE 20. D/A CONVERTER EMPLOYING R-2R LADDER WITH EQUAL VALUE SWITCHED CURRENT SOURCES

One other specialized type D/A converter used primarily in CRT display systems is the deglitched D/A converter. All D/A converters produce output spikes, or glitches, which are most serious at the major output transitions of $^1/_4f_S$, $^1/_2f_S$, and $^3/_4f_S$ as illustrated in Figure 21A.

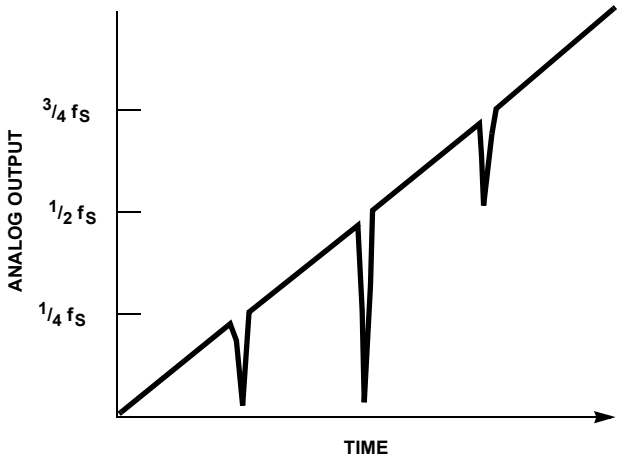


FIGURE 21A. OUTPUT GLITCHES

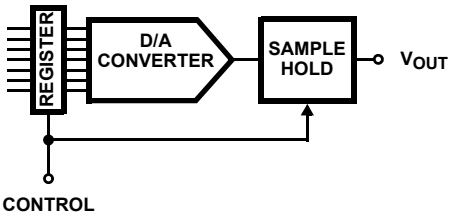


FIGURE 21B. DEGLITCHED D/A CONVERTER

Glitches are caused by small time differences between some current sources turning off and others turning on. Take, for example, the major code transition at half scale from 0111 ...1111 to 1000...0000. Here the MSB current source turns on while all other current sources turn off. The small differences in switching times results in a narrow half scale glitch. Such a glitch produces distorted characters on CRT displays.

Glitches can be virtually eliminated by the circuit shown in Figure 21B. The digital input to a D/A converter is controlled by an input register while the converter output goes to a specially designed sample-hold circuit. When the digital input is updated by the register, the sample-hold is switched into the hold mode. After the D/A has changed to its new output value and all glitches have settled out, the sample-hold is then switched back into the tracking mode. When this happens, the output changes smoothly from its previous value to the new value with no glitches present.

Voltage Reference Circuits

An important circuit required in both A/D and D/A converters is the voltage reference. The accuracy and stability of a data converter ultimately depends upon the reference; it must therefore produce a constant output voltage over both time and temperature.

The compensated Zener reference diode with a buffer-stabilizer circuit is commonly used in most data converters today. Although the compensated Zener may be one of several types, the compensated subsurface, or buried, Zener is probably the best choice. These new devices produce an avalanche breakdown which occurs beneath the surface of the silicon, resulting in better long-term stability and noise characteristics than with earlier surface breakdown Zeners.

These reference devices have reverse breakdown voltages of about 6.4V and consist of a forward biased diode in series with the reversed biased Zener. Because the diodes have approximately equal and opposite voltage changes with temperature, the result is a temperature stable voltage. Available devices have temperature coefficients from 100ppm/^{o}C to less than 1ppm/^{o}C.

Some of the new IC voltage references incorporate active circuitry to buffer the device and reduce its dynamic impedance; in addition, some contain temperature regulation circuitry on the chip to achieve ultra-low tempcos.

A popular buffered reference circuit is shown in Figure 22; this circuit produces an output voltage higher than the reference voltage. It also generates a constant, regulated current through the reference which is determined by the three resistors.

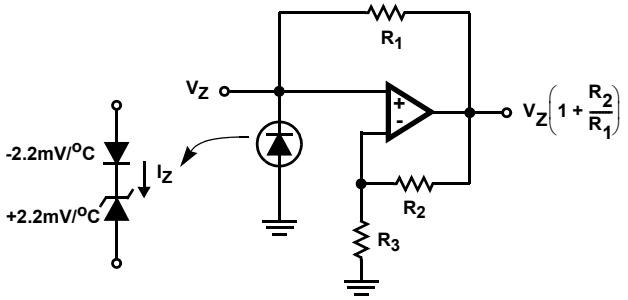


FIGURE 22. A PRECISION, BUFFERED VOLTAGE REFERENCE CIRCUIT

Some monolithic A/D and D/A converters use another type of reference device known as the bandgap reference. This circuit is based on the principle of using the known, predictable base-to-emitter voltage of a transistor to generate a constant voltage equal to the extrapolated bandgap voltage of silicon. This reference gives excellent results for the lower reference voltages of 1.2 or 2.5V.

Analog-to-Digital Converters

Counter Type A/D Converter

Analog-to-digital converters, also called ADCs or encoders, employ a variety of different circuit techniques to implement the conversion function. As with D/A converters, however, relatively few of these circuits are widely used today. Of the various techniques available, the choice depends on the resolution and speed required.

One of the simplest A/D converters is the counter, or servo, type. This circuit employs a digital counter to control the input of a D/A converter. Clock pulses are applied to the counter and the output of the D/A is stepped up one LSB at a time. A comparator compares the D/A output with the analog input and stops the clock pulses when they are equal. The counter output is then the converted digital word.

While this converter is simple, it is also relatively slow. An improvement on this technique is shown in Figure 23 and is known as a tracking A/D converter, a device commonly used in control systems. Here an up-down counter controls the DAC, and the clock pulses are directed to the pertinent counter input depending on whether the D/A output must increase or decrease to reach the analog input voltage.

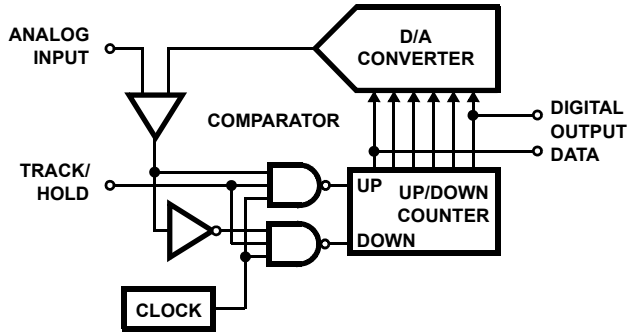


FIGURE 23. TRACKING TYPE A/D CONVERTER

The obvious advantage of the tracking A/D converter is that it can continuously follow the input signal and give updated digital output data if the signal does not change too rapidly. Also, for small input changes, the conversion can be quite fast. The converter can be operated in either the track or hold modes by a digital input control.

Successive-Approximation A/D Converters

By far, the most popular A/D conversion technique in general use for moderate to high speed applications is the successive-approximation type A/D. This method falls into a class of techniques known as feedback type A/D converters, to which the counter type also belongs. In both cases a D/A converter is in the feedback loop of a digital control circuit which changes its output until it equals the analog input. In the case of the successive-approximation converter, the DAC is controlled in an optimum manner to complete a conversion in just n-steps, where n is the resolution of the converter in bits.

The operation of this converter is analogous to weighing an unknown on a laboratory balance scale using standard weights in a binary sequence such as 1, $1/_2$, $1/_4$, $1/_8$ ...1/n kilograms. The correct procedure is to begin with the largest standard weight and proceed in order down to the smallest one.

The largest weight is placed on the balance pan first; if it does not tip, the weight is left on and the next largest weight is added. If the balance does tip, the weight is removed and the next one added. The same procedure is used for the next largest weight and so on down to the smallest. After the nth standard weight has been tried and a decision made, the weighing is finished. The total of the standard weights remaining on the balance is the closest possible approximation to the unknown.

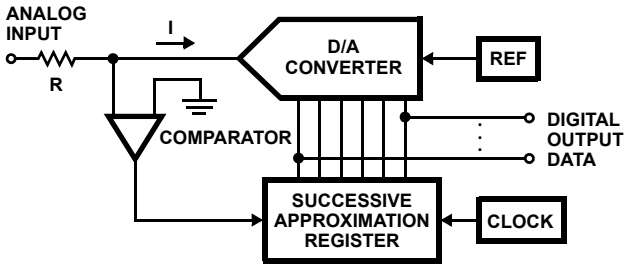


FIGURE 24. SUCCESSIVE APPROXIMATION A/D CONVERTER

In the successive-approximation A/D converter illustrated in Figure 24, a successive-approximation register (SAR) controls the D/A converter by implementing the weighing logic just described. The SAR first turns on the MSB of the DAC and the comparator tests this output against the analog input. A decision is made by the comparator to leave the bit on or turn it off after which bit 2 is turned on and a second comparison made. After n-comparisons the digital output of the SAR indicates all those bits which remain on and produces the desired digital code. The clock circuit controls the timing of the SAR. Figure 25 shows the D/A converter output during a typical conversion.

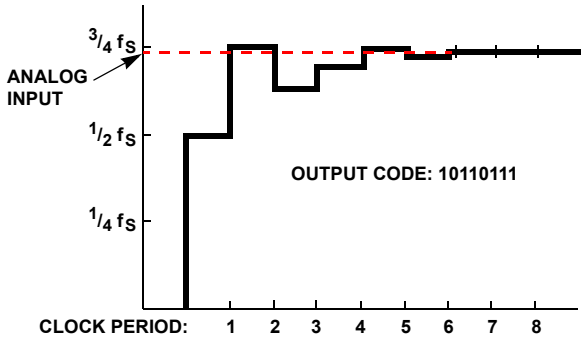


FIGURE 25. D/A OUTPUT FOR 8-BIT SUCCESSIVE APPROXIMATION CONVERSION

The conversion efficiency of this technique means that high resolution conversions can be made in very short times. For example, it is possible to perform a 10-bit conversion in 1µs or less and a 12-bit conversion in 2µs or less. Of course the speed of the internal circuitry, in particular the D/A and comparator, are critical for high speed performance.

The Parallel (Flash) A/D Converter

For ultra-fast conversions required in video signal processing and radar applications where up to 8-bits resolution is required, a different technique is employed; it is known as the parallel (also flash, or simultaneous) method and is illustrated in Figure 26.

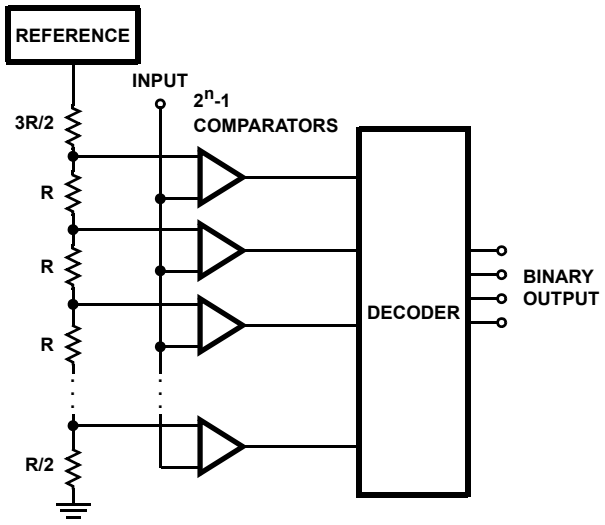


FIGURE 26. 4-BIT PARALLEL A/D CONVERTER

This circuit employs 2^n-1 analog comparators to directly implement the quantizer transfer function of an A/D converter.

The comparator trip-points are spaced 1 LSB apart by the series resistor chain and voltage reference. For a given analog input voltage all comparators biased below the voltage turn on and all those biased above it remain off. Since all comparators change state simultaneously, the quantization process is a one-step operation.

A second step is required, however, since the logic output of the comparators is not in binary form.

Therefore an ultra-fast decoder circuit is employed to make the logic conversion to binary. The parallel technique reaches the ultimate in high speed because only two sequential operations are required to make the conversion.

The limitation of the method, however, is in the large number of comparators required for even moderate resolutions. A 4-bit converter, for example, requires only 15 comparators, but an 8-bit converter needs 255. For this reason it is common practice to implement an 8-bit A/D with two 4-bit stages as shown in Figure 27.

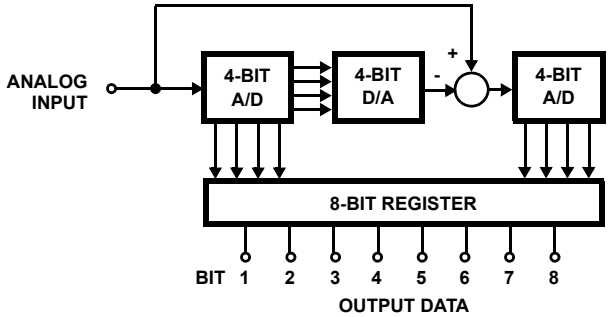


FIGURE 27. TWO-STAGE PARALLEL 8-BIT A/D CONVERTER

The result of the first 4-bit conversion is converted back to analog by means of an ultra-fast 4-bit D/A and then subtracted from the analog input. The resulting residue is then converted by the second 4-bit A/D, and the two sets of data are accumulated in the 8-bit output register.

Converters of this type achieve 8-bit conversions at rates of 20MHz and higher, while single stage 4-bit conversions can reach 50 to 100MHz rates.

Integrating Type A/D Converters

Indirect A/D Conversion

Another class of A/D converters known as integrating type operates by an indirect conversion method. The unknown input voltage is converted into a time period which is then measured by a clock and counter. A number of variations exist on the basic principle such as single-slope, dual-slope, and triple-slope methods. In addition there is another technique - completely different - which is known as the charge-balancing or quantized feedback method.

The most popular of these methods are dual-slope and charge-balancing; although both are slow, they have excellent linearity characteristics with the capability of rejecting input noise. Because of these characteristics, integrating type A/D converters are almost exclusively used in digital panel meters, digital multimeters, and other slow measurement applications.

Dual-Slope A/D Conversion

The dual-slope technique, shown in Figure 28, is perhaps best known. Conversion begins when the unknown input voltage is switched to the integrator input; at the same time the counter begins to count clock pulses and counts up to overflow. At this point the control circuit switches the integrator to the negative reference voltage which is integrated until the output is back to zero. Clock pulses are counted during this time until the comparator detects the zero crossing and turns them off.

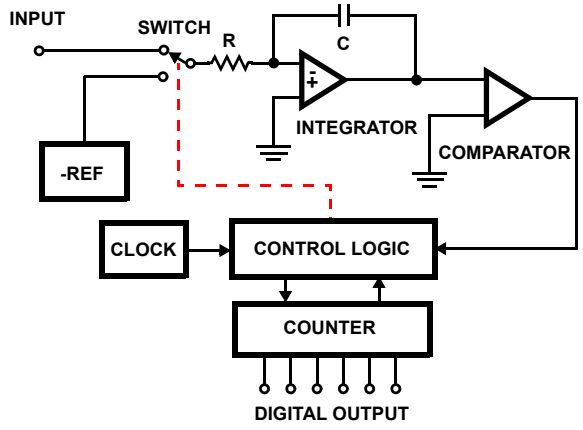


FIGURE 28. DUAL SLOPE A/D CONVERTER

The counter output is then the converted digital word. Figure 29 shows the integrator output waveform where T_1 is a fixed time and T_2 is a time proportional to the input voltage. The times are related as follows:

$$T_2 = T_1 \frac{E_{IN}}{V_{REF}} \quad \text{(EQ. 16)}$$

The digital output word therefore represents the ratio of the input voltage to the reference.

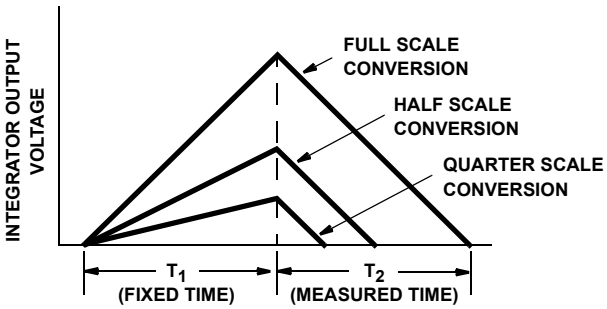


FIGURE 29. INTEGRATOR OUTPUT WAVEFORM FOR DUAL SLOPE A/D CONVERTER

Dual-slope conversion has several important features. First, conversion accuracy is independent of the stability of the clock and integrating capacitor so long as they are constant during the conversion period. Accuracy depends only on the reference accuracy and the integrator circuit linearity. Second, the noise rejection of the converter can be infinite if T_1 is set to equal the period of the noise. To reject 60Hz power noise therefore requires that T_1 be 16.667ms.

Charge-Balancing A/D Conversion

The charge-balancing, or quantized feedback, method of conversion is based on the principle of generating a pulse train with frequency proportional to the input voltage and then counting the pulses for a fixed period of time. This circuit is shown in Figure 30. Except for the counter and timer, the circuit is a voltage-to-frequency (V/F) converter which generates an output pulse rate proportional to input voltage.

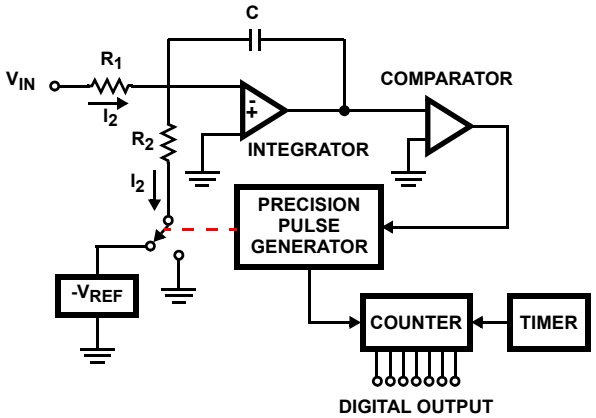


FIGURE 30. CHARGE-BALANCING A/D CONVERTER

The circuit operates as follows. A positive input voltage causes a current to flow into the operational integrator through R_1. This current is integrated, producing a negative going ramp at the output. Each time the ramp crosses zero the comparator output triggers a precision pulse generator which puts out a constant width pulse.

The pulse output controls switch S_1 which connects R_2 to the negative reference for the duration of the pulse. During this time a pulse of current flows out of the integrator summing junction, producing a fast, positive ramp at the integrator output. This process is repeated, generating a train of current pulses which exactly balances the input current - hence the name charge balancing. This balance has the following relationship:

$$f = \frac{1}{\tau}\frac{V_{IN}}{V_{REF}}\frac{R_2}{R_1} \quad \text{(EQ. 17)}$$

where τ is the pulse width and f the frequency.

A higher input voltage therefore causes the integrator to ramp up and down faster, producing higher frequency output pulses. The timer circuit sets a fixed time period for counting. Like the dual-slope converter, the circuit also integrates input noise, and if the timer is synchronized with the noise frequency, infinite rejection results. Figure 31 shows the noise rejection characteristic of all integrating type A/D converters with rejection plotted against the ratio of integration period to noise period.

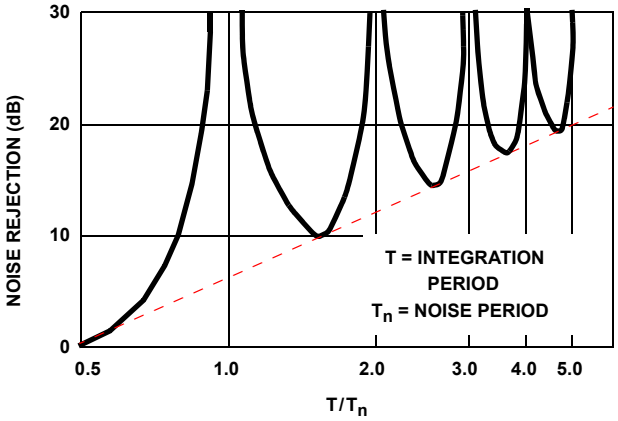


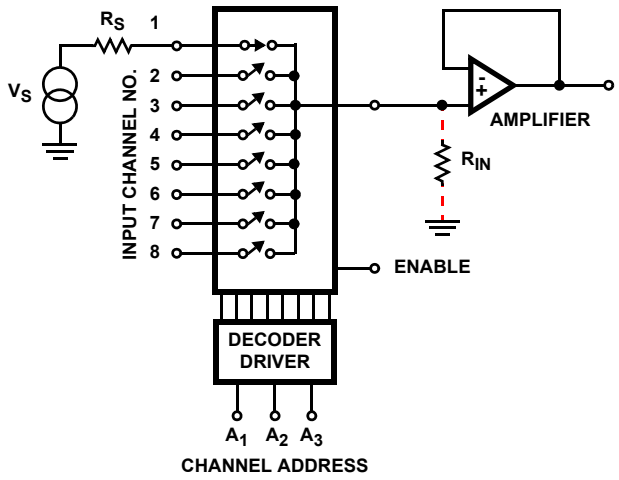
FIGURE 31. NOISE REJECTION FOR INTEGRATING TYPE A/D CONVERTERS

Analog Multiplexers

Analog Multiplexer Operation

Analog multiplexers are the circuits that time-share an A/D converter among a number of different analog channels. Since the A/D converter in many cases is the most expensive component in a data acquisition system, multiplexing analog inputs to the A/D is an economical approach. Usually the analog multiplexer operates into a sample-hold circuit which holds the required analog voltage long enough for A/D conversion.

As shown in Figure 32, an analog multiplexer consists of an array of parallel electronic switches connected to a common output line. Only one switch is turned on at a time. Popular switch configurations include 4, 8, and 16 channels which are connected in single (single-ended) or dual (differential) configurations.



A_1	A_2	A_3	EN	ON-CHAN
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

FIGURE 32. ANALOG MULTIPLEXER CIRCUIT

The multiplexer also contains a decoder-driver circuit which decodes a binary input word and turns on the appropriate switch. This circuit interfaces with standard TTL inputs and drives the multiplexer switches with the proper control voltages. For the 8-channel analog multiplexer shown, a one-of-eight decoder circuit is used.

Most analog multiplexers today employ the CMOS switch circuit shown in Figure 33. A CMOS driver controls the gates of parallel-connected P-Channel and N-Channel MOSFETs. Both switches turn on together with the parallel connection giving relativity uniform on-resistance over the required analog input voltage range. The resulting on-resistance may vary from about 50Ω to 2kΩ depending on the multiplexer; this resistance increases with temperature.

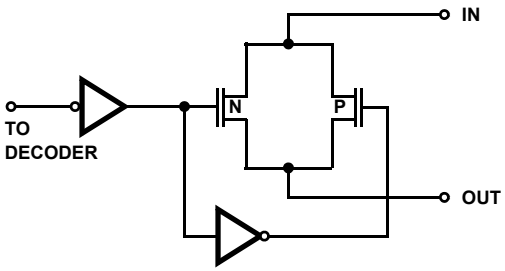


FIGURE 33. CMOS ANALOG SWITCH CIRCUIT

Analog Multiplexer Characteristics

Because of the series resistance, it is common practice to operate an analog multiplexer into a very high load resistance such as the input of a unity gain buffer amplifier shown in the diagram. The load impedance must be large compared with the switch on-resistance and any series source resistance in order to maintain high transfer accuracy. Transfer error is the input to output error of the multiplexer with the source and load connected; error is expressed as a percent of input voltage.

Transfer errors of 0.1% to 0.01% or less are required in most data acquisition systems. This is readily achieved by using operational amplifier buffers with typical input impedances from 10^8 to $10^{12}\Omega$. Many sample-hold circuits also have very high input impedances.

Another important characteristic of analog multiplexers is break-before-make switching. There is a small time delay between disconnection from the previous channel and connection to the next channel which assures that two adjacent input channels are never instantaneously connected together.

Settling time is another important specification for analog multiplexers; it is the same definition previously given for amplifiers except that it is measured from the time the channel is switched on. Throughput rate is the highest rate at which a multiplexer can switch from channel to channel with the output settling to its specified accuracy. Crosstalk is the ratio of output voltage to input voltage with all channels connected in parallel and off; it is generally expressed as an input to output attenuation ratio in dB.

As shown in the representative equivalent circuit of Figure 34, analog multiplexer switches have a number of leakage currents and capacitances associated with their operation. These parameters are specified on data sheets and must be considered in the operation of the devices. Leakage currents, generally in picoamperes at room temperature, become troublesome only at high temperatures. Capacitances affect crosstalk and settling time of the multiplexer.

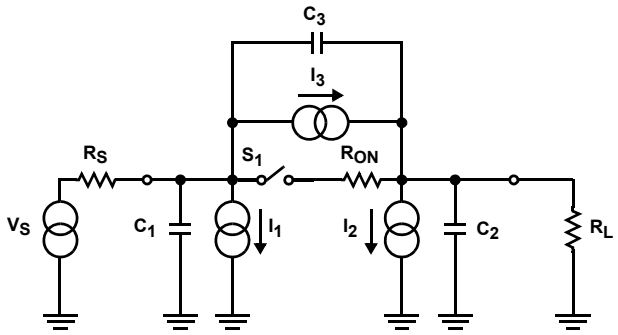


FIGURE 34. EQUIVALENT CIRCUIT OF ANALOG MULTIPLEXER SWITCH

Analog Multiplexer Applications

Analog multiplexers are employed in two basic types of operation: high-level and low-level. In high-level multiplexing; the most popular type, the analog signal is amplified to the 1V to 10V range ahead of the multiplexer. This has the advantage of reducing the effects of noise on the signal during the remaining analog processing. In low-level multiplexing the signal is amplified after multiplexing, therefore great care must be exercised in handling the low-level signal up to the multiplexer. Low-level multiplexers generally use two-wire differential switches in order to minimize noise pick-up. Reed relays, because of essentially zero series resistance and absence of switching spikes, are frequently employed in low-level multiplexing systems. They are also useful for high common-mode voltages.

A useful specialized analog multiplexer is the flying-capacitor type. This circuit, shown as a single channel in Figure 35 has differential inputs and is particularly useful with high common-mode voltages. The capacitor connects first to the differential analog input, charging up to the input voltage, and is then switched to the differential output which goes to a high input impedance instrumentation amplifier. The differential signal is therefore transferred to the amplifier input without the common mode voltage and is then further processed up to A/D conversion.

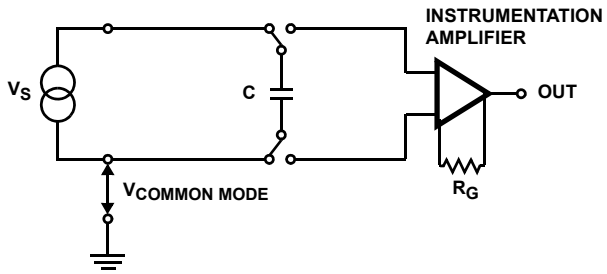


FIGURE 35. FLYING CAPACITOR MULTIPLEXER SWITCH

In order to realize large numbers of multiplexed channels, you can connect analog multiplexers in parallel using the enable input to control each device. This is called single-level multiplexing. You can also connect the output of several

multiplexers to the inputs of another to expand the number of channels; this method is double-level multiplexing.

Sample-Hold Circuits

Operation of Sample-Holds

Sample-hold circuits, discussed earlier, are the devices which store analog information and reduce the aperture time of an A/D converter. A sample-hold is simply a voltage-memory device in which an input voltage is acquired and then stored on a high quality capacitor. A popular circuit is shown in Figure 36.

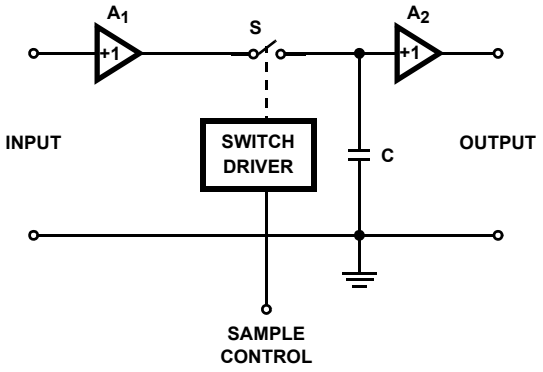


FIGURE 36. POPULAR SAMPLE-HOLD CIRCUIT

A_1 is an input buffer amplifier with a high input impedance so that the source, which may be an analog multiplexer, is not loaded. The output of A_1 must be capable of driving the hold capacitor with stability and enough drive current to charge it rapidly. S_1 is an electronic switch, generally an FET, which is rapidly switched on or off by a driver circuit which interfaces with TTL inputs.

C is a capacitor with low leakage and low dielectric absorption characteristics; it is a polystyrene, polycarbonate, polypropylene, or Teflon™ type. In the case of hybrid sample-holds, the MOS type capacitor is frequently used.

A_2 is the output amplifier which buffers the voltage on the hold capacitor. It must therefore have extremely low input bias current, and for this reason an FET input amplifier is required.

There are two modes of operation for a sample-hold: sample (or tracking) mode, when the switch is closed; and hold mode, when the switch is open. Sample-holds are usually operated in one of two basic ways. The device can continuously track the input signal and be switched into the hold mode only at certain specified times, spending most of the time in tracking mode. This is the case for a sample-hold employed as a deglitcher at the output of a D/A converter, for example.

Alternatively, the device can stay in the hold mode most of the time and go to the sample mode just to acquire a new input signal level. This is the case for a sample-hold used in a data acquisition system following the multiplexer.

The Sample-Hold as a Data Recovery Filter

A common application for sample-hold circuits is data recovery, or signal reconstruction, filters. The problem is to reconstruct a train of analog samples into the original signal; when used as a recovery filter, the sample-hold is known as a zero-order hold. It is a useful filter because it fills in the space between samples, providing data smoothing.

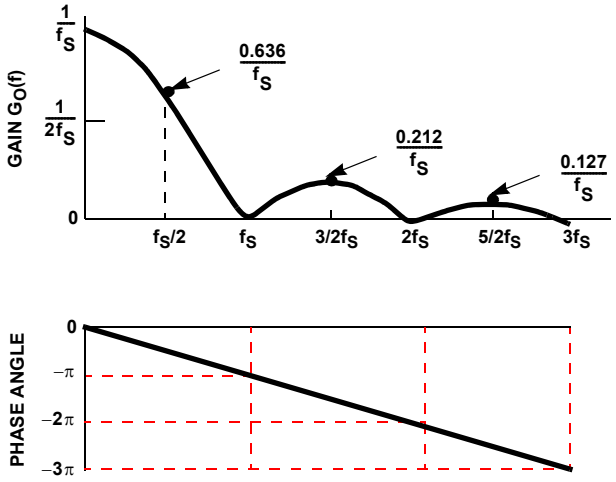


FIGURE 37. GAIN AND PHASE COMPONENTS OF ZERO-ORDER HOLD TRANSFER FUNCTION

As with other filter circuits, the gain and phase components of the transfer function are of interest. By an analysis based on the impulse response of a sample-hold and use of the Laplace transform, the transfer function is found to be

$$G_0(f) = \frac{1}{f_S}\left[\frac{\sin\pi\left(\frac{f}{f_S}\right)}{\pi\left(\frac{f}{f_S}\right)}\right]\varepsilon - j\pi f/f_S \qquad \text{(EQ. 18)}$$

where f_S is the sampling frequency. This function contains the familiar (sin x)/x term plus a phase term, both of which are plotted in Figure 37.

The sample-hold is therefore a low pass filter with a cutoff frequency slightly less than $f_S/2$ and a linear phase response which results in a constant delay time of T/2, where T is the time between samples. Notice that the gain function also has significant response lobes beyond f_S. For this reason a sample-hold reconstruction filter is frequently followed by another conventional low pass filter.

Other Sample-Hold Circuits

In addition to the basic circuit of Figure 36, there are several other sample-hold circuit configurations which are frequently used. Figure 38 shows two such circuits which are closed loop circuits as contrasted with the open loop circuit of Figure 36. Figure 38A uses an operational integrator and another amplifier to make a fast, accurate inverting sample-hold. A buffer amplifier is sometimes added in front of this circuit to

give high input impedance. Figure 38B shows a high input impedance non-inverting sample-hold circuit.

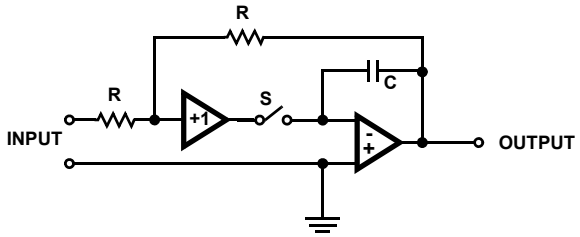


FIGURE 38A. CLOSED LOOP SAMPLE-HOLD CIRCUIT

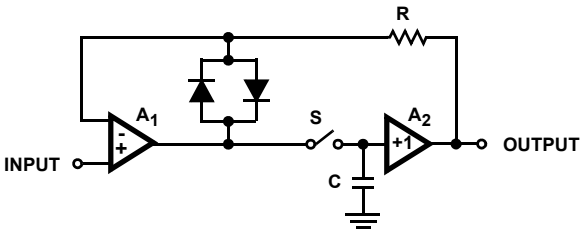


FIGURE 38B. CLOSED LOOP SAMPLE-HOLD CIRCUIT

The circuit in Figure 36, although generally not as accurate as those in Figure 38, can be used with a diode-bridge switch to realize ultra-fast acquisition sample-holds.

Sample-Hold Characteristics

A number of parameters are important in characterizing sample-hold performance. Probably most important of these is acquisition time. The definition is similar to that of settling time for an amplifier. It is the time required, after the sample-command is given, for the hold capacitor to charge to a full-scale voltage change and remain within a specified error band around final value.

Several hold-mode specifications are also important. Hold-mode droop is the output voltage change per unit time when the sample switch is open. This droop is caused by the leakage currents of the capacitor and switch, and the output amplifier bias current. Hold-mode feedthrough is the percentage of input signal transferred to the output when the sample switch is open. It is measured with a sinusoidal input signal and caused by capacitive coupling.

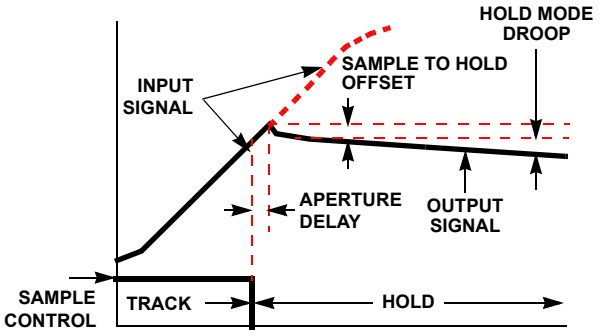


FIGURE 39. SOME SAMPLE-HOLD CHARACTERISTICS

The most critical phase of sample-hold operation is the transition from the sample mode to the hold mode. Several important parameters characterize this transition. Sample-to-hold offset (or step) error is the change in output voltage from the sample mode to the hold mode, with a constant input voltage. It is caused by the switch transferring charge onto the hold capacitor as it turns off.

Aperture delay is the time elapsed from the hold command to when the switch actually opens; it is generally much less than a microsecond. Aperture uncertainty (or aperture jitter) is the time variation, from sample to sample, of the aperture delay. It is the limit on how precise is the point in time of opening the switch. Aperture uncertainty is the time used to determine the aperture error due to rate of change of the input signal. Several of the above specifications are illustrated in the diagram of Figure 39.

Sample-hold circuits are simple in concept, but generally difficult to fully understand and apply. Their operation is full of subtleties, and they must therefore be carefully selected and then tested in a given application.

Specification of Data Converters

Ideal vs Real Data Converters

Real A/D and D/A converters do not have the ideal transfer functions discussed earlier. There are three basic departures from the ideal: offset, gain, and linearity errors. These errors are all present at the same time in a converter; in addition they change with both time and temperature.

Figure 40 shows A/D converter transfer functions which illustrate the three error types. Figure 40A shows offset error, the analog error by which the transfer function fails to pass through zero. Next, in Figure 40B is gain error, also called scale factor error; it is the difference in slope between the actual transfer function and the ideal, expressed as a percent of analog magnitude.

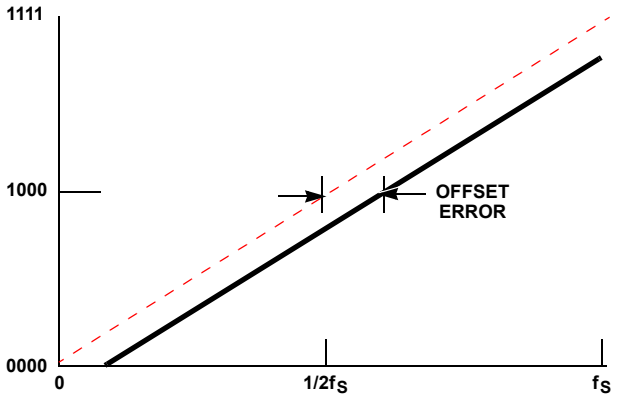


FIGURE 40A. OFFSET ERRORS FOR AN A/D CONVERTER

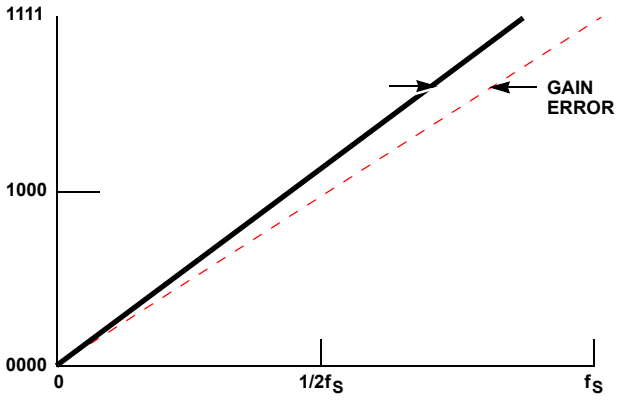


FIGURE 40B. GAIN ERRORS FOR AN A/D CONVERTER

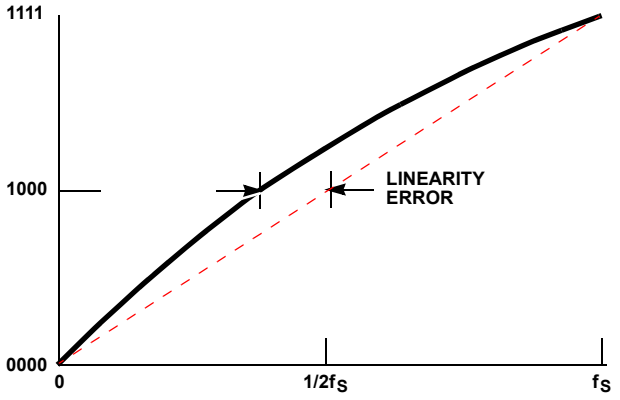


FIGURE 40C. LINEARITY ERRORS FOR AN A/D CONVERTER

In Figure 40C linearity error, or nonlinearity, is shown; this is defined as the maximum deviation of the actual transfer function from the ideal straight line at any point along the function. It is expressed as a percent of full scale or in LSB size, such as $\pm^1/_2$ LSB, and assumes that offset and gain errors have been adjusted to zero.

Most A/D and D/A converters available today have provision for external trimming of offset and gain errors. By careful adjustment these two errors can be reduced to zero, at least at ambient temperature. Linearity error, on the other hand, is the remaining error that cannot be adjusted out and is an inherent characteristic of the converter.

Data Converter Error Characteristics

Basically there are only two ways to reduce linearity error in a given application. First, a better quality higher cost converter with smaller linearity error can be procured. Second, a computer or microprocessor can be programmed to perform error correction on the converter. Both alternatives may be expensive in terms of hardware or software cost.

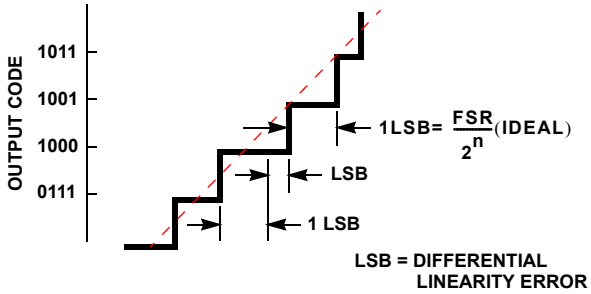


FIGURE 41. DEFINING DIFFERENTIAL LINEARITY ERROR

The linearity error discussed above is actually more precisely termed integral linearity error. Another important type of linearity error is known as differential linearity error. This is defined as the maximum amount of deviation of any quantum (or LSB change) in the entire transfer function from its ideal size of $FSR/2^n$. Figure 41 shows that the actual quantum size may be larger or smaller than the ideal; for example, a converter with a maximum differential linearity error of $\pm^1/_2$ LSB can have a quantum size between $^1/_2$ LSB and 1 $^1/_2$ LSB anywhere in its transfer function. In other words, any given analog step size is (1 $\pm^1/_2$) LSB. Integral and differential linearities can be thought of as macro- and micro-linearities, respectively.

Two other important data converter characteristics are closely related to the differential linearity specification. The first is monotonicity, which applies to D/A converters. Monotonicity is the characteristic whereby the output of a circuit is a continuously increasing function of the input. Figure 42A shows a nonmonotonic D/A converter output where, at one point, the output decreases as the input increases. A D/A converter may go nonmonotonic if its differential linearity error exceeds 1 LSB; if it is always less than 1 LSB, it assures that the device will be monotonic.

The term missing code, or skipped code, applies to A/D converters. If the differential linearity error of an A/D converter exceeds 1 LSB, its output can miss a code as shown in Figure 42B. On the other hand, if the differential linearity error is always less than 1 LSB, this assures that the converter will not miss any codes. Missing codes are the result of the A/D converter's internal D/A converter becoming nonmonotonic.

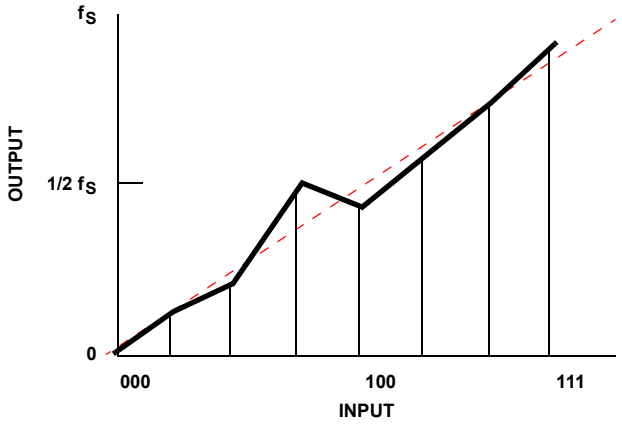


FIGURE 42A. NONMONOTONIC D/A CONVERTER

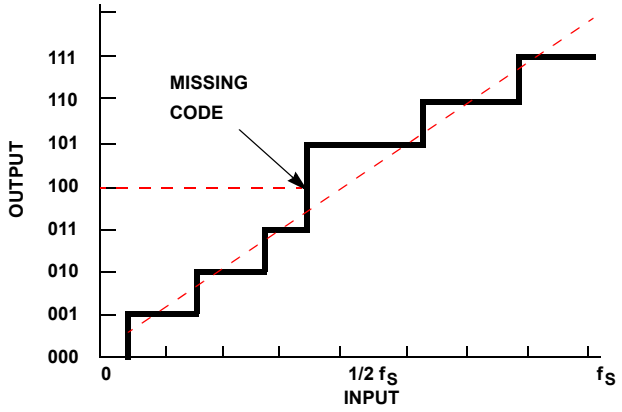


FIGURE 42B. A/D CONVERTER WITH MISSING CODE

For A/D converters the character of the linearity error depends on the technique of conversion. Figure 43A, for example, shows the linearity characteristic of an integrating type A/D converter. The transfer function exhibits a smooth curvature between zero and full scale. The predominant type of error is integral linearity error, while differential linearity error is virtually nonexistent.

Figure 43B, on the other hand, shows the linearity characteristic of a successive approximation A/D converter; in this case differential linearity error is the predominant type, and the largest errors occur at the specific transitions at $^1/_2$, $^1/_4$, and $^3/_4$ scale. This result is caused by the internal D/A converter nonlinearity; the weight of the MSB and bit 2 current sources is critical in relation to all the other weighted current sources in order to achieve $\pm^1/_2$ LSB maximum differential linearity error.

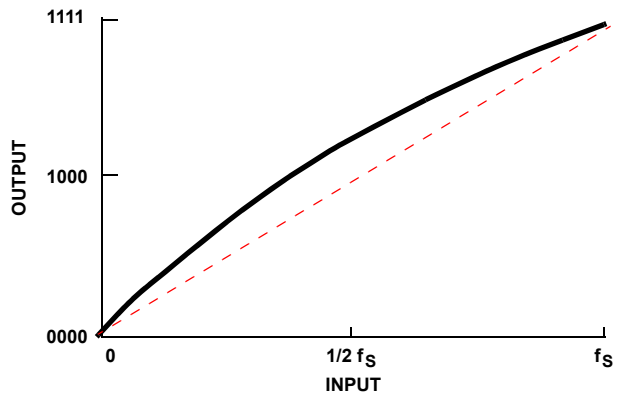


FIGURE 43A. LINEARITY CHARACTERISTICS OF INTEGRATING A/D CONVERTERS

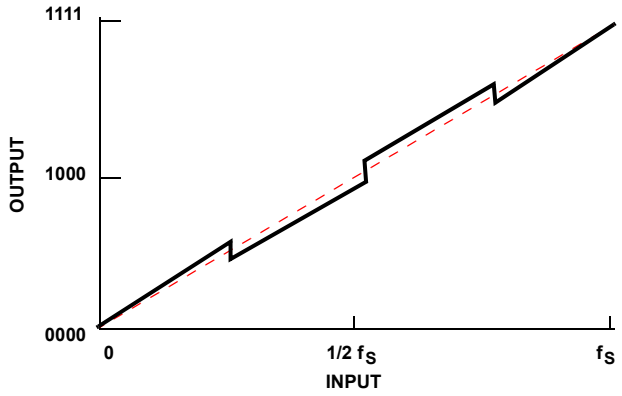


FIGURE 43B. SUCCESSIVE APPROXIMATION A/D CONVERTERS

Temperature Effects

Ambient temperature change influences the offset, gain, and linearity errors of a data converter. These changes over temperature are normally specified in ppm of full scale range per degree Celsius. When operating a converter over significant temperature change, the effect on accuracy must be carefully determined. Of key importance is whether the device remains monotonic, or has no missing codes, over the temperatures of concern. In many cases the total error change must be computed, i.e., the sum of offset, gain, and linearity errors due to temperature.

The characteristic of monotonicity, or no missing codes, over a given temperature change can be readily computed from the differential linearity tempco specified for a data converter. Assuming the converter initially has $^1/_2$ LSB of differential linearity error, the change in temperature for an increase to 1 LSB is therefore

$$\Delta T = \frac{2^{-n} \bullet 10^6}{2DLT} \qquad \text{(EQ. 19)}$$

where n is the converter resolution in bits and DLT is the specified differential linearity tempco in ppm of FSR/^{o}C. ΔT is the maximum change in ambient temperature which assures

that the converter will remain monotonic, or have no missing codes.

Selection of Data Converters

One must keep in mind a number of important considerations in selecting A/D or D/A converters. An organized approach to selection suggests drawing up a checklist of required characteristics. An initial checklist should include the following key items:

1. Converter Type
2. Resolution
3. Speed
4. Temperature Coefficient

After the choice has been narrowed by these considerations, a number of other parameters must be considered. Among these are analog signal range, type of coding, input impedance, power supply requirements, digital interface required, linearity error, output current drive, type of start and status signals for an A/D, power supply rejection, size, and weight. One should list these parameters in order of importance to efficiently organize the selection process.

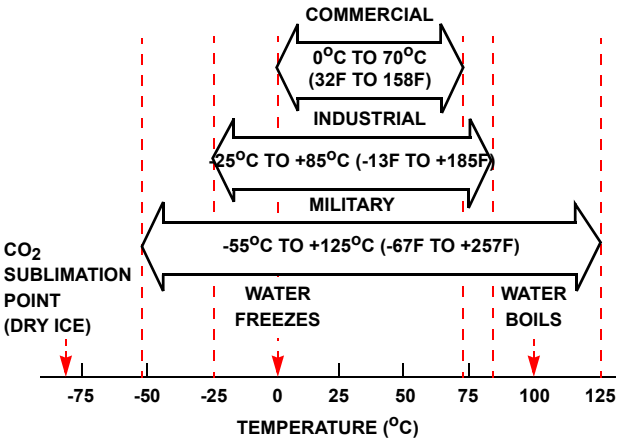


FIGURE 44. STANDARD OPERATING TEMPERATURE RANGES FOR DATA CONVERTERS

In addition, the required operating temperature range must be determined; data converters are normally specified for one of three basic ranges known in the industry as commercial, industrial, or military. These temperature ranges are illustrated in Figure 44. Further, the level of reliability must be determined in terms of a standard device, a specially screened device, or a military standard 883 device.

And finally, not to be forgotten are those important specifications, price and delivery, to which the reputation of the manufacturer must be added.

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(Rev.4.0-1 November 2017)

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