

ClockMatrix™

Aligning 1PPS Clocks in Larger Chassis Systems

Abstract

This document explains how to configure multiple ClockMatrix devices to align one pulse-per-second (PPS) signal between a master and multiple line cards in a system using Pulse-Width Modulation (PWM), DPLL alignment mode (frame and sync), phase measurement, and output phase adjustments.

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Related Documents

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1. Introduction

Commonly, a chassis system must align one pulse-per-second (1PPS or 1Hz) clock edges on different line cards with the 1PPS input of the master. As a chassis system has different types of cards plugged into a common backplane, the accuracy of the 1PPS alignment for modern applications requires compensating for the delay between the cards over the backplane. A chassis system can align two ClockMatrix devices with a pair of clocks (high and low speed) or a single Pulse-Width Modulation (PWM) encoded high-speed clock. Using PWM in signature mode, the 1PPS phase is encoded within the high-speed clock on the master by changing the pulse width in a set pattern to mark the 1PPS phase in the high-speed signal. On the line card, a PWM decoder in ClockMatrix extracts the 1PPS pulse phase signature from the PWM signal and uses it to drive a 1PPS output.



See Figure 1 for the configuration of a chassis system with paired clocks.

Figure 1. Example System using Paired Clocks

In Figure 1, the solid lines are high-speed clock signals; the dotted lines are 1PPS (1Hz) signals.

First, 25MHz and 1PPS external signals are fed into DPLL0 on the master timing card; next, the output from DPLL0 at 25MHz and 1PPS are fed through buffers. For the 25MHz signal, one output from the buffer connects to the mux to compensate for the delay through the buffer and the mux. From the buffer, another output feeds through the backplane to the DPLLs on the line cards. For ref-sync pulse alignment mode, the DPLL is configured to align the input 1PPS signal to both the output 1PPS signal and an edge of the output 25MHz signal. The 1PPS clock is fed through the second buffer to the DPLLs on the line cards. A 25MHz output from DPLL0 on each line card feeds back to the master timing card for a round-trip delay measurement. (The measurement assumes that the one-way delay across the backplane is half of the measured phase difference.) The measured phase offset sets the phase adjustment separately on each line card to adjust both the 25MHz and 1PPS outputs on each line card so that the 1PPS outputs from each line card is aligned to the 1PPS input to the master with the required accuracy.

The system measures the round-trip delay for each line card as required to compensate for delay changes through the backplane, and for comparison, the system measures the delay through the buffer before the backplane. (For a constant temperature, the delay through the backplane should not change, and the system should choose to measure only at start-up.) Because the delay is measured using a 25MHz signal, any delay over one period of this signal (40ns for 25MHz) must be manually compensated for by delaying the outputs by the measured delay pulse of the number of full cycles.

External feedback is used on the slave ClockMatrix devices to provide the lowest input-to-output delay variation for this system. This method requires two inputs per line card and one output per line card on the backplane.

Figure 2Figure 2 shows an alternate method for distributing the clocks through the system using the PWM signature mode. The main advantage of using this rather than paired clocks is that there is only two clocks per line card (one high-speed output clock with PWM to each line card and one high-speed output clock from the line card). In many designs, high-speed clocks are easier to route on each card and through the backplane.



Figure 2. Example System using PWM

In Figure 2, the lines are as follows:

- · Lightweight solid lines are high-speed clock signals;
- · Dotted lines are 1PPS (1Hz) signals; and
- Heavyweight solid lines are high-speed clock signals with embedded 1PPS signals.

In Figure 2, a similar sequence aligns the 1PPS from the line cards to the master as in Figure 1. First, 25MHz and 1PPS external signals are fed into DPLL0 on the master timing card. DPLL0 on the master card locks to the signals as a ref-sync pair encodes the 1PPS phase on the output PWM clock. Next, the PWM output from DPLL0 at 25MHz feeds through a buffer to the DPLL0 on Line Card 1 and the DPLL0 on Line Card 2. A clock output from DPLL0 on each line card feeds back to the master timing card for a round-trip phase measurement. The round-trip measurement is from the input 25MHz on the master to the clock from the line card. (The

measurement assumes that the one-way delay across the backplane is half of the measured phase difference.) This phase adjustment is used to adjust the 1PPS and 25MHz outputs from DPLL0 on each line card individually so that the 1PPS output from each line card is aligned to the 1PPS input to the master with the required accuracy. A delay of 15 cycles of the PWM encoded clock is due to the PWM encoding and decoding process, and half of the round-trip phase measurement accounts for the delay in the cabling and the buffer.

External feedback is used on the slave ClockMatrix devices to provide the lowest input-to-output delay variation in this system. This method requires two clocks on the backplane per line card (one PWM input per line card and one PWM output per line card).

2. Configuring Master with PWM in Timing Commander

In this example, three channels are used in the configuration. Channel 0 is in DPLL mode to align the frequency with the incoming high-speed signal. Channel 1 is in ref-sync alignment mode to lock to the inputs and generate the PWM output through the combo bus with the Channel 0 frequency updates. Channels 0 and 1 have the Global Sync Enable function enabled, and the output time-to-digital converter (TDC) aligns the 25MHz output clocks. Because two 25MHz signals require alignment, the master divider should be set to 20 (500/25MHz). Channel 2 measures the round-trip delay between the high-speed input and the round-trip input.

Note: To use ref-sync mode on Channel 0, several related fast-lock registers must be set to ensure a quick-lock time to the low frequency sync input.



Figure 3. Overview of Configuration for Master



Figure 4. High-Speed Input for Master

CLK2 Config
Frances
riequency
Goal Frequency: 1 PPS
Frequency Representation M/N
Numerator: 1
Denominator:
Actual Frequency: 1PPS
Input label: Low speed
Sync pulse: (none) Y 🖸 Enabled: 🔲 😭
Inverse:
Divider: 1 bypassed
Phase Offset (ps): Ops
Input Protocol: CMOS 🕤
Predefined DPLL config to use when this clock is the input to a DPLL with Predefined Configurations enabled:
Reference Monitoring
Masks Image: Construction of the section of the sec
Loss-of-Signal Config
LOS gap: LOS gap disabled Y
LOS tolerance (ms):
LOS margin
Non-Activity Config
Qualification timer: 4x
Activity limit (%): 1000 ppm Y
Frequency Offset Config
Validation interval (seconds):
Validation Interval (milliseconds):
Frequency offset limit 9.2 ppm(A), 12 ppm(R)
Phase Transient Config
Threshold (ns):
Period (µs): 0µs

Figure 5. Low-Speed Input for Master

	<u>CLK3 Config</u>	
Frequency		
Soal Frequency:	25 MHz 🎦	
Frequency Rep	esentation M/N	
Numerator:	25000000	
Denominator:	0	
Actual Frequency:	25MHz	
nput label:	High speed round trip	
iync pulse:	(none) Y 🗂 Enabled: 🔲	2
nverse:	•	
Divider:	1 bypassed	
hase Offset (ps):	Ops 🞦	
and Destaurals	CMOS y 🔼	

Figure 6. High-Speed Round-Trip Input for Master



Figure 7. DPLL Channel 0 for Master

Loop Filter Config for DPLL0						
Max Frequency Offset:	Max Frequency Offset: 0PPM					
MAIN CONFIG						
Loop Bandwidth:	25 🞦 Units: Hz 💙 🎦					
Damping Factor:	1.002, 0.02 dB, overdamp; 🛛 🖌 🎦					
Phase slope limiting:	Ons/s 📑 (no limit)					
Decimator Factor:	4 100Hz					

Figure 8. DPLL Channel 0 Loop Filter for Master

TIMING COMMANDER	Diagram	Bit Sets	_
	Q PLL0_fastlock_lock ×	All	v
	List		
			COLUMN SH
DPLL0_FASTLOCK_LOC	K_ACQ_FAST_ACQ_EN	disabled	× [
DPLL0_FASTLOCK_LOC	K_ACQ_FREQ_SNAP_EN	disabled	× [
DPLL0_FASTLOCK_LOC	K_ACQ_OL_PULL_IN_EN	disabled	× [
DPLL0_FASTLOCK_LOC	K_ACQ_PHASE_SNAP_EN	disabled	~ [*
DPLL0_FASTLOCK_LOC	K_REC_FAST_ACQ_EN	disabled	× [
DPLL0_FASTLOCK_LOC	K_REC_FREQ_SNAP_EN	disabled	× [
DPLL0_FASTLOCK_LOC	K_REC_OL_PULL_IN_EN	disabled	× [
	K REC PHASE SNAP EN	disabled	v [=

Figure 9. DPLL Channel 0 Fast Lock Settings for Master



Figure 10. DPLL Channel 1 for Master



Figure 11. DPLL Channel 1 Loop Filter for Master

8A34001 V8.4.1		
Diagram	Bit Sets	
List		
DPLL1_FASTLOCK_LOCK_ACQ_FAST_ACQ_EN	disabled	× 📑
DPLL1_FASTLOCK_LOCK_ACQ_FREQ_SNAP_EN	disabled	× 📑
DPLL1_FASTLOCK_LOCK_ACQ_OL_PULL_IN_EN	disabled	- 🖸
DPLL1_FASTLOCK_LOCK_ACQ_PHASE_SNAP_EN	enabled	~ 🖸
DPLL1_FASTLOCK_LOCK_REC_FAST_ACQ_EN	disabled	× 🖸
DPLL1_FASTLOCK_LOCK_REC_FREQ_SNAP_EN	disabled	× 🖸
DPLL1_FASTLOCK_LOCK_REC_OL_PULL_IN_EN	disabled	× 🔁
DPLL1_FASTLOCK_LOCK_REC_PHASE_SNAP_EN	enabled	- 🖸

Figure 12. DPLL Channel 1 Fast Lock Settings for Master



Figure 13. Phase Measurement (Channel 2) for Master





Figure 14. Output TDC for Master

			×
<u>Outp</u>	ut TDC0 A	lignme	nt Mask
DPLLO	2	DPLL4	
DPLL1		DPLL5	
DPLL2		DPLL6	
DPLL3		DPLL7	
Align Ta	rget Mask	0000	0001

Figure 15. Output TDC0 Alignment Mask for Master

PWM Encoders						
DUAL-CHANNEL	Enabled	<u>Signature Mode</u>	TOD Tx Signal Configuration	<u>Carrier</u>	<u>Trigger</u>	<u>ID</u>
Encoder 0			🔲 🕤 ToD PPS 🛛 🕤 primary output 🝸 🗂 TODO 👻 🗂			0 🛅
Encoder 1	Z 🖸		🔲 💼 💽 alternate PPS 🝸 🎦 primary output 🛛 🍸	Q2	Q3	0 🛅

Figure 16. PWM Configuration for Master

		x		
PWM1 ENCODER Signature				
Symbol 1	zero	× 🖸		
Symbol 2	zero	× 📑		
Symbol 3	zero	× 🖸		
Symbol 4	zero	× 🗂		
Symbol 5	zero	× 🗂		
Symbol 6	zero	× 🖸		
Symbol 7	zero	× 🖸		
Symbol 8	zero	× 🖸		

Figure 17. PWM Signature Configuration for Master

Note: For the PWM encode to operate correctly, a 1PPS signal must be configured for Q1; however, it can be set to output type "high-Z" to avoid noise on other signals, or it can be used as a test point.

3. Configuring Line Card with PWM in Timing Commander

In this example, two channels are used in the configuration. Channel 0 is in DPLL mode with external feedback and locks to the frequency and PWM encoded phase of the input signal. Channel 1 is a satellite channel that works with Channel 0 to generate additional clocks locked to the inputs. Channels 0 and 1 have the Global Sync Enable function enabled with a master divider of 20 (500/25 MHz) to align the two 25MHz outputs. The **Phase Offset** value (from the round-trip measurement on the master card) is applied only to Channel 0, and this is provided to Channel 1 through the output TDC. (The combo bus aligns the frequency of the two channels so that the output TDC only requires a small phase adjustment.)

Note: To use ref-sync mode on Channel 0, several related fast-lock registers must be set to ensure a quick-lock time to the low frequency sync input.



Note: A line card does not require a TCXO or OCXO.

Figure 18. Overview of Configuration for Line Card



Figure 19. High-speed Input for Line Card

LKL Config Fequency Gol Frequency Lenominator: Lonominator: Lonominator: <th></th> <th>x</th>		x			
Erequency 25 Goal Frequency Representation M/N Numerator: 2500000 Denominator: 0 Actual Frequency: 25MHz Imput labet: High Speed FB Sync pute: (none) Imput labet: High Speed FB Sync pute: (none) Inverse: 1 Divider:	CLK1 Config				
Goal Frequency: 25 Frequency Representation M/N Numerator: 2500000 Denominator: 0 Otal Frequency: 25MH: Actual Frequency: 25MH: Input label: Figh Speed FB Origin Date: Inone: Outline: Outline: Outline: Numerator: Outline: Inone: Outline: Outline: Imput label: Figh Speed FB Outline: Imput label: Imput label: Imput label: Imput Protocol: VDS Outline: Imput Protocol: VDS Outline: Imput Protocol: VDS Imput Protocol: VIDS Imput Protocol: VIDS Imput Protocol: VIDS Imput Protocol: VDS Imput Protocol: VIDS Imput Protocol: VIDS Imput Protocol: VIDS Imput Protocol: VIDS Imput Protocol:	Frequency				
Frequency Representation M/N Numerator: 2500000 Denominator: 0 Actual Frequency: 25MH: Input label: Figh Speed FB 0 Sync pulse: 1 0 Didder: 1 0 Prase Office((pp): 0.05 0 Input Protocol: V/DS 0 Prase framed Config 0 consold 0 Image: 1 0 0 Image: 1 0 0 0 Prase of signal 1 0 0 0 Image: 1 0 0 0 0 Image: 1 0 0 0 0	Goal Frequency:	25 🙆			
Numerator: 2500000 Denominator: 0 Actual Frequency: 25MH: Input label: Figh Speed FB Sync pulse: 1 Input label: Figh Speed FB Order: 1 Divider: 0 Divider: 0 Praced Prace Praced 0 Dispusification time: 2.5 s Dispusification time: 2.5 s Qualification time: 2.5 s Dispusification time: 2.5 s US tolerance (ms): 0 Qualification time: 2.5 s Vidication time: 4.x * Vidication time: 9.2 ppm(A), 12 ppm(R) • Vidication time: 9.2 ppm(A), 12 ppm(R)<	Frequency Rep	resentation M/N			
benominator: 0 Actual Frequency: 25MHz Input label: High Speed FB Sync pubs: (none) Imput label: High Speed FB Sync pubs: (none) Imput label: High Speed FB Sync pubs: (none) Imput label: Imput label: Sync pubs: (none) Imput label: Imput label: Imput Protocol: UDS Predefined DPLL config to use when this dock is the input to a DPLI with redefined Configurations enabled: PredD Predefined DPLL config to use when this dock is the input to a DPLI with redefined Configurations enabled: Imput Protocol: Imput Protocol: UDS Imput PredD Imput Protocol: Imput Protocol: UDS Imput Protocol: Imput Protocol: Imput Protocol: UDS Imput PredD Imput Protocol: Imput Protocol: UDS Imput Protocol: Imput Protocol: Imput Protocol: UDS Imput Protocol: Imput Protocol: Imput Protocol: Imput Protocol: Imput Protocol: Imput Protocol: Imput Protocol: Imput P	Numerator:	2500000 📑			
Actual Frequency: 25MHz: Imput labe: High Speed FB Sync pube: Imput labe: Imput	Denominator:	• 🖸			
Input labe: High Speed FB Sync pubs: (none) Inverse: Imput Protocol: Divider: Imput Protocol: IVDS Imput Protocol: Imput Protocol: IVDS Predefined DPLL config to uce when this clock is the input to a DPL with Predefined Configurations enabled: Predefined DPL config to uce when this clock is the input to a DPL config to uce when this clock is the input to a DPL config to uce when this clock is the input to a DPL config to uce when this clock is the input to a DPL config to uce when this clock is the input to a DPL config to uce when this clock is the input to a DPL config to use when this clock is the input to a DPL config to use when this clock is the input to a DPL config to use when this clock is the input to a DPL config to use when this clock is the input to a DPL config to use when this clock is the input to a DPL config to use when this clock is the input to a DPL config to use of signal Imput to a DPL config to use of signal Imput to a DPL config to use when this clock is the input to a DPL config to use when this clock is the input to a DPL config to use when this clock is the input to a DPL config to use when the clock is the input to a DPL config to use the clock is the input to a DPL config to use the clock is the input to a DPL config to use to a DPL config to us	Actual Frequency:	25MHz			
Sync pubse: (none) Image: Gradient Control of Co	Input label:	High Speed FB			
Inverse: Divider: 1 bypassed Phase Offiset (ps): Input Protocol: Input Protocol: VDS Predefined DPLL config to use when this clock is the input to a DPLL with Predefined Configurations enabled: Predefined Configurations enabled: Disparations (ms): Disparations (ms): Disparatification timer: Activity Config Disparatification timer: Activity Imit (%): 1000 ppm Predefined Config Threshold (ns): Priced (us): Output Disparation (Us): Output Disparation (Us): Output Disparation (Us): Predefined Config Threshold (ns): Output Disparation (Us): Output Disparation (Us): Disparation (Us): Disparati	Sync pulse:	(none) Y 💽 Enabled: 🔲 🎦			
Divider: 1 Dispassed Phase Officer (pg): 0p5 Input Protocol: VDS C Prodefined DPLL config to use when this clock is the input to a DPLL with Predefined Configurations enabled: PredU Reference Monitoring C frabled Masks Reference Monitoring C frabled Masks C for another of the phase transient Dispassed is so of signal fraction on a-activity framework frequency offset fraction of the phase transient Loss of ransee (ms): 0 fraction LOS tolerance (ms): 0 fraction Prequency Offset Config Validation interval (milliseconds): 0 fraction Frequency offset limit: 9.2 ppm(A), 12 ppm(R) fraction Phase Transient Config Threshold (ns): 0 fraction Priced (us): 0 fraction Priced (us): 0 fraction Phase Transient Config Threshold (ns): 0 fraction Phase Transient Config Display fraction the fraction Phase Transient Config Display fraction fraction Phase Transient Config Display fracti	Inverse:				
Phase Offiset (ps) Toput Protocol: Typut Pro	Divider:	1 bypassed			
Input Protocol: UDS view when this clock is the input Productional DPLL config to use when this clock is the input to a DPLL with Predefined Configurations enabled:	Phase Offset (ps):	Ops 📑			
Predefined DPLL config to use when this clock is the input to a DPLL with Predefined Configurations enabled:	Input Protocol:	LVDS 👻 🖻			
Reference Monitoring 	Predefined DPLL con to a DPLL with Prede	fig to use when this clock is the input			
Reference Monitoring Enabled Masks Ioss of signal non-activity frequency offset phase transient Loss of signal phase transient Loss of signal phase transient Loss of signal config Gap disabled frequency offset gap disabled frequency config Disqualification timer: gap disabled frequency offset frequency offset gap disabled frequency offset frequency offset Config Validation interval (milliseconds): gap gap (acconds): gap (acconds): gap (acconds):<					
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Loss-of-Signal Config LoS gap: LOS qap disabled LOS tokrance (ms): 0 Image: Disputification time: 2.5 s Qualification time: $4x$ Qualification time: $4x$ Activity Lonfig 0 Disqualification time: $4x$ Activity limit (%): 1000 ppm Frequency Offset Config 0 Validation interval (wellisecond): 0 Frequency offset limit: 9.2 ppm(A), 12 ppm(R) Phase Transient Config 1 Threshold (ms): 0 Period (µc): 0	Masks	signal I non-activity I fransient detect			
LOS gap: LOS qap disabled ✓ LOS tolarance (ms): 0 LOS tolarance (ms): 0 LOS margin Non-Activity Config Diqualification timer: 2.5 s ✓ Qualification timer: 4x ✓ • 2.5 s = 10000ms Activity limit (%): 1000 ppm ✓ • • • • • • • • • • • • • • • • • •	Loss-of-Signa	l Config			
LOS tolarance (ms): 0 Cos margin Non-Activity Config Diqualification timer: 2.5 s	LOS gap:	LOS gap disabled 👻 🛅			
Image: US margin Non-Activity Config Disqualification timer: Qualification timer: $4x$ $4x$ $4x$ $4x$ $4x$ 2.5 ± 10000 ms Activity limit (%): 1000 ppm $4x$ $4x$ $4x$ $4x$ 2.5 ± 10000 ms Activity limit (%): 1000 ppm $4x$ $10x$ $10x$ $10x$ $10x$ $10x$ $10x$ $10x$ $10x$	LOS tolerance (m	sj: 0 🗂			
Non-Activity Config Disqualification timer: 2.5 s Qualification timer: $4x$ Activity limit: $92 \text{ s} = 10000 \text{ ms}$ Activity limit: 91000 ppm Frequency Offset Config Validation interval (seconds): 0 Validation interval (realized): 0 Frequency offset limit: $9.2 \text{ ppm}(A), 12 \text{ ppm}(R)$ Phase Transient Config Threshold (rs): 0 Quisition interval 0	LOS ma	argin			
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Activity limit (%): 1000 ppm v •	Qualification time	er: 4x Y 2.5 s = 10000ms			
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Validation Interval (milliseconds): 0 Frequency offset limit: 9,2 ppm(A), 12 ppm(R) Phase Transient Config Threshold (ns): 0 Period (us): 0 Usi	Validation interva	l (seconds):			
Frequency offset limit: 9.2 ppm(A), 12 ppm(R)	Validation Interva	I (milliseconds):			
Phase Transient Config Threshold (ns): 0 Period (uc): 0µs):	Frequency offset	limit: 9.2 ppm(A), 12 ppm(R) 🛛 🔀			
Threshold (ns): 0 Period (µs): 0µs	Phase Transie	nt Config			
Period (µs): Oµs	Threshold (ns):				
	Period (µs):	Ομε			

Figure 20. Feedback Input for Line Card

		x
	Channel 0	🔀 🎦 Global Sync Enable
Mode of Operation: DPLL Mode	 1 1 	
Profile: Jitter Attenuator 🛛 🗧	1	d 🗌 h
Jitter Attenuator (loop filter bw 50Hz > 10Hz)		
Phase Control Werd Phase Error Pro- Decimator	Digital Loop Fittered Fittered Voter Voter Fittered Voter Chan	control 5'S APLL 13.4076dtz t t t t t t t t t t t t t t t t t t t
Combo Mode - Master (for Filtered source) Filter input: integrator value only Bandwidt: 0 Unit: UHz Unit: UHz	Combo Mode - Slave	Enable secondary combo source
proportional and integrator of the Master.	Input Reference	Alignment Mode
Lock Criteria	Reference Mode: manual Y	frame pulse mode
Error: 1 🖸 * 100ns - Y 🞦	Hitless: 🔲 🗂 PLL Feedback Src: 🔲 🗂	
Duration (sec): 1 1 100ns over 1 second	Hitless type: HS type 1 🗸 🎦	Write Timer Mode
		simple holdover mode 🝸 🎦
External Feedback	Input: CLK0 Y	
Enabled: 🖉 🛅		
Reference: Input 1	Phase Offset	
	Goal: Ops Actual: Ops	

Figure 21. DPLL Channel 0 Configuration for Line Card

Loop Filter Config for DPLL0					
Max Frequency Offset					
MAIN CONFIG					
Loop Bandwidth:	50 🗂 Units: Hz 💙 📑				
Damping Factor:	1.002, 0.02 dB, overdamp; 🛛 🖌 🛅				
Phase slope limiting:	Ons/s 👩 (no limit)				
Decimator Factor:	4 200Hz				

Figure 22. DPLL Channel 0 Loop Filter Configuration for Line Card

DPLL0_FASTLOCK_LOCK_ACQ_FAST_ACQ_EN	disabled 🗸 🔁	
DPLL0_FASTLOCK_LOCK_ACQ_FREQ_SNAP_EN	disabled 🗸 🗂	
DPLL0_FASTLOCK_LOCK_ACQ_OL_PULL_IN_EN	disabled 🗸 🗂	
DPLL0_FASTLOCK_LOCK_ACQ_PHASE_SNAP_EN	enabled 🗸 🎦	
DPLL0_FASTLOCK_LOCK_REC_FAST_ACQ_EN	disabled 🗸 🗂	
DPLL0_FASTLOCK_LOCK_REC_FREQ_SNAP_EN	disabled 🗸 📑	
DPLL0_FASTLOCK_LOCK_REC_OL_PULL_IN_EN	disabled 🗸 🗂	
DPLL0_FASTLOCK_LOCK_REC_PHASE_SNAP_EN	enabled 🗸 🎦	
DPLL0_FASTLOCK_PRE_FAST_ACQ_TIMER	0	

Figure 23. DPLL Channel 0 Fast Lock Register Configuration for Line Card

PWM Decoders					
Enabled	Generate PPS	PPS Rate	Signature Mode	ID	
Decoder 0 🛛 🖸	☑ 🖸	1Hz 🎦		0	

Figure 24. PWM Configuration for Line Card

		x			
PWM0 DECODER Signature					
Symbol 1	zero	× 🗂			
Symbol 2	zero	× 🗂			
Symbol 3	zero	× 🖸			
Symbol 4	zero	× 🗂			
Symbol 5	zero	× 🖸			
Symbol 6	zero	× 🖸			
Symbol 7	zero	× 🖸			
Symbol 8	zero	× 🗂			

Figure 25. PWM Configuration Signature for Line Card



Figure 26. Synthesizer Channel 1 Configuration for Line Card

											x
	Output TDC Config										
Enable Output 1 Reference Clock	TDC: XTAL	× 🚺	Fast Lock Enable Delay	r. 0	500µs	Fast Lock Disable	eDelay:	0 🞦 500µs		read	
	<u>Source</u>	<u>Target</u>	Mode	<u>Туре</u>		<u>Align Reset</u>		<u>Samples</u> (0 == 4096)	<u>Target Phase</u> <u>Offset</u>	<u>Measurement</u> <u>Status</u>	<u>Go</u>
Output TDC 0	DPLLO Y	DPLLO Y	alignment 🛛 🐣	continuous	Keep	accumulated 🗡	Alignment Mask	0	0	9280	🗖 🖸
Output TDC 1	DPLL0 Y	DPLL0 Y	measurement Y	single shot	keep	accumulated Y	Alignment Mask	0	0	0	
					<u> </u>						
Output TDC 2	DPLL0 Y	DPLL0 Y	measurement Y	single shot	keep	accumulated Y	Alignment Mask	0	0	0	
					<u> </u>						
Output TDC 3	DPLL0 Y	DPLL0 Y	measurement Y	single shot	keep	accumulated 🗡	Alignment Mask	0	0	0	

Figure 27. Output TDC for Line Card



Figure 28. Output TDC0 Alignment Mask for Line Card

	×				
	OUT1 Config				
Output Label:	Low Speed Output				
Squelch:	squelch disabled 🛛 🎽 🗂				
Squeich Value:	low Y				
Divider:	50000000				
VDDO:	1.8V Y				
Output Type:	LVCMOS, Q enabled, 👻 🎦				
Divider Sync:	enable Y				
Output Sync					
Pulse Code:	custom Y				
Frame Pulse Mode:					
Associated Clock:					
Duty Cycle High:					
Actual High Cycle: 0.0ns					
Cool phase adjust	e: IS				
Goal phase adjust Ulis Actual: Ofs					
Circle Coded Output					
Voltage Impediance: 60 Ohm					
voitage impedance					

Figure 29. Output 1PPS (Q1) for Line Card

The **Goal phase adjust** for the low speed clock is where the adjustment (that is based on the individual phase measurement) is set on each line card. This value should be set to 15 periods of the PWM clock, and it should be half of the round-trip phase measurement.

4. Revision History

Revision	Date	Description
1.0	Nov.17.20	Initial release.

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