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# M16C/60,M16C/20 Series

## Address Match Interrupt

### 1. Abstract

This document describes sample application for ROM correction functions using address match interrupts.

### 2. Introduction

The explanation of this issue is applied of the following condition.

Applicable MCU: M16C/60 Series, M16C/20 Series.

### 3.0 Contents

### 3.1 Outline of Address Match Interrupt

The Address Match Interrupt is generated immediately before execution of the instruction indicated by the address set in the Address Match Interrupt Register. The M16C/60 Series is equipped with 2 Address Match Interrupt Registers.

**Enabling/Disabling The Address Match Interrupt**

The Address Match Interrupt Enable Bit enables or disables an Address Match Interrupt. It is not affected by the Processor Interrupt Priority Level (IPL) nor the Interrupt Enable Flag (I Flag).

**Timing of Address Match Interrupt Generation**

Set the first address of the instruction in the Address Match Interrupt Register. However, the interrupt will not be generated if the first address of the starting instruction in an interrupt routine is set. Also, setting an address from the middle of an instruction or an address of tabulated data does not generate an interrupt.

**Returning from An Address Match Interrupt**

The return destination address saved in the stack when an Address Match Interrupt occurs depends on the instruction of the address indicated by the Address Match Interrupt Register. Either rewrite the stack and return from the interrupt using the REIT instruction, or restore the stack to its pre-interrupt state using the POP instruction, etc., and return from the interrupt using the jump instruction.

**How to Determine An Address Match Interrupt**

Address Match Interrupts can be set in two different locations as M16C/60 Series MCUs are equipped with 2 Address Match Interrupt Registers. However, there is only one vector address for housing the interrupt routine starting address. Therefore, it is necessary to determine which Address Match Interrupt Register has generated the Address Match Interrupt. In the first part of the interrupt routine, determine which interrupt has occurred, using the contents of the stack, etc

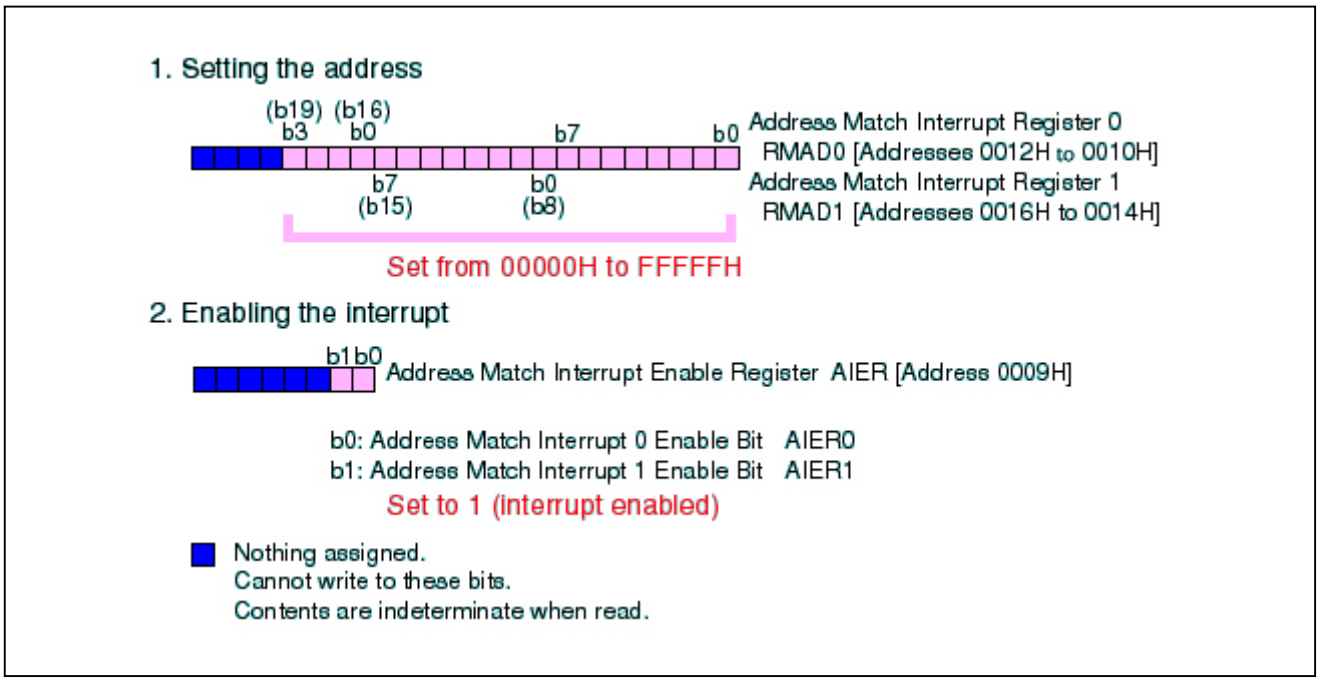


**Figure1. Setup Procedure**

## 3.2 ROM Correction

The ROM Correction Function uses the Address Match Interrupt to correct deficiencies detected after mask production.

1. After reset, send the corrected program to the internal RAM from external memory ($E^2$EPROM, etc.). The address, which contains the deficiency, should be set in the address match interrupt register.
2. An Address Match Interrupt is generated just before the address set in the Address Match Interrupt Register is executed.
3. Arrange the Address Match Interrupt program so that the program, which was transferred to the internal RAM, is executed in the Address Match Interrupt routine.

Note: The ROM Correction Function is not for reprogramming a masked code with the correct code.

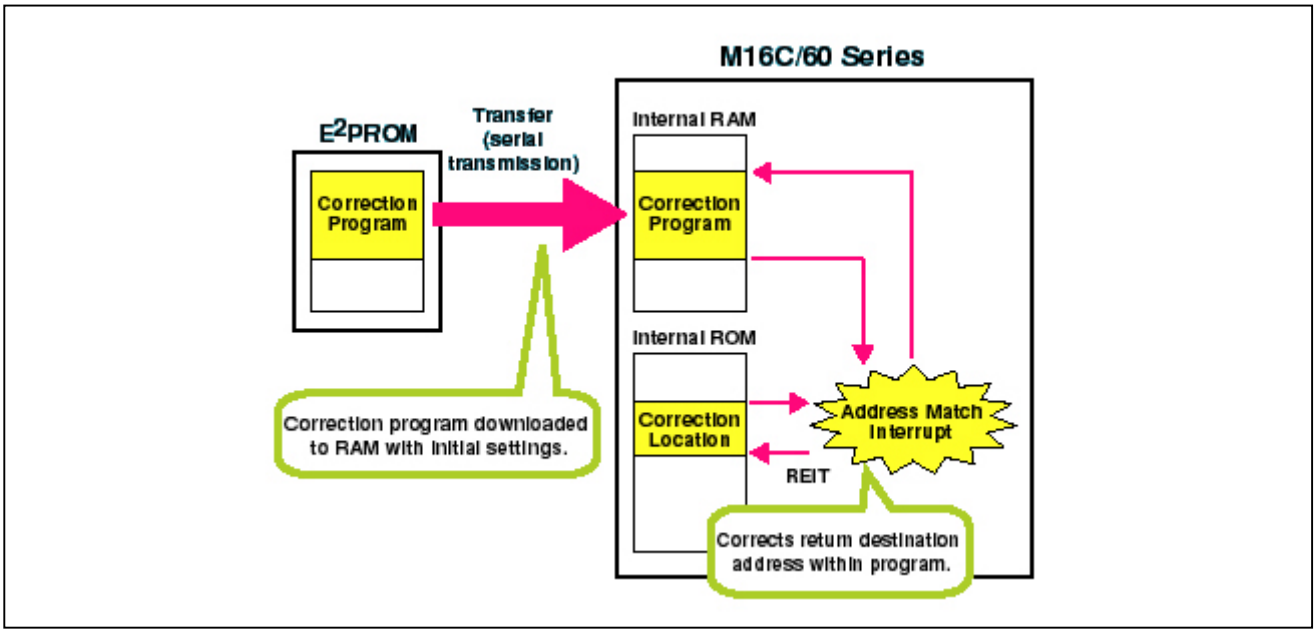


**Figure2. Sample Application of ROM Correction Function using Address Match Interrupt**

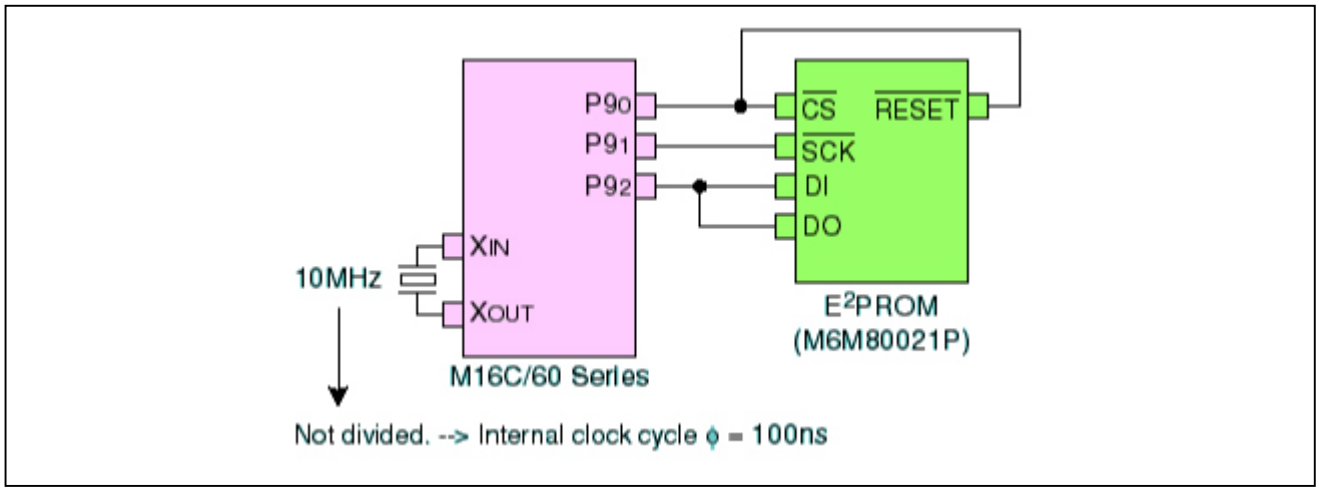

**Figure3. Hardware Configuration Example**

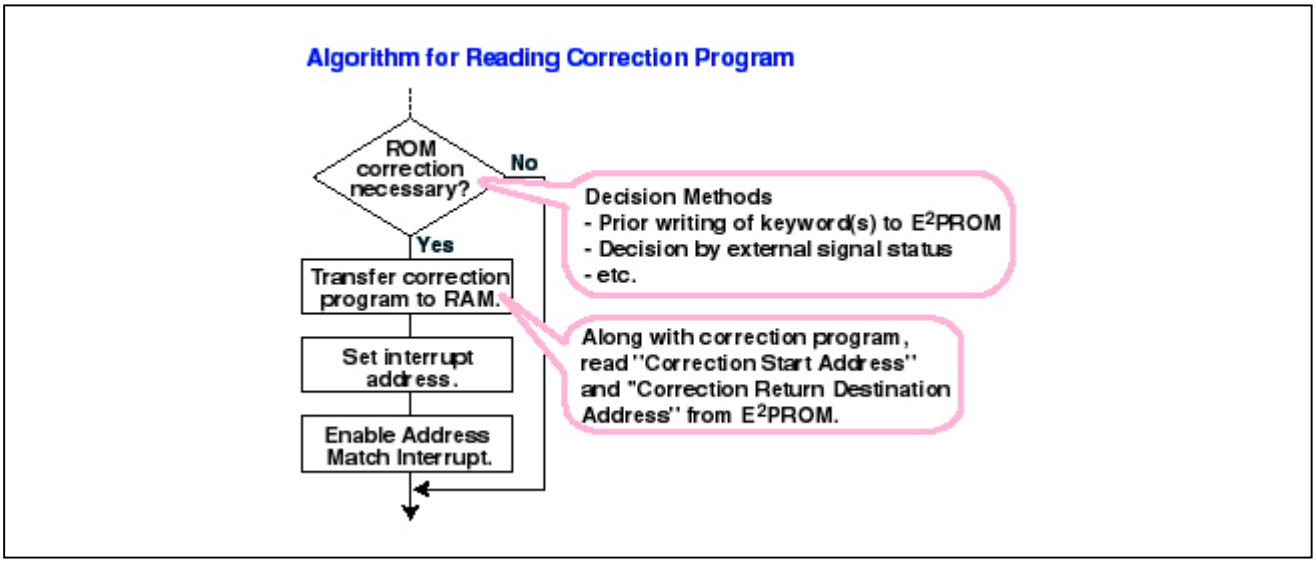


**Figure4. Software Program [Initial Settings]**

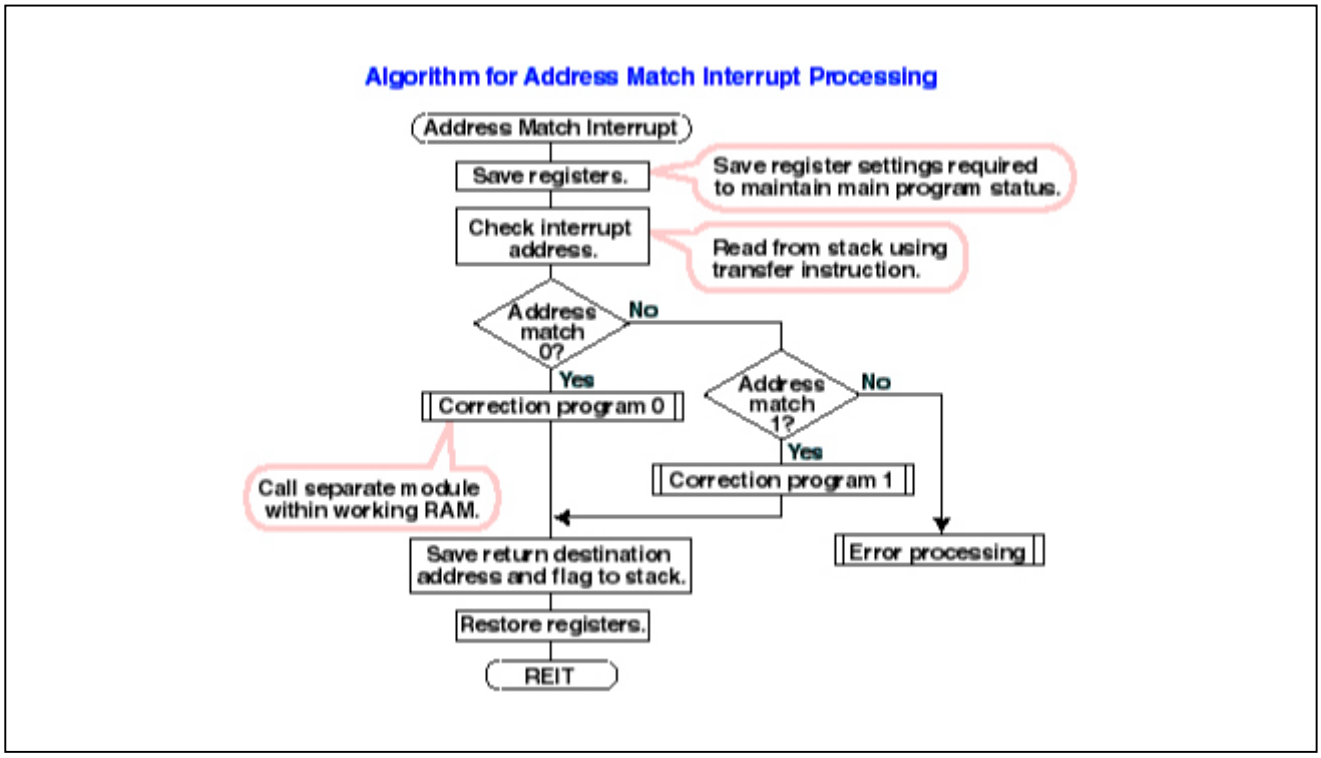


**Figure5. Software Program [Address Match Interrupt Processing]**

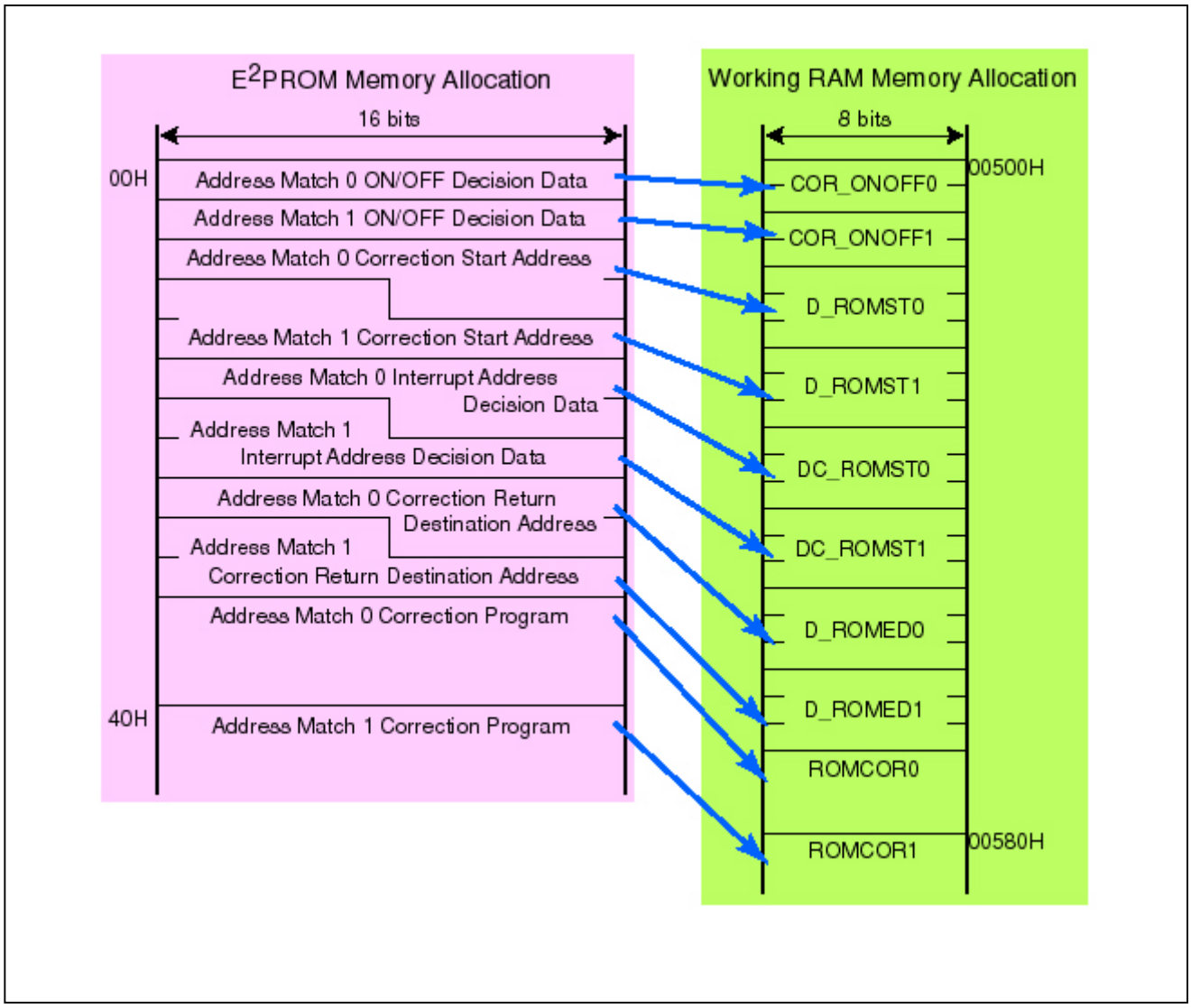


**Figure6. Memory Allocation Example**

**Address Match 0/1 ON/OFF Decision Data**

**COR_ONOFF0/1**

This value determines whether to use the Address Match Interrupt 0/1.

When "0," Address Match Interrupt 0/1 is invalid, when "00A5H," it's valid.

**Address Match 0/1 Correction Start Address**

**D_ROMST0/1**

This value is set to the Address Match Interrupt Register 0/1.

**Address Match 0/1 Interrupt Address Decision Data**

**DC_ROMST0/1**

This value is saved to the stack when an Address Match Interrupt is generated.

It determines whether Address Match Interrupt 0 or 1 has been generated.

**Address Match 0/1 Correction Return Destination Address**

**D_ROMED00/1**

This is the return destination address from the Address Match Interrupt.

The REIT instruction returns to this address from the Address Match Interrupt.

**Address Match 0/1 Correction Program**

**ROMCOR0/1**

This is the correction program.

The correction program size for Address Match Interrupt 0 is approximately 100 bytes.

There are no program size limitations in the correction program for Address Match Interrupt 1, except for the $E^2$PROM and MCU internal RAM sizes.

**How to Determine the Address Match Interrupt Register**

The address for generation of the Address Match Interrupt can be set in two different locations. However, there is only one vector address for both addresses. Therefore, it is necessary to determine, in the first part of the interrupt routine, which address will generate the interrupt.

The method for determining this is to use the address saved in the stack. When an Address Match Interrupt is generated, the address listed below is saved in the stack. The generated interrupt can be determined by examining the addresses saved in the stack.

**Addresses To Be Saved**

When an Address Match Interrupt is generated, the value "match address +1" or "+2" ("the first address of instruction +1" or "+2") is saved to the stack. The decision to increment the address saved to the stack by "+1" or "+2" depends on the instruction at which the match occurred.

**Instructions requiring increment of "address +2" at Address Match Interrupt]**

1. 16-bit op-code instructions
2. The following 8-bit op-code instructions (when dest = A0/A1)

```
ADD.B:S #IMM8,dest
OR.B:S #IMM8,dest
STNZ.B:S #IMM8,dest
CMP.B:S #IMM8,dest
JMPS #IMM8
MOV.B:S #IMM,dest
SUB.B:S #IMM8,dest
MOV.B:S #IMM8,dest
STZX.B:S #IMM81,#IMM82,dest
PUSHM src
JSRS #IMM8
AND.B:S #IMM8,dest
STZ.B:S #IMM8,dest
POPM dest
```

**[Instructions requiring increment of "address +1" at Address Match Interrupt]**

All instructions other than those indicated above.

### 3.3 Example of Address Match Interrupt

The following processes are performed in the ROM correction sample program.

1. The address to be stored in the stack when an Address Match Interrupt is generated is calculated from the correction address and the instruction to be corrected, and saved in the EPROM.
2. The address calculated in #1 above and the actual address saved in the stack are compared in the first part of the interrupt routine.

```
        MOV.W   0[SP],R2            ;Read address from stack
        MOV.B   3[SP],R0L
        AND.B   #0FH,R0L            ;Only lower 4 bits are valid
        BTST    F_ROMCOR0           ;Determine whether Address Match 0 Interrupt is enabled
        JZ      JUDGE_1             ;No "ROM Correction 0" -> Judge "ROM Correction 1"
        CMP.W   DC_ROMST0,R2        ;Correction location?
        JNZ     JUDGE_1
        CMP.B   DC_ROMST0+2,R0L
        JZ      ROM0
JUDGE_1:
        BTST    F_ROMCOR1           ;Determine whether Address Match 1 Interrupt is enabled
        JZ      AD_ERR              ;No "ROM Correction 1" (Perform neither ROM correction)
        CMP.W   DC_ROMST1,R2        ;Correction location?
        JNZ     AD_ERR
        CMP.B   DC_ROMST1+2,R0L
        JZ      ROM1
        JMP     AD_ERR
ROM0:
        JMP     ROMCOR0             ;Jump Address Match 0 Correction Program
ROM1:
        JMP     ROMCOR1             ;Jump Address Match 1 Correction Program
AD_ERR:
        JMP     ERROR               ;Error processing
```

## 4. Reference

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## REVISION HISTORY

| Rev. | Date | Description | |
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| | | Page | Summary |
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| | | | |
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