Introduction

In BITS applications, there are cases where the reception and transmit of a 2048kHz clock, as described in G.703 Chapter 13, are desired.

This application note can also be applied to the following IDT devices: 82V2082, 82V2084, 82V2088, 82P2281, 82P2282, and 82P2284.

2048kHz Digital Clock Specifications

The transmit port (output) of a 2048kHz digital clock should meet the following specifications. The signal is measured at the line side of the transmit transformer, at the near end of the cable, with a 75 ohm or 120 ohm resistive load in place of the cable. From an implementation viewpoint, the output signal described in G.703 section 13 is a configuration mode of the E1 output port that is designated as a timing source and will have similar electrical and connector characteristics.

The 2048kHz digital clock output signal accuracy and jitter characteristics will be directly related to the 2048kHz system clock used to generate the synchronization signal together with the transmitter characteristics. The system clock signal will be the same clock signal that is used to define the HDB3 (pulse) signal timing for the same port in E1 mode. Note that the pulse rate of an E1 signal is 2048k pulses per second, whereas its fundamental frequency is 1024kHz, therefore the transmission of a 2048kHz system clock in place of an E1 signal can be considered a doubling of the frequency of the transmitted data signal.

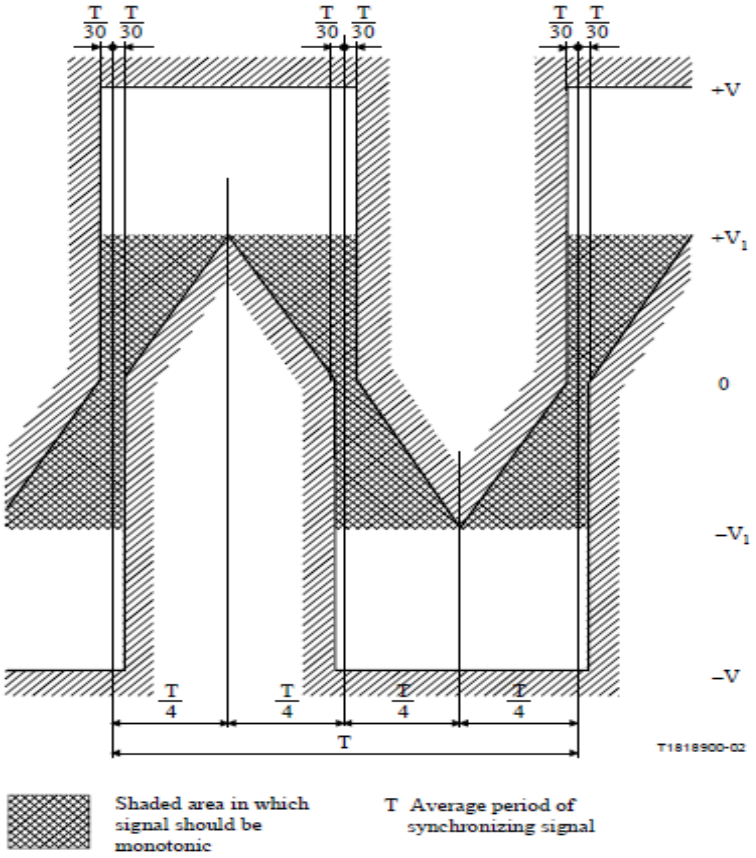

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Table 1: Digital 2048 kHz Clock Interfaces

Pulse Shape	Signal Requirement	
Type of Interface	**Coaxial Pair**	**Symmetrical Pair**
Impedance	75Ω	120Ω
Max Peak Voltage (V)	1.5V	1.9V
Min Peak Voltage (V1)	0.75V	1.0V
Max Jitter at Output	(see Table 2)	

Table 2: Maximum Permissible Jitter at Synchronization Interfaces

Output Interfaces	Frequency Accuracy	Measurement Bandwidth, -3 dB Frequencies (Hz)	Peak-to-Peak Amplitude (UIpp)
PRC	G.811	20–100k	0.05
SSU	G.812	20–100k	0.05
SEC	4.6ppm (refer to G.813)	20–100k	0.5
		49–100k	0.2
PDH Synchronization	±50ppm	20–100k	1.5
		18–100k	0.2

Note: For other specifications (i.e., noise tolerance at input ports), please refer to G.812 and G.813 for SSU and SEC, respectively.

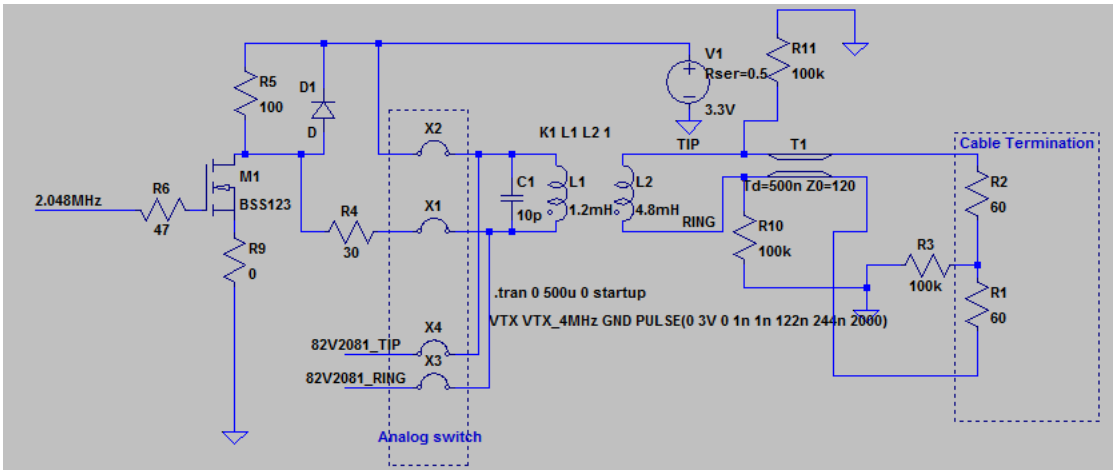
Receive and Transmit of 2048kHz Clock

By configuring 82V2081 in “slicer” mode (R_MD[1:0] = 00), the receiver will work in slicer mode. The 2.048MHz clock can be received and output at RDP/RDN. In order to transmit the clock, the following circuit in Figure 1 is proposed.

The transmitter needs to be external for G.703 Section 13 support. For the external circuit to work, 82V2081's own transmitter needs to be in high impedance to avoid signal conflict. That can be realized by setting T_OFF = 1.

External circuit in Figure 1 is shown below. The circuitry consists of discrete components. The 2.048MHz is a 3.3V CMOS clock input signal. The transistor (M1) is used to boost transmitter's driving capability into the transmission lines. The power for the transistor can be 3.3V or 2.5V. The selection of 3.3V or 2.5V is discussed in the following section. The transformer is modeled from our suggested turn ratio = 1:2 transformers (refer to AN-377).

Figure 1. Proposed External Transmitter Circuit



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Transmitted pulses are analyzed with the following simulation results. Figure 2 shows the transmitted pulses with 3.3V power supply for the transistor (M1). The total pulse amplitude is 4.1V with 2.4V DC offset. The net signal amplitude is 1.7V, meeting pulse amplitude requirement for twisted-pair transmission (refer to Table 1 above).

Figure 2. Transmitted Pulses with 3.3V

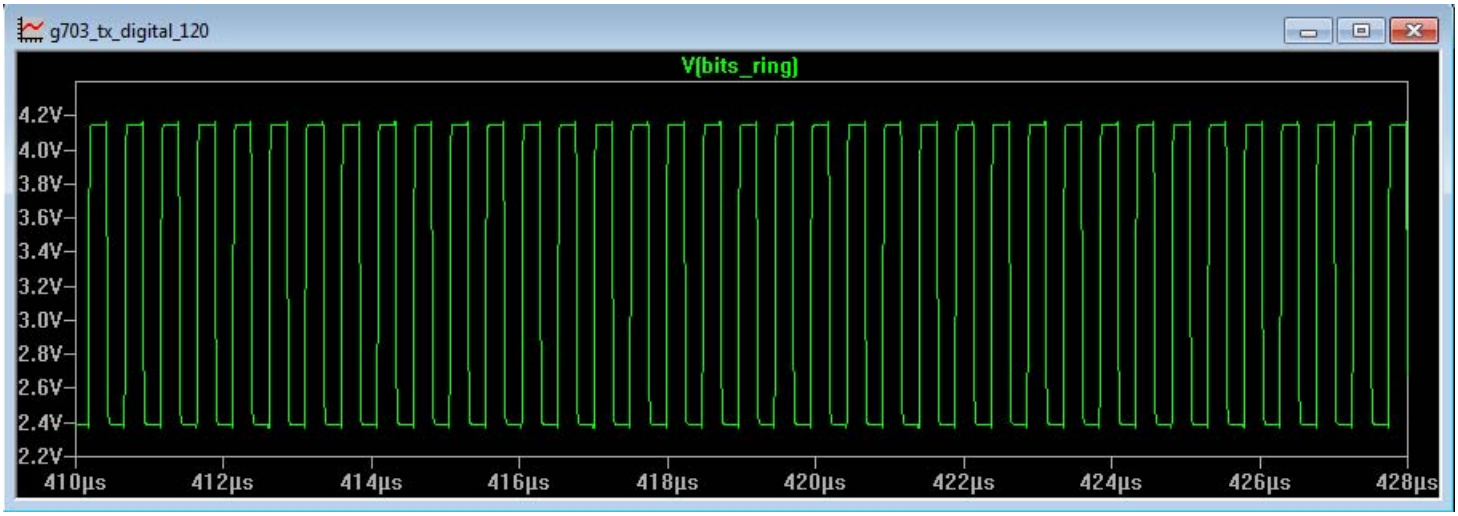
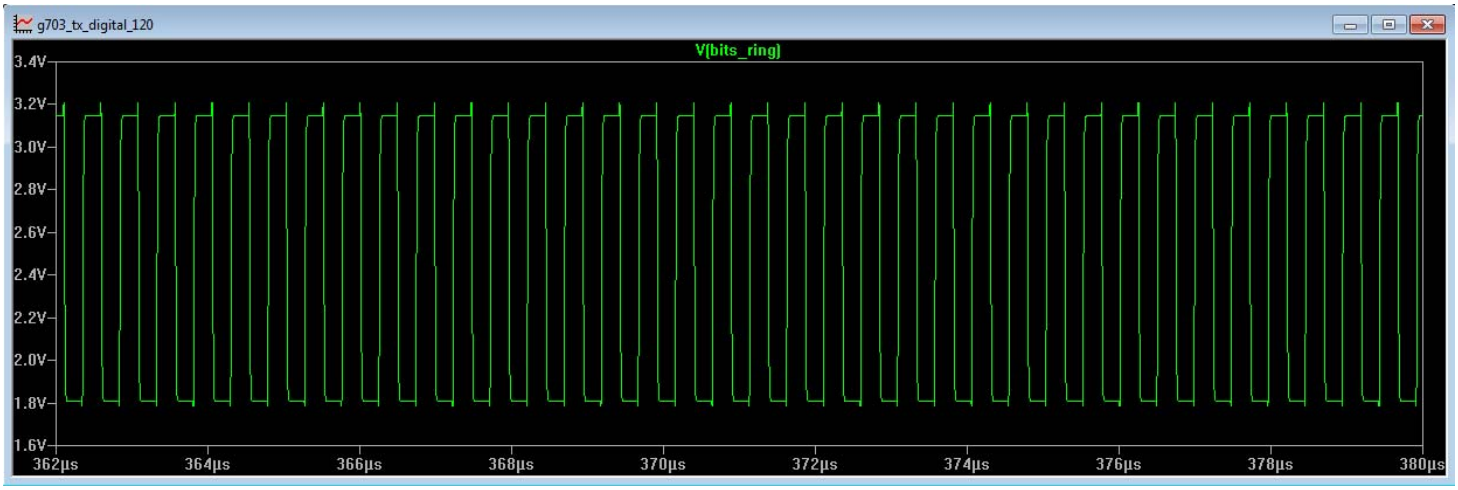


Figure 3 shows the lower transmitted pulse amplitude with transistor power supply of 2.5V. In this condition, total signal amplitude is close to 3.2V with a DC offset 1.8V, leaving the net signal amplitude of about 1.4V, also meeting required signal level (Table 1).

Figure 3. Transmitted Pulses with 2.5V



X1~X4 are 4 analog switches. Any STDP with low Ron can be used. Analog switches are used to isolate the 82V2081's own circuit from external transmitter. When 2.5V is used as the transistor power supply, the transmitted pulses have an overall amplitude of 3.2V, which will not conduct the ESD diodes used in the circuit as a protection diodes. In this condition, X3 and X4 are not needed.

Circuit Implementations

The circuit uses a transistor, a 1:2 transformer and a few analog switches. The transistor used in the example is BSS123. Other transistors can be used with similar specifications. The transformer can be selected from IDT's transformer selection guide AN-377 with a turn ratio of 1:2. R5 is a current-limiting resistor. The power rating for this resistor should be >= 0.1W. R4 is the termination impedance. For 120Ω twisted-pair transmission line, R4 = 30Ω. For 75Ω coax transmission, it is 18.75Ω.

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