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RENESAS

Application Note

78K0S/Kx1+

Sample Program (16-bit Timer/Event Counter 00)

External Event Counter

This document describes an operation overview of the sample program and how to use it, as well as how to set and use the external event counter function of 16-bit timer/event counter 00. In the sample program, the LED output is reversed every fixed time the falling edge of the external pulse input is detected, by using the external event counter function of 16-bit timer/event counter 00.

Target devices

78K0S/KA1+ microcontroller
78K0S/KB1+ microcontroller
78K0S/KU1+ microcontroller
78K0S/KY1+ microcontroller

CONTENTS

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M8E 02. 11-1

CHAPTER 1 OVERVIEW

An example of using the external event counter function of 16-bit timer/event counter 00 is presented in this sample program. The LED output is reversed every 10 times (11 times only for the first reversal) the falling edge of the external pulse input is detected.

1.1 Main Contents of the Initial Settings

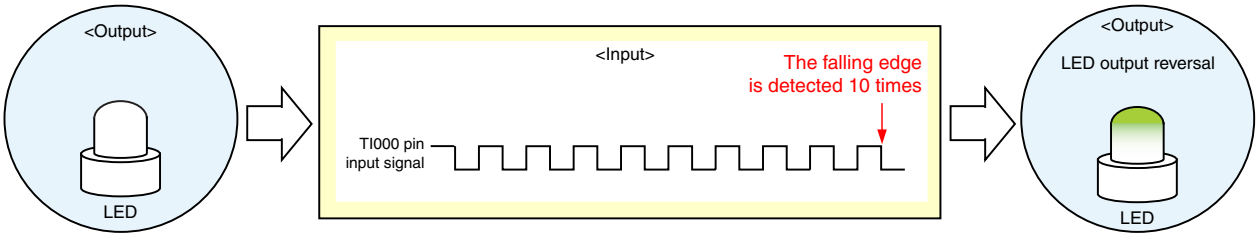
The main contents of the initial settings are as follows.

- Selecting the high-speed internal oscillator as the system clock source[Note]
- Stopping watchdog timer operation
- Setting V_{LVI} (low-voltage detection voltage) to 4.3 V ±0.2 V
- Generating an internal reset (LVI reset) signal when it is detected that V_{DD} is less than V_{LVI}, after V_{DD} (power supply voltage) becomes greater than or equal to V_{LVI}
- Setting the CPU clock frequency to 8 MHz
- Setting the I/O ports
- Setting 16-bit timer/event counter 00
  - Setting CR000 as a compare register
  - Setting the external event counter compare value to CR000
  - Setting the count clock as the valid edge (falling edge) of the TI000 pin
  - Setting the operation mode to clear & start upon a match between TM00 and CR000
- Enabling INTTM000 interrupts

Note This is set by using the option byte.

1.2 Contents Following the Main Loop

The LED output is reversed every 10 times (11 times only for the first reversal) the falling edge of the external pulse input is detected, by using the generation of a 16-bit timer/event counter 00 interrupt (INTTM000), after completion of the initial settings.



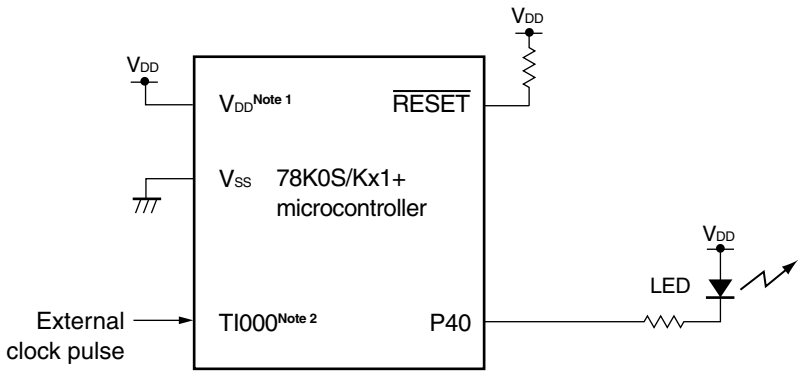
Caution For cautions when using the device, refer to the user's manual of each product (78K0S/KU1+, 78K0S/KY1+, 78K0S/KA1+, 78K0S/KB1+).

CHAPTER 2 CIRCUIT DIAGRAM

This chapter describes a circuit diagram and the peripheral hardware to be used in this sample program.

2.1 Circuit Diagram

A circuit diagram is shown below.



Notes 1. Use this in a voltage range of 4.5 V ≤ V_{DD} ≤ 5.5 V.

2. TI000/INTP0/P30: 78K0S/KA1+ and 78K0S/KB1+ microcontrollers
TI000/ANI0/TOH1/P20: 78K0S/KY1+ and 78K0S/KU1+ microcontrollers

Cautions 1. Connect the AV_{REF} pin directly to V_{DD} (only for the 78K0S/KA1+ and 78K0S/KB1+ microcontrollers).

2. Connect the AV_{SS} pin directly to GND (only for the 78K0S/KB1+ microcontroller).

3. Leave all unused pins open (unconnected), except for the pins shown in the circuit diagram and the AV_{REF} and AV_{SS} pins.

2.2 Peripheral Hardware

The peripheral hardware to be used is shown below.

- **LED**
  An LED is used as an output corresponding to the external event counter function of 16-bit timer/event counter 00.

CHAPTER 3 SOFTWARE

This chapter describes the file configuration of the compressed file to be downloaded, internal peripheral functions of the microcontroller to be used, and initial settings and operation overview of the sample program, and shows a flow chart.

3.1 File Configuration

The following table shows the file configuration of the compressed file to be downloaded.

File Name	Description	Compressed (*.zip) File Included		
				
main.asm (Assembly language version) main.c (C language version)	Source file for hardware initialization processing and main processing of microcontroller	●Note 1	●Note 1	
op.asm	Assembler source file for setting the option byte (sets the system clock source)	●	●	
tm00evc.prw	Work space file for integrated development environment PM+		●	
tm00evc.prj	Project file for integrated development environment PM+		●	
tm00evc.pri tm00evc.prs tm00evc.prm	Project files for system simulator SM+ for 78K0S/Kx1+		●Note 2	
tm00evc0.pnl	I/O panel file for system simulator SM+ for 78K0S/Kx1+ (used for checking peripheral hardware operations)		●Note 2	●
tm00evc0.wvo	Timing chart file for system simulator SM+ for 78K0S/Kx1+ (used for checking waveforms)			●

Notes 1. “main.asm” is included with the assembly language version, and “main.c” with the C language version.

2. These files are not included among the files for the 78K0S/KU1+ microcontroller.

Remark  : Only the source file is included.

 : The files to be used with integrated development environment PM+ and 78K0S/Kx1+ system simulator SM+ are included.

 : The microcontroller operation simulation file to be used with system simulator SM+ for 78K0S/Kx1+ is included.

3.2 Internal Peripheral Functions to Be Used

The following internal peripheral functions of the microcontroller are used in this sample program.

- External event counter function: 16-bit timer/event counter 00
- $V_{DD} < V_{LVI}$ detection: Low-voltage detector (LVI)
- External pulse input: TI000[Note]
- LED output: P40 (output port)

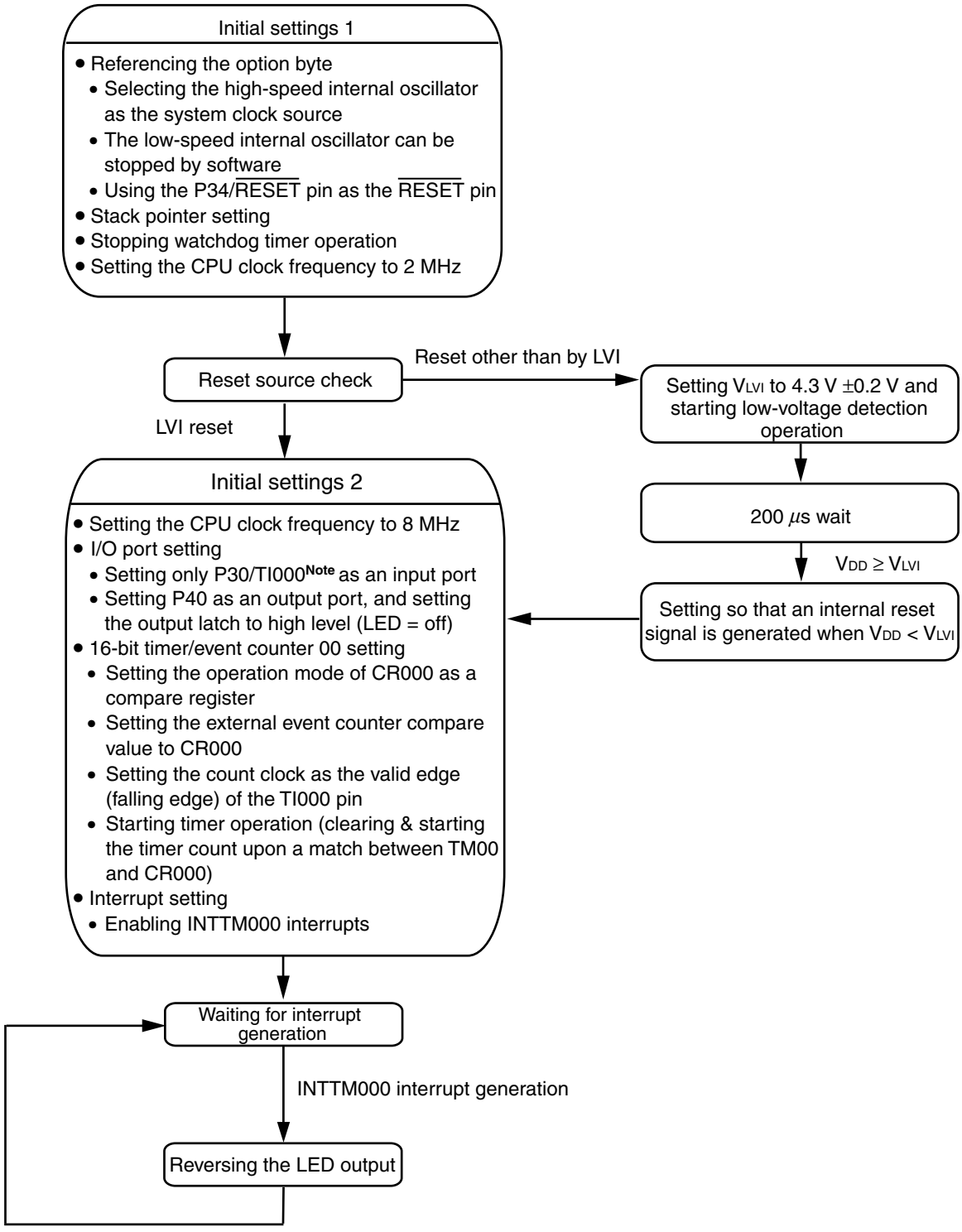
Note TI000/INTP0/P30: 78K0S/KA1+ and 78K0S/KB1+ microcontrollers
TI000/ANI0/TOH1/P20: 78K0S/KY1+ and 78K0S/KU1+ microcontrollers

3.3 Initial Settings and Operation Overview

In this sample program, initial settings including the setting of the low-voltage detection function, selection of the clock frequency, setting of the I/O ports, setting of 16-bit timer/event counter 00 (external event counter function), and setting of interrupts are performed.

The LED output is reversed every 10 times (11 times only for the first reversal) the falling edge of the external pulse input is detected, by using the generation of a 16-bit timer/event counter 00 interrupt (INTTM000), after completion of the initial settings.

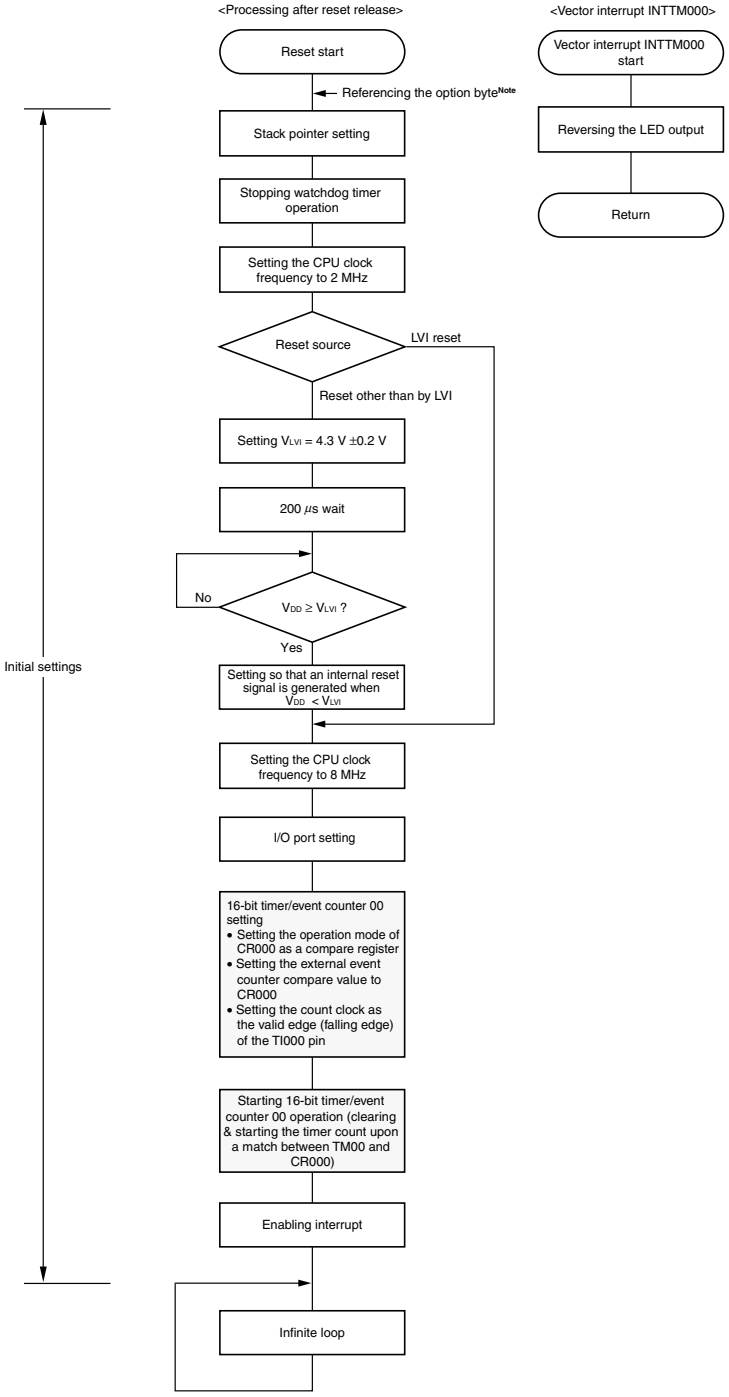
The details are described in the status transition diagram shown below.



Note TI000/P30: 78K0S/KA1+ and 78K0S/KB1+ microcontrollers
TI000/P20: 78K0S/KY1+ and 78K0S/KU1+ microcontrollers

3.4 Flow Charts

The flow charts for the sample program are shown below.



Note Referencing the option byte is automatically performed by the microcontroller after reset release. In this sample program, the following contents are set by referencing the option byte.

- Using the high-speed internal oscillation clock (8 MHz (TYP.)) as the system clock source
- The low-speed internal oscillator can be stopped by using software
- Using the P34/$\overline{\text{RESET}}$ pin as the $\overline{\text{RESET}}$ pin

CHAPTER 4 SETTING METHODS

This chapter describes the external event counter function of 16-bit timer/event counter 00.

For other initial settings, refer to the **78K0S/Kx1+ Sample Program (Initial Settings) LED Lighting Switch Control Application Note**. For interrupt, refer to the **78K0S/Kx1+ Sample Program (Interrupt) External Interrupt Generated by Switch Input Application Note**. For low-voltage detection (LVI), refer to the **78K0S/Kx1+ Sample Program (Low-Voltage Detection) Reset Generation During Detection at Less than 2.7 V Application Note**.

For how to set registers, refer to the user's manual of each product (**78K0S/KU1+**, **78K0S/KY1+**, **78K0S/KA1+**, **78K0S/KB1+**).

For assembler instructions, refer to the **78K/0S Series Instructions User's Manual**.

4.1 Setting the External Event Counter Function of 16-bit Timer/Event Counter 00

When using 16-bit timer/event counter 00 as an external event counter, the valid edge of the external event input (input from the TI000 pin) is counted and an interrupt signal (INTTM000) is generated upon a match between the TM00 counter and CR000 register.

The INTTM000 signal is generated at the following timings.

- INTTM000 signal generation timing (only first time)
  = The number of times the valid edge of the external event input is detected × (CR000 setting value + 2)

- INTTM000 signal generation timing (second and following times)
  = The number of times the valid edge of the external event input is detected × (CR000 setting value + 1)

The valid edge is detected for the first time, when the TI000 pin input signal is sampled at the f_{XP} clock cycle and the valid edge level is detected for two consecutive times. Therefore, noise with a short pulse width can be eliminated.

The following six types of registers are set when using 16-bit timer/event counter 00 as an external event counter.

- Capture/compare control register 00 (CRC00)
- 16-bit timer capture/compare register 000 (CR000)
- Prescaler mode register 00 (PRM00)
- 16-bit timer mode control register 00 (TMC00)
- Port mode register x (PMx)[Note]
- Port mode control register x (PMCx)[Note]

Note Set as follows, because the TI000 pin is used as the timer input when using the external event counter function.

	PMx Register	PMCx Register
78K0S/KA1+ and 78K0S/KB1+ microcontrollers	PM30 = 1	Setting not required
78K0S/KY1+ and 78K0S/KU1+ microcontrollers	PM20 = 1	PMC20 = 0

<Example of the basic operation setting procedure when using 16-bit timer/event counter 00 as an external event counter>

<1> Setting the CRC00 register
<2> Setting an arbitrary value to the CR000 register
<3> Using the PRM00 register to set the count clock as the valid edge of the TI000 pin
<4> Setting the TMC00 register: starting operation

Caution Steps <1> to <3> may be performed randomly.

(1) Setting the CRC00 register

This register controls the operation of the CR000 and CR010 registers.

Caution CR010 is not used when using 16-bit timer/event counter 00 as an external event counter.

Figure 4-1. Format of Capture/Compare Control Register 00 (CRC00)

CRC00

0	0	0	0	0	CRC002	CRC001	CRC000

CR000 operation mode selection

0	Operates as a compare register.
1	Operates as a capture register.

CR000 capture trigger selection

0	Captures at the valid edge of the TI010 pin.
1	Captures at the reverse phase of the valid edge of the TI000 pin.

CR010 operation mode selection

0	Operates as a compare register.
1	Operates as a capture register.

Cautions 1. The timer operation must be stopped before setting the CRC00 register.

2. Do not specify the CR000 register as a capture register when the clear & start mode has been selected upon a match between TM00 and CR000 by using the TMC00 register.

(2) Setting the CR000 register

This register has the functions of both a capture register and a compare register.

Figure 4-2. Format of 16-bit Timer Capture/Compare Register 000 (CR000)

CR000

When using CR000 as a compare register

The value set to CR000 is constantly compared with the 16-bit timer counter 00 (TM00) count value, and an interrupt request (INTTM000) is generated if they match. It can also be used as the register that holds the interval time when TM00 is set to interval timer operation.

- Interval time = (N + 1)/fsam

Cautions 1. Set a value other than 0000H to the CR000 register in the clear & start mode entered on a match between TM00 and CR000.

2. If the new value of the CR000 register is less than the TM00 counter value, TM00 continues counting, overflows, and then starts counting from 0 again. If the new value of the CR000 register is less than the old value, therefore, the timer must be reset and restarted after the CR000 register value is changed.

3. The value of the CR000 register after the TM00 counter has been stopped is not guaranteed.

4. Capture operation may not be performed for the CR000 register set to the compare mode, even if a capture trigger is input.

5. Changing the CR000 register setting during TM00 counter operation may cause a malfunction.

Remark N: CR000 register setting value (0001H to FFFFH)

fsam: TM00 counter count clock frequency

(3) Setting the PRM00 register

This register is used to set the count clock of the TM00 counter and the valid edges of the TI000 and TI010 pin inputs.

Figure 4-3. Format of Prescaler Mode Register 00 (PRM00)

PRM00

ES110	ES100	ES010	ES000	0	0	PRM001	PRM000

Count clock (fsam) selection

0	0	f_{XP}
0	1	$f_{XP}/2^2$
1	0	$f_{XP}/2^8$
1	1	TI000 pin valid edge[Note]

TI000 pin valid edge selection

0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

TI010 pin valid edge selection

0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

Note The external clock requires a pulse longer than two cycles of the internal clock (f_{XP}).

Remark f_{XP}: Oscillation frequency of the clock supplied to peripheral hardware

Cautions 1. Always set data to the PRM00 register after stopping timer operation.

2. When setting the valid edge of the TI000 pin as the count clock, do not set the clear & start mode with the valid edge of the TI000 pin and the TI000 pin as the capture trigger.

3. In the following cases, note with caution that the valid edge of the TI0n0 pin (n = 0, 1) is detected.

<1> A high level is input to the TI0n0 pin and the TM00 operation is enabled immediately after a system reset.

→ If the rising edge or both the rising and falling edges are specified as the valid edge of the TI0n0 pin, a rising edge is detected immediately after the TM00 operation is enabled.

<2> The TM00 operation is stopped while the TI0n0 pin is at high level and it is then enabled after a low level is input to the TI0n0 pin.

→ If the falling edge or both the rising and falling edges are specified as the valid edge of the TI0n0 pin, a falling edge is detected immediately after the TM00 operation is enabled.

<3> The TM00 operation is stopped while the TI0n0 pin is at low level and it is then enabled after a high level is input to the TI0n0 pin.

→ If the rising edge or both the rising and falling edges are specified as the valid edge of the TI0n0 pin, a rising edge is detected immediately after the TM00 operation is enabled.

Cautions 4. To use the valid edge of TI000 with the count clock, it is sampled with f_{XP} to eliminate noise. The capture operation is not performed until the valid edge is sampled and the valid level is detected twice, thus eliminating noise with a short pulse width.

5. When the TI010/TO00/Pxx pin is used as the input pin (TI010) of the valid edge, it cannot be used as a timer output pin (TO00). When it is used as a timer output pin (TO00), it cannot be used as the input pin (TI010) of the valid edge.

(4) Setting the TMC00 register

This register sets the 16-bit timer/event counter 00 operation mode, TM00 counter clear mode, and output timing, and detects overflows.

Figure 4-4. Format of 16-bit Timer Mode Control Register 00 (TMC00)

TMC00

0	0	0	0	TMC003	TMC002	TMC001	OVF00

Overflow detection of 16-bit timer counter 00 (TM00)

0	Overflow not detected.
1	Overflow detected.

			Operation mode and clear mode selection	TO00 inversion timing selection	Interrupt request generation
0	0	0	Operation stop (TM00 cleared to 0)	No change	Not generated
0	0	1			
0	1	0	Free-running mode	Match between TM00 and CR000 or match between TM00 and CR010	<When used as compare register> Generated upon match between TM00 and CR000, or match between TM00 and CR010 <When used as capture register> Generated at valid edge of TI000 pin or TI010 pin
0	1	1		Match between TM00 and CR000, match between TM00 and CR010, or valid edge of TI000 pin	
1	0	0	Clear & start occurs at valid edge of TI000 pin	–	
1	0	1			
1	1	0	Clear & start occurs upon match between TM00 and CR000	Match between TM00 and CR000 or match between TM00 and CR010	
1	1	1		Match between TM00 and CR000, match between TM00 and CR010, or valid edge of TI000 pin	

Cautions 1. The operation of the TM00 counter starts when values other than 0 and 0 (operation stop mode) are set to TMC002 and TMC003, respectively. To stop the operation, set TMC002 and TMC003 to 0 and 0, respectively.

2. Write to the bits other than the OVF00 flag after stopping the timer operation.

3. When the timer is stopped, timer counts and timer interrupts do not occur, even if a signal is input to the TI000/TI010 pin.

4. Except when the valid edge of the TI000 pin is selected as the count clock, stop the timer operation before setting to the STOP mode or system clock stop mode; otherwise the timer may malfunction when the system clock starts.

5. Set the valid edge of the TI000 pin with bits 4 and 5 of the PRM00 register after stopping the timer operation.

6. If the clear & start mode is set upon a match between TM00 and CR000 or at the valid edge of the TI000 pin, or the free-running mode is selected, when the set value of the CR000 register is FFFFH and the TM00 counter value changes from FFFFH to 0000H, the OVF00 flag is set to 1.

7. Even if the OVF00 flag is cleared before the next count clock is counted (before the TM00 counter becomes 0001H) after the TM00 counter overflows, it is re-set and clearing is disabled.

8. Capture operation is performed at the fall of the count clock. An interrupt request (INTTM0n0: n = 0, 1), however, occurs at the rise of the next count clock.

[Example 1] Setting the count clock as the valid edge (falling edge) of the TI000 pin and generating an interrupt when the valid edge is detected for 10 times (11 times for the first interrupt)
(Same contents as in this sample program source)

(1) Register settings

<1> CRC00

0	0	0	0	0	x	x	0

CR000 operation mode selection

0	Operates as a compare register.

CR000 capture trigger selection

x	(Invalid setting because CR000 is used as a compare register.)

CR010 operation mode selection

x	(Does not use CR010.)

<2> CR000
Setting value (N): 9

<3> PRM00

x	x	0	0	0	0	1	1

Count clock (fsam) selection

1	1	TI000 pin valid edge

TI000 pin valid edge selection

0	0	Falling edge

TI010 pin valid edge selection

x	x	(Invalid setting because the TI010 pin is not used. Setting “1, 0”, however, is prohibited.)

<4> TMC00

0	0	0	0	1	1	x	0

Overflow detection of 16-bit timer counter 00 (TM00)

0	Overflow not detected.

			Operation mode and clear mode selection	TO00 inversion timing selection	Interrupt request generation
1	1	0	Clear & start occurs upon match between TM00 and CR000	Match between TM00 and CR000 or match between TM00 and CR010	<When used as compare register> Generated upon match between TM00 and CR000, or match between TM00 and CR010 <When used as capture register> Generated at valid edge of TI000 pin or TI010 pin
1	1	1		Match between TM00 and CR000, match between TM00 and CR010, or valid edge of TI000 pin	

<5> PMX, PMCx

	PMx Register	PMCx Register
78K0S/KA1+ and 78K0S/KB1+ microcontrollers	PM30 = 1	Setting not required
78K0S/KY1+ and 78K0S/KU1+ microcontrollers	PM20 = 1	PMC20 = 0

(2) Sample program

In the example below, “x” in **(1) Register settings** is set to “0”.

<1> Assembly language (when using the 78K0S/KA1+ and 78K0S/KB1+ microcontrollers)

```
SET1   PM3.0
MOV    CRC00, #00000000B
MOVW   CR000, #9
MOV    PRM00, #00000011B
MOV    TMC00, #00001100B
```

<2> C language (when using the 78K0S/KA1+ and 78K0S/KB1+ microcontrollers)

```
PM3.0 = 1;
CRC00 = 0b00000000;
CR000 = 9;
PRM00 = 0b00000011;
TMC00 = 0b00001100;
```

[Example 2] Setting the count clock as the valid edge (both rising and falling edges) of the TI000 pin and generating an interrupt when the valid edge is detected for 100 times (101 times for the first interrupt)

(1) Register settings

<1> CRC00

0	0	0	0	0	x	x	0

CR000 operation mode selection

0	Operates as a compare register.

CR000 capture trigger selection

x	(Invalid setting because CR000 is used as a compare register.)

CR010 operation mode selection

x	(Does not use CR010.)

<2> CR000

Setting value (N): 99

<3> PRM00

x	x	1	1	0	0	1	1

Count clock (fsam) selection

1	1	TI000 pin valid edge

TI000 pin valid edge selection

1	1	Both rising and falling edges

TI010 pin valid edge selection

x	x	(Invalid setting because the TI010 pin is not used. Setting “1, 0”, however, is prohibited.)

<4> TMC00

0	0	0	0	1	1	x	0

Overflow detection of 16-bit timer counter 00 (TM00)

0	Overflow not detected.

			Operation mode and clear mode selection	TO00 inversion timing selection	Interrupt request generation
1	1	0	Clear & start occurs upon match between TM00 and CR000	Match between TM00 and CR000 or match between TM00 and CR010	<When used as compare register> Generated upon match between TM00 and CR000, or match between TM00 and CR010 <When used as capture register> Generated at valid edge of TI000 pin or TI010 pin
1	1	1		Match between TM00 and CR000, match between TM00 and CR010, or valid edge of TI000 pin	

<5> PMx, PMCx

	PMx Register	PMCx Register
78K0S/KA1+ and 78K0S/KB1+ microcontrollers	PM30 = 1	Setting not required
78K0S/KY1+ and 78K0S/KU1+ microcontrollers	PM20 = 1	PMC20 = 0

(2) Sample program

In the example below, “x” in **(1) Register settings** is set to “0”.

<1> Assembly language (when using the 78K0S/KA1+ and 78K0S/KB1+ microcontrollers)

```
SET1   PM3.0
MOV    CRC00, #00000000B
MOVW   CR000, #99
MOV    PRM00, #00110011B
MOV    TMC00, #00001100B
```

<2> C language (when using the 78K0S/KA1+ and 78K0S/KB1+ microcontrollers)

```
PM3.0 = 1;
CRC00 = 0b00000000;
CR000 = 99;
PRM00 = 0b00110011;
TMC00 = 0b00001100;
```

[Excerpt from this sample program source]

An excerpt from **APPENDIX A PROGRAM LIST**, which is related to the 16-bit timer/event counter 00 function, is shown below (same contents as in [**Example 1**] mentioned above).

(1) Assembly language

```
EVENTCNT     EQU    10            ; Timer 00 external event counter compare value
                    •
                    •
                    •
XMAIN  CSEG   UNIT
RESET_START:
                    •
                    •
                    •
       MOV    CRC00, #00000000B   ; Use CR000 as a compare register
       MOVW   AX,    #EVENTCNT-1  ; Set the compare value
       MOVW   CR000, AX           ; Set the compare value
       MOV    PRM00, #00000011B   ; Set the count clock as the falling edge of the
TI000 pin
       MOV    TOC00, #00000000B   ; Do not perform timer output
       MOV    TMC00, #00001100B   ; Start the timer operation (clear & start upon a
match between TM00 and CR000)

       MOV    IF0,   #00H         ; Clear invalid interrupt requests in advance
       CLR1   TMMK000             ; Unmask INTTM000 interrupts

       EI                         ; Enable vector interrupt

MAIN_LOOP:
       NOP
       BR     $MAIN_LOOP          ; Go to the MAIN_LOOP

INTERRUPT_TM000:
       XOR    P4,    #00000001B   ; Reverse the LED output
       RETI                       ; Return from interrupt servicing

end
```

Setting the external event counter compare value

Setting the operation mode of CR000 as a compare register

Setting the count clock

Starting timer operation

Clearing the INTTM000 interrupt request flag

Enabling INTTM000 interrupt servicing

Starting interrupt servicing by INTTM000 interrupt generation

(2) C language

```
#define eventCnt 10                 /* Timer 00 external event counter compare value */
                    •
                    •
                    •
void hdwinit(void){
      unsigned char ucCnt200us;     /* 8-bit variable for 200 us wait */
                    •
                    •
                    •
      CRC00 = 0b00000000;           /* Use CR000 as a compare register */
      CR000 = eventCnt-1;           /* Initialize the compare value */
      PRM00 = 0b00000011;           /* Set the count clock as the falling edge of the
TI000 pin */
      TOC00 = 0b00000000;           /* Do not perform timer output */
      TMC00 = 0b00001100;           /* Start the timer operation (clear & start upon a
match between TM00 and CR000) */


      IF0   = 0x00;                 /* Clear invalid interrupt requests in advance */
      TMMK000 = 0;                  /* Unmask INTTM000 interrupts */
      return;
}

void main(void){

      EI();                         /* Enable vector interrupt */

      while (1){
            NOP();
            NOP();
      }
}

__interrupt void fn_inttm000(){

      P4 ^= 0b00000001;             /* Reverse the LED output */

      return;
}
```

Setting the external event counter compare value

Setting the operation mode of CR000 as a compare register

Setting the count clock

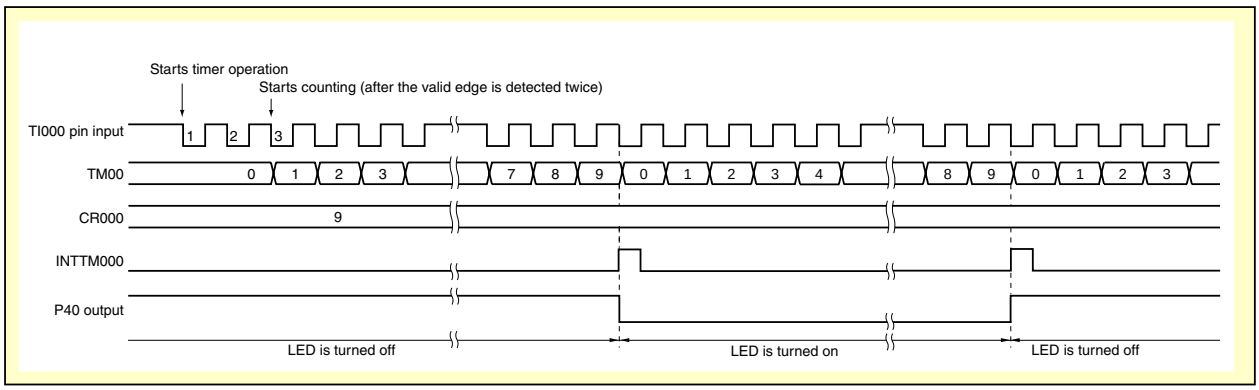
Starting timer operation

Clearing the INTTM000 interrupt request flag

Enabling INTTM000 interrupt servicing

Starting interrupt servicing by INTTM000 interrupt generation

Figure 4-5. External Event Counter Operation Timing Chart Example (in the Case of This Sample Program Source)



CHAPTER 5 OPERATION CHECK USING SYSTEM SIMULATOR SM+

This chapter describes how the sample program operates with system simulator SM+ for 78K0S/Kx1+, by using the assembly language file (source files + project file) that has been downloaded by selecting the  icon.

<R> **Caution System simulator SM+ for 78K0S/Kx1+ is not supported with the 78K0S/KU1+ microcontroller (as of July 2008). The operation of the 78K0S/KU1+ microcontroller, therefore, cannot be checked by using system simulator SM+ for 78K0S/Kx1+.**

<R> 5.1 Building the Sample Program

To check the operation of the sample program by using system simulator SM+ for 78K0S/Kx1+ (hereinafter referred to as “SM+”), SM+ must be started after building the sample program. This section describes how to build a sample program by using the assembly language sample program (source program + project file) downloaded by clicking the  icon. See the **78K0S/Kx1+ Sample Program Startup Guide Application Note** for how to build other downloaded programs.

For the details of how to operate PM+, refer to the **PM+ Project Manager User’s Manual**.

[Column] Build errors

Change the compiler option setting according to the following procedure when the error message “A006 File not found ‘C:\NECTOOLS32\LIB78K0S\s0sl.rel’” or “*** ERROR F206 Segment ‘@@DATA’ can’t allocate to memory - ignored.” is displayed, when building with PM+.

<1> Select [Compiler Options] from the [Tool] menu.
<2> The [Compiler Options] dialog box will be displayed. Select the [Startup Routine] tab.
<3> Uncheck the [Using Fixed Area of Standard Library] check box. (Leave the other check boxes as they are.)

A RAM area of 118 bytes that has been secured as a fixed standard library area will be enabled for use when the [Using Fixed Area of Standard Library] check box is unchecked; however, the standard libraries (such as the getchar function and malloc function) will be disabled for use.

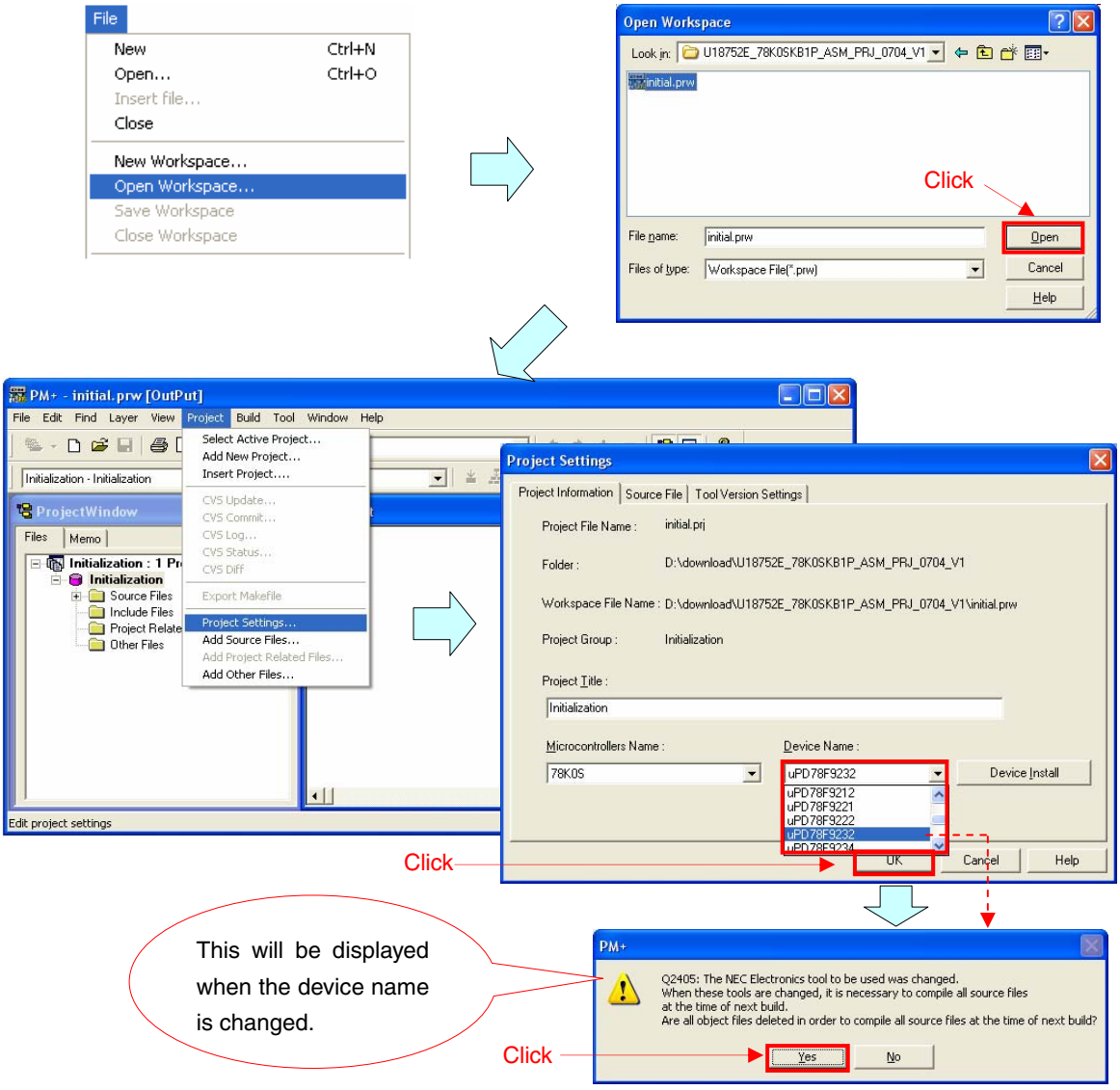
The [Using Fixed Area of Standard Library] check box is unchecked by default when the file that has been downloaded by clicking the  icon is used in this sample program.

(1) Start PM+.

(2) Select “tm00evc.prw” by clicking [Open Workspace] from the [File] menu and click [Open]. A workspace into which the source file will be automatically read will be created.

(3) Select [Project Settings] from the [Project] menu. When the [Project Settings] window opens, select the name of the device to be used (the device with the largest ROM or RAM size will be selected by default), and click [OK].

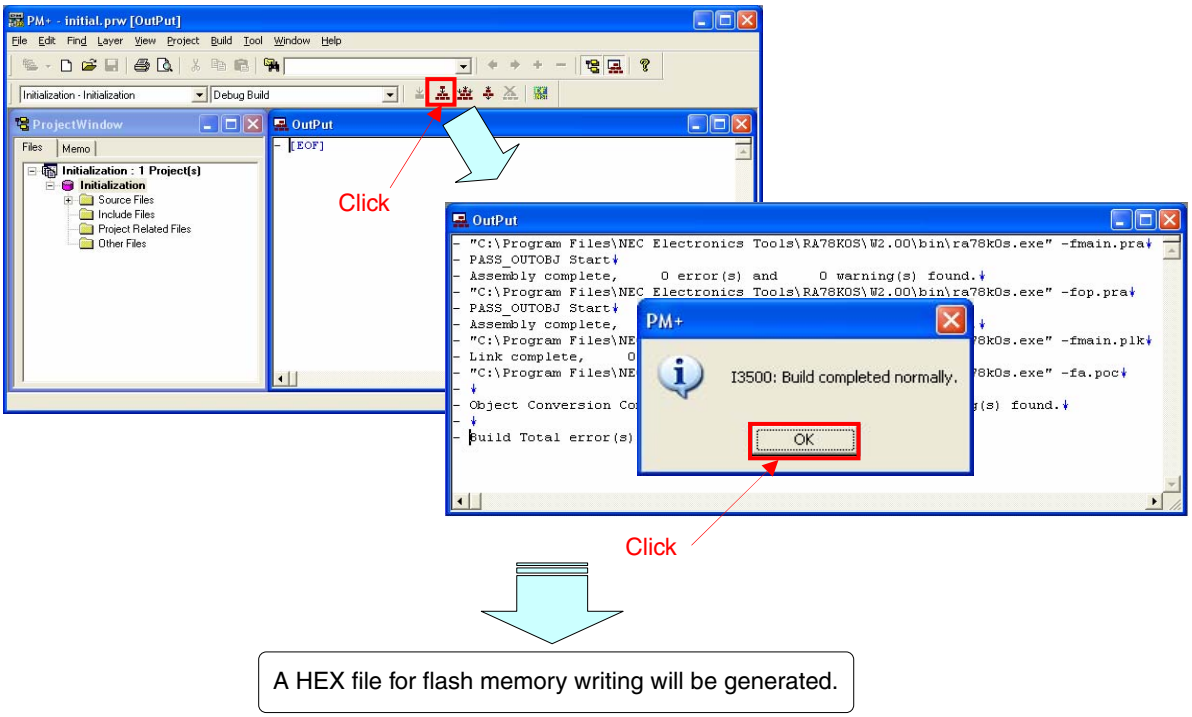
Remark Screenshots of the Sample Program (Initial Settings) LED Lighting Switch Control are shown below.



(4) Click  ([Build] button). When the source files are built normally, the message “I3500: Build completed normally.” will be displayed.

(5) Click the [OK] button in the message dialog box. A HEX file for flash memory writing will be created.

Remark Screenshots of the Sample Program (Initial Settings) LED Lighting Switch Control are shown below.



5.2 Operation with SM+

This section describes examples of checking the operation on the I/O panel window or timing chart window of SM+. For the details of how to operate SM+, refer to the **SM+ System Simulator Operation User’s Manual**.

<R> (1) When SM+ for 78K0S/Kx1+ W1.02 (“SM+” hereafter) is used in the environment of PM+ Ver. 6.30, SM+ cannot be selected as the debugger. In this case, start SM+ via method (a) or (b) described below, while keeping PM+ running after completing building a project.

(a) When starting SM+ in PM+

<1> Select [Register Ex-tool] from the [Tool] menu and register “SM+ for 78K0S/Kx1+”.

<2> Select [Ex-tool Bar] from the [View] menu and add the SM+ icon to the PM+ toolbar.

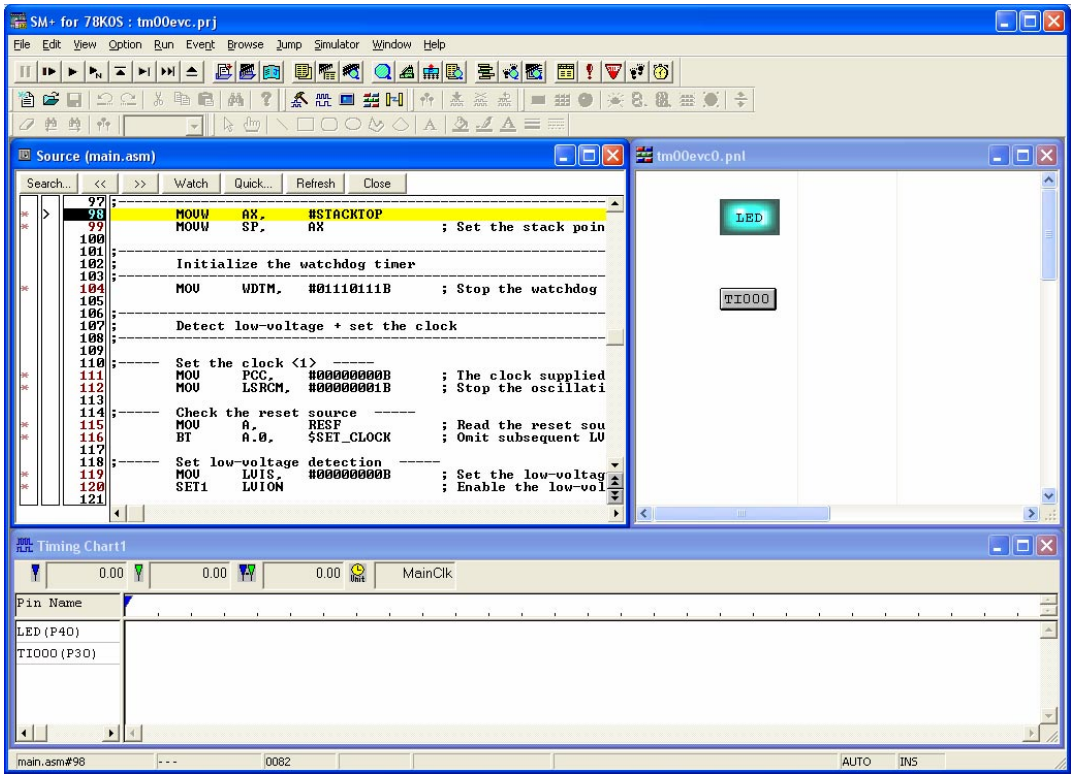
<3> Click the SM+ icon and start SM+.

(See the PM+ help for details on how to register external tools.)

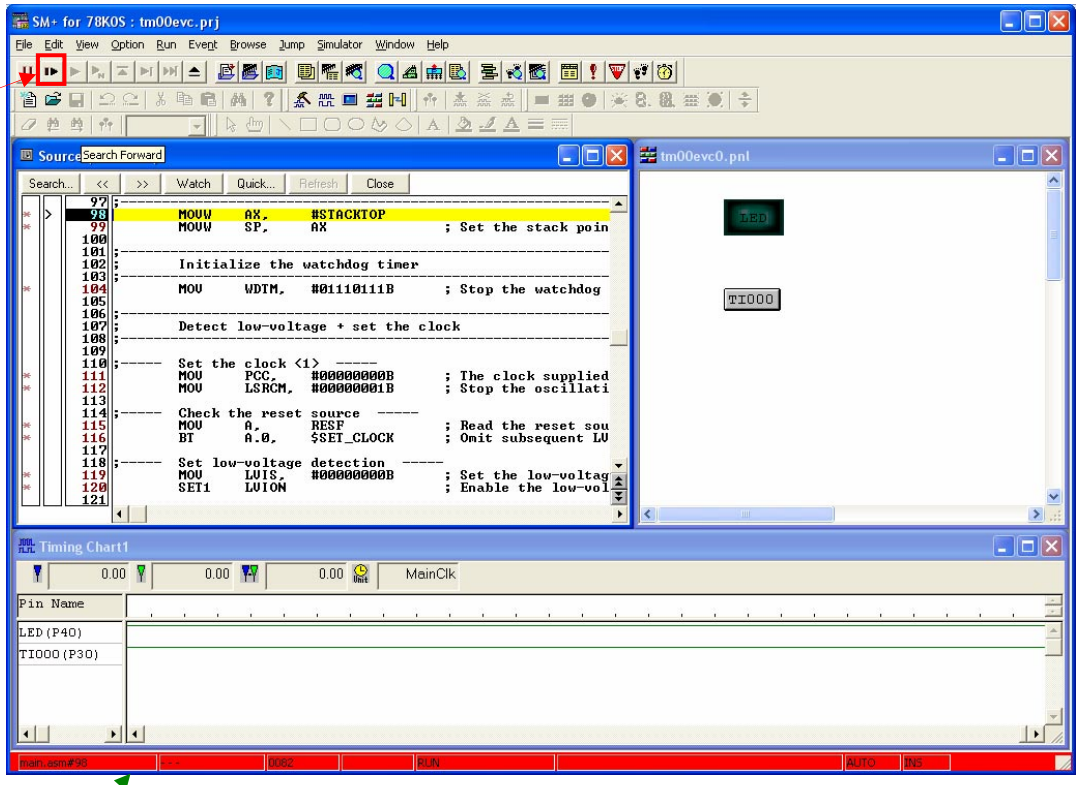
(b) When not starting SM+ in PM+

•Start SM+ from the Windows start menu.

(2) The following screen will be displayed when SM+ is started. (This is a sample screenshot of when an assembly language source file downloaded by clicking the  icon was used.)

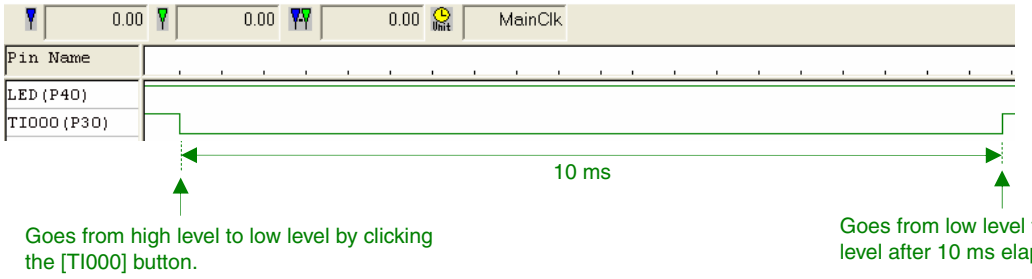


(3) Click  ([Restart] button). The program will be executed after the CPU is reset and the following screen will be displayed.

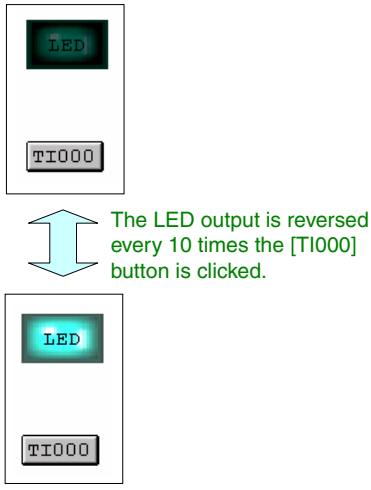
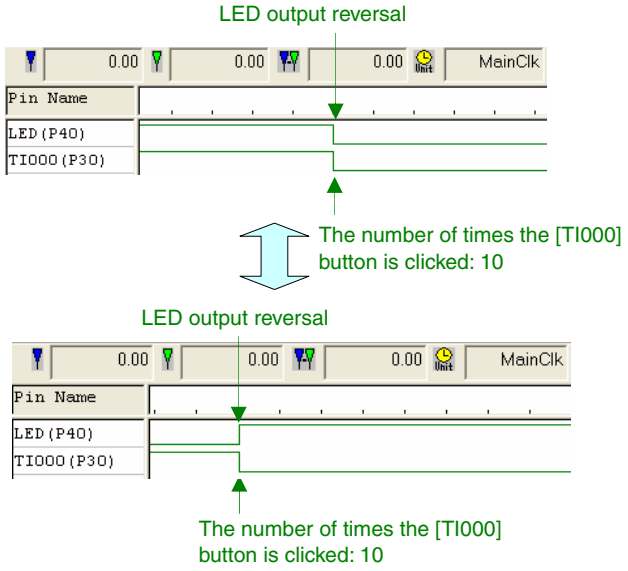


(4) Click the [TI000] button in the I/O panel window, during program execution.
The waveform of TI000 is as follows when the [TI000] button is clicked.

Timing Chart Window



Check that, by clicking the [TI000] button 10 times, the valid edge (falling edge) is detected for 10 times[Note], and the [LED] output in the I/O panel window and the LED waveform displayed in the timing chart window are reversed.

I/O Panel Window	Timing Chart Window
	

Note With an actual device, only the first LED output reversal takes place when the valid edge (falling edge) of the TI000 pin is detected for 11 times. (The second and following LED output reversals take place when the valid edge is detected for 10 times.)

CHAPTER 6 RELATED DOCUMENTS

<R>

Document Name			Japanese/English
78K0S/KU1+ User's Manual			PDF
78K0S/KY1+ User's Manual			PDF
78K0S/KA1+ User's Manual			PDF
78K0S/KB1+ User's Manual			PDF
78K/0S Series Instructions User's Manual			PDF
RA78K0S Assembler Package User's Manual		Language	PDF
		Operation	PDF
CC78K0S C Compiler User's Manual		Language	PDF
		Operation	PDF
PM+ Project Manager User's Manual			PDF
SM+ System Simulator Operation User's Manual			PDF
Flash Programming Manual (Basic) MINICUBE2 version		78K0S/KU1+	PDF
		78K0S/KY1+	PDF
		78K0S/KA1+	PDF
		78K0S/KB1+	PDF
78K0S/Kx1+ Application Note	Sample Program Startup Guide		PDF
	Sample Program (Initial Settings) LED Lighting Switch Control		PDF
	Sample Program (Interrupt) External Interrupt Generated by Switch Input		PDF
	Sample Program (Low-Voltage Detection) Reset Generation During Detection at Less than 2.7 V		PDF
	Sample Program (16-bit Timer/Event Counter 00) Interval Timer		PDF
	Sample Program (16-bit Timer/Event Counter 00) Pulse Width Measurement		PDF
	Sample Program (16-bit Timer/Event Counter 00) PPG Output		PDF
	Sample Program (16-bit Timer/Event Counter 00) One-Shot Pulse Output		PDF

APPENDIX A PROGRAM LIST

As a program list example, the 78K0S/KB1+ microcontroller source program is shown below.

● main.asm (Assembly language version)

```
  ;*******************************************************************************
  ;
  ;   NEC Electronics     78K0S/KB1+
  ;
  ;*******************************************************************************
  ;   78K0S/KB1+  Sample program
  ;*******************************************************************************
  ;   16-bit timer 00 (external event counter)
  ;*******************************************************************************
  ;<<History>>
  ;   2007.7.--   Release
  ;*******************************************************************************
  ;
  ;<<Overview>>
  ;
  ;This sample program presents an example of using the external event counter
  ;function of 16-bit timer 00.  The LED output is reversed by generating an
  ;interrupt every 10 times the falling edge of the external clock pulse input
  ;to the TI000 pin is counted.
  ;
  ;
  ;  <Principal setting contents>
  ;
  ;  - Stop the watchdog timer operation
  ;  - Set the low-voltage detection voltage (VLVI) to 4.3 V +-0.2 V
  ;   - Generate an internal reset signal (low-voltage detector) when VDD <
VLVI after VDD >= VLVI
  ;  - Set the CPU clock to 8 MHz
  ;  - Set the clock supplied to the peripheral hardware to 8 MHz
  ;
  ;
  ;  <16-bit timer 00 settings>
  ;  - Operation mode: Clear & start the timer count upon a match between TM00
and CR000
  ;  - Not performing timer output
  ;  - Setting the count clock to the falling edge of the TI000 pin
  ;  - Setting the counter compare value to 10
  ;
  ;
  ;<<I/O port settings>>
  ;
```

```
;  Input: P30
;  Output: P00-P03, P20-P23, P31-P33, P40-P47, P120-P123, P130
;  # All unused ports are set as the output mode.
;
;************************************************************************


;========================================================================
;
;   Define the symbol
;
;========================================================================
EVENTCNT  EQU   10          ; Timer 00 external event counter compare value

;========================================================================
;
;   Vector table
;
;========================================================================
XVCTCSEG  AT    0000H
    DW    RESET_START       ;(00) RESET
    DW    RESET_START       ;(02) --
    DW    RESET_START       ;(04) --
    DW    RESET_START       ;(06) INTLVI
    DW    RESET_START       ;(08) INTP0
    DW    RESET_START       ;(0A) INTP1
    DW    RESET_START       ;(0C) INTTMH1
    DW    INTERRUPT_TM000   ;(0E) INTTM000
    DW    RESET_START       ;(10) INTTM010
    DW    RESET_START       ;(12) INTAD
    DW    RESET_START       ;(14) --
    DW    RESET_START       ;(16) INTP2
    DW    RESET_START       ;(18) INTP3
    DW    RESET_START       ;(1A) INTTM80
    DW    RESET_START       ;(1C) INTSRE6
    DW    RESET_START       ;(1E) INTSR6
    DW    RESET_START       ;(20) INTST6

;========================================================================
;
;   Define the memory stack area
;
;========================================================================
XSTKDSEG  AT    0FEE0H
STACKEND:
    DS    20H               ; Memory stack area = 32 bytes
STACKTOP:                   ; Start address of the memory stack area = FF00H
```

```
;*****************************************************************************
;
;   Initialization after RESET
;
;*****************************************************************************
XMAIN     CSEG  UNIT
RESET_START:
;-----------------------------------------------------------------------------
;   Initialize the stack pointer
;-----------------------------------------------------------------------------
    MOVW  AX,   #STACKTOP
    MOVW  SP,   AX          ; Set the stack pointer

;-----------------------------------------------------------------------------
;   Initialize the watchdog timer
;-----------------------------------------------------------------------------
    MOV   WDTM, #01110111B  ; Stop the watchdog timer operation

;-----------------------------------------------------------------------------
;   Detect low-voltage + set the clock
;-----------------------------------------------------------------------------

;-----  Set the clock <1>  -----
    MOV   PCC,  #00000000B ; The clock supplied to the CPU (fcpu) = fxp (=
fx/4 = 2 MHz)
    MOV   LSRCM,#00000001B ; Stop the oscillation of the low-speed internal
oscillator

;-----  Check the reset source  -----
    MOV   A,    RESF        ; Read the reset source
    BT    A.0,  $SET_CLOCK  ; Omit subsequent LVI-related processing and go
to SET_CLOCK during LVI reset

;-----  Set low-voltage detection  -----
    MOV   LVIS, #00000000B  ; Set the low-voltage detection level (VLVI) to
4.3 V +-0.2 V
    SET1  LVION             ; Enable the low-voltage detector operation

    MOV   A,    #40         ; Assign the 200 us wait count value
;-----  200 us wait  -----
WAIT_200US:
    DEC   A
    BNZ   $WAIT_200US       ; 0.5[us/clk] x 10[clk] x 40[count] = 200[us]

;-----  VDD >= VLVI wait processing  -----
WAIT_LVI:
    NOP
    BT    LVIF, $WAIT_LVI   ; Branch if VDD < VLVI
```

```
      SET1  LVIMD             ;  Set  so  that  an  internal  reset  signal  is
generated when VDD < VLVI

  ;-----  Set the clock <2>  -----
  SET_CLOCK:
      MOV   PPCC, #00000000B  ; The clock supplied to the peripheral hardware
(fxp) = fx (= 8 MHz)
                              ;  -> The clock supplied to the CPU (fcpu) = fxp
= 8 MHz

  ;---------------------------------------------------------------------------
  ;   Initialize the port 0
  ;---------------------------------------------------------------------------
      MOV   P0,   #00000000B  ; Set output latches of P00-P03 as low
      MOV   PM0,  #11110000B  ; Set P00-P03 as output mode

  ;---------------------------------------------------------------------------
  ;   Initialize the port 2
  ;---------------------------------------------------------------------------
      MOV   P2,   #00000000B  ; Set output latches of P20-P23 as low
      MOV   PM2,  #11110000B  ; Set P20-P23 as output mode

  ;---------------------------------------------------------------------------
  ;   Initialize the port 3
  ;---------------------------------------------------------------------------
      MOV   P3,   #00000000B  ; Set output latches of P30-P33 as low
      MOV   PM3,  #11110001B  ; Set P31-P33 as output mode, P30/TI000 as input
mode

  ;---------------------------------------------------------------------------
  ;   Initialize the port 4
  ;---------------------------------------------------------------------------
      MOV   P4,   #00000001B  ; Set output latches of P41-P47 as low, P40 as
high (turn off LED)
      MOV   PM4,  #00000000B  ; Set P40-P47 as output mode

  ;---------------------------------------------------------------------------
  ;   Initialize the port 12
  ;---------------------------------------------------------------------------
      MOV   P12,  #00000000B  ; Set output latches of P120-P123 as low
      MOV   PM12, #11110000B  ; Set P120-P123 as output mode

  ;---------------------------------------------------------------------------
  ;   Initialize the port 13
  ;---------------------------------------------------------------------------
      MOV   P13,  #00000001B  ; Set output latch of P130 as high
```

```
  ;-------------------------------------------------------------------------
  ;   Set 16-bit timer 00
  ;-------------------------------------------------------------------------
      MOV   CRC00,      #00000000B  ; Use CR000 as a compare register
      MOVW  AX,         #EVENTCNT-1 ; Set the compare value
      MOVW  CR000,      AX          ; Set the compare value
      MOV   PRM00,      #00000011B  ; Set the count clock as the falling edge
of the TI000 pin
      MOV   TOC00,      #00000000B  ; Do not perform timer output
      MOV   TMC00,      #00001100B  ; Start the timer operation (clear & start
upon a match between TM00 and CR000)

  ;-------------------------------------------------------------------------
  ;   Set the interrupt
  ;-------------------------------------------------------------------------
      MOV   IF0,  #00H              ;  Clear  invalid  interrupt  requests  in
advance
      CLR1  TMMK000                 ; Unmask INTTM000 interrupts

      EI                            ; Enable vector interrupt

  ;*************************************************************************
  ;
  ;   Main loop
  ;
  ;*************************************************************************
  MAIN_LOOP:
      NOP
      BR    $MAIN_LOOP              ; Go to the MAIN_LOOP

  ;*************************************************************************
  ;
  ;   Interrupt INTTM000
  ;
  ;*************************************************************************
  INTERRUPT_TM000:
      XOR   P4,   #00000001B        ; Reverse the LED output
      RETI                          ; Return from interrupt servicing

  end
```

● main.c (C language version)

```
/************************************************************************

    NEC Electronics     78K0S/KB1+

************************************************************************
    78K0S/KB1+  Sample program
************************************************************************
    16-bit timer 00 (external event counter)
************************************************************************
<<History>>
    2007.7.--   Release
************************************************************************

<<Overview>>

This sample program presents an example of using the external event counter
function of 16-bit timer 00.  The LED output is reversed by generating an
interrupt every 10 times the falling edge of the external clock pulse input
to the TI000 pin is counted.


  <Principal setting contents>

  - Declare a function run by an interrupt: INTTM000 -> fn_inttm000()
  - Stop the watchdog timer operation
  - Set the low-voltage detection voltage (VLVI) to 4.3 V +-0.2 V
  - Generate an internal reset signal (low-voltage detector) when VDD < VLVI
after VDD >= VLVI
  - Set the CPU clock to 8 MHz
  - Set the clock supplied to the peripheral hardware to 8 MHz


  <16-bit timer 00 settings>
  - Operation mode: Clear & start the timer count upon a match between TM00
and CR000
  - Not performing timer output
  - Setting the count clock to the falling edge of the TI000 pin
  - Setting the counter compare value to 10


<<I/O port settings>>

  Input: P30
  Output: P00-P03, P20-P23, P31-P33, P40-P47, P120-P123, P130
  # All unused ports are set as the output mode.
```

```
  ************************************************************************/


  /*=======================================================================

      Preprocessing directive (#pragma)

  =======================================================================*/
  #pragma   SFR                    /* SFR names can be described at the C
source level */
  #pragma   EI                     /* EI instructions can be described at the
C source level */
  #pragma   NOP                    /* NOP instructions can be described at
the C source level */
  #pragma interrupt INTTM000 fn_inttm000  /*        Interrupt        function
declaration:INTTM000 */

  #define eventCnt 10              /* Timer 00 external event counter compare
value */

  /************************************************************************

      Initialization after RESET

  ************************************************************************/
  void hdwinit(void){
      unsigned char ucCnt200us;     /* 8-bit variable for 200 us wait */

  /*-----------------------------------------------------------------------
      Initialize the watchdog timer + detect low-voltage + set the clock
  -----------------------------------------------------------------------*/
      /* Initialize the watchdog timer */
      WDTM  = 0b01110111;           /* Stop the watchdog timer operation */

      /* Set the clock <1> */
      PCC   = 0b00000000;           /* The clock supplied to the CPU (fcpu) =
fxp (= fx/4 = 2 MHz) */
      LSRCM = 0b00000001;           /* Stop the oscillation of the low-speed
internal oscillator */

      /* Check the reset source */
      if (!(RESF & 0b00000001)){    /* Omit subsequent LVI-related processing
during LVI reset */

            /* Set low-voltage detection */
            LVIS  = 0b00000000;     /*  Set  the  low-voltage  detection  level
(VLVI) to 4.3 V +-0.2 V */
```

```
            LVION = 1;              /*   Enable   the   low-voltage   detector
operation */

            for (ucCnt200us = 0; ucCnt200us < 9; ucCnt200us++){   /*  Wait  of
about 200 us */
                  NOP();
            }

            while (LVIF){           /* Wait for VDD >= VLVI */
                  NOP();
            }

            LVIMD = 1;              /* Set so that an internal reset signal is
generated when VDD < VLVI */
      }

      /* Set the clock <2> */
      PPCC  = 0b00000000;           /*  The  clock  supplied  to  the  peripheral
hardware (fxp) = fx (= 8 MHz)
                                        ->  The  clock  supplied  to  the  CPU
(fcpu) = fxp = 8 MHz */

  /*-------------------------------------------------------------------------
      Initialize the port 0
  -------------------------------------------------------------------------*/
      P0    = 0b00000000;           /* Set output latches of P00-P03 as low */
      PM0   = 0b11110000;           /* Set P00-P03 as output mode */

  /*-------------------------------------------------------------------------
      Initialize the port 2
  -------------------------------------------------------------------------*/
      P2    = 0b00000000;           /* Set output latches of P20-P23 as low */
      PM2   = 0b11110000;           /* Set P20-P23 as output mode */

  /*-------------------------------------------------------------------------
      Initialize the port 3
  -------------------------------------------------------------------------*/
      P3    = 0b00000000;           /* Set output latches of P30-P33 as low */
      PM3   = 0b11110001;           /*  Set  P31-P33  as  output  mode,  P30/TI000
as input mode */

  /*-------------------------------------------------------------------------
      Initialize the port 4
  -------------------------------------------------------------------------*/
      P4    = 0b00000001;           /*  Set  output  latches  of  P41-P47  as  low,
P40 as high (turn off LED) */
      PM4   = 0b00000000;           /* Set P40-P47 as output mode */
```

```
  /*---------------------------------------------------------------------------
      Initialize the port 12
  ---------------------------------------------------------------------------*/
      P12   = 0b00000000;           /* Set output latches of P120-P123 as low
*/
      PM12  = 0b11110000;           /* Set P120-P123 as output mode */

  /*---------------------------------------------------------------------------
      Initialize the port 13
  ---------------------------------------------------------------------------*/
      P13   = 0b00000001;           /* Set output latch of P130 as high */

  /*---------------------------------------------------------------------------
      Set 16-bit timer 00
  ---------------------------------------------------------------------------*/
      CRC00 = 0b00000000;           /* Use CR000 as a compare register */
      CR000 = eventCnt-1;           /* Initialize the compare value */
      PRM00 = 0b00000011;           /* Set the count clock as the falling edge
of the TI000 pin */
      TOC00 = 0b00000000;           /* Do not perform timer output */
      TMC00 = 0b00001100;           /*  Start  the  timer  operation  (clear  &
start upon a match between TM00 and CR000) */

  /*---------------------------------------------------------------------------
      Set the interrupt
  ---------------------------------------------------------------------------*/
      IF0   = 0x00;                 /*  Clear  invalid  interrupt  requests  in
advance */
      TMMK000 = 0;                  /* Unmask INTTM000 interrupts */

      return;
  }

  /****************************************************************************

      Main loop

  ****************************************************************************/
  void main(void){

      EI();                         /* Enable vector interrupt */

      while (1){
            NOP();
            NOP();
      }
  }
```

```
  /************************************************************************

      Interrupt INTTM000

  ************************************************************************/
  __interrupt void fn_inttm000(){

      P4 ^= 0b00000001;       /* Reverse the LED output */

      return;
  }
```

● op.asm (Common to assembly language and C language versions)

```
;=========================================================================
;
;     Option byte
;
;=========================================================================
OPBT       CSEG     AT     0080H
        DB        10011100B       ; Option byte area
;                     ||||
;                     |||+---------- Low-speed  internal  oscillator  can  be
stopped by software
;                     |++---------- High-speed internal oscillation clock (8
MHz) is selected for system clock source
;                     +------------ P34/RESET pin is used as RESET pin

        DB        11111111B       ; Protect   byte   area   (for   the   self
programming mode)
;                 ||||||||
;                 ++++++++---------- All blocks can be written or erased

end
```

APPENDIX B REVISION HISTORY

The mark “<R>” shows major revised points. The revised points can be easily searched by copying an “<R>” in the PDF file and specifying it in the “Find what.” field.

Edition	Date Published	Page	Revision
1st edition	December 2007	–	–
2nd edition	September 2008	p.22	CHAPTER 5 OPERATION CHECK USING SYSTEM SIMULATOR SM+ • Modification of description in Caution ((as of August 2007) → (as of July 2008))
		pp.22 to 24	Modification of 5.1 Building the Sample Program
		p.24	5.2 Operation with SM+ • Addition of (1)
		p.27	CHAPTER 6 RELATED DOCUMENTS • Addition of Flash Programming Manual (Basic) MINICUBE2 version

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