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RENESAS

Application Note

78K0S/Kx1+

Sample Program (16-bit Timer/Event Counter 00)

Interval Timer

This document describes an operation overview of the sample program and how to use it, as well as how to set and use the interval timer function of 16-bit timer/event counter 00. In the sample program, the LEDs are blinked at fixed cycles by using the interval timer function of 16-bit timer/event counter 00. Furthermore, the blinking cycle of the LEDs is changed in accordance with the number of switch inputs.

Target devices

78K0S/KA1+ microcontroller
78K0S/KB1+ microcontroller
78K0S/KU1+ microcontroller
78K0S/KY1+ microcontroller

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CHAPTER 1 OVERVIEW

An example of using the interval timer function of 16-bit timer/event counter 00 is presented in this sample program. The LEDs are blinked at fixed cycles and the blinking cycle of the LEDs is changed in accordance with the number of switch inputs.

1.1 Main Contents of the Initial Settings

The main contents of the initial settings are as follows.

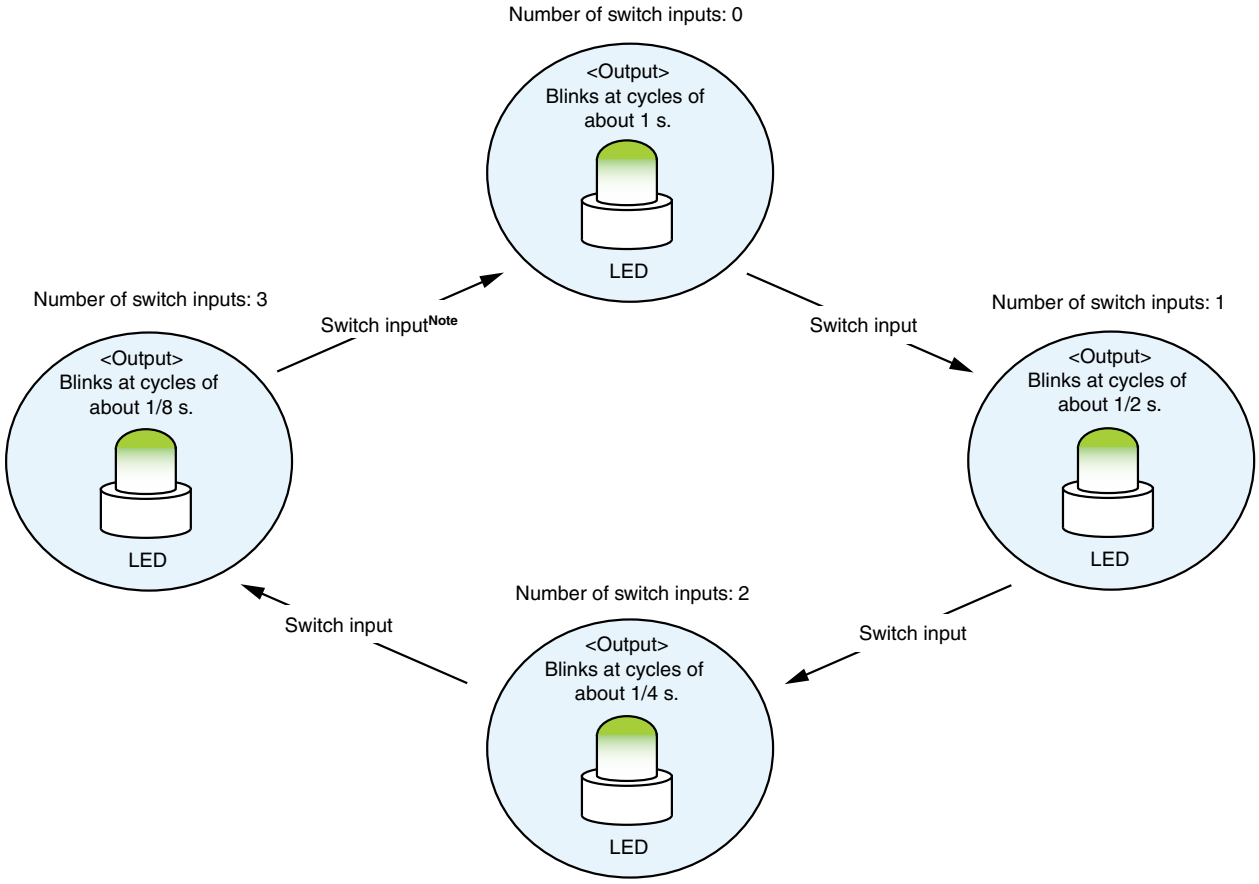
- Selecting the high-speed internal oscillator as the system clock source[Note]
- Stopping watchdog timer operation
- Setting V_{LVI} (low-voltage detection voltage) to 4.3 V ±0.2 V
- Generating an internal reset (LVI reset) signal when it is detected that V_{DD} is less than V_{LVI}, after V_{DD} (power supply voltage) becomes greater than or equal to V_{LVI}
- Setting the CPU clock frequency to 8 MHz
- Setting the I/O ports
- Setting 16-bit timer/event counter 00
  - Setting CR000 as a compare register
  - Setting the interval cycle to about 2 ms (32 μs × 63)
  - Setting the count clock to $f_{XP}/2^8$ (31.25 kHz)
  - Disabling timer output (TO00 pin output)
  - Setting the operation mode to clear & start upon a match between TM00 and CR000
- Setting the valid edge of INTP1 (external interrupt) to the falling edge
- Enabling INTP1 and INTTM000 interrupts

Note This is set by using the option byte.

1.2 Contents Following the Main Loop

The LEDs are blinked at fixed cycles by using the generation of a 16-bit timer/event counter 00 interrupt (INTTM000), after completion of the initial settings.

An INTP1 interrupt is serviced when the falling edge of the INTP1 pin, which is generated by switch input, is detected. Chattering is identified when INTP1 is at high level (switch is off), after 10 ms have elapsed since a fall of the INTP1 pin was detected. The blinking cycle of the LEDs is changed in accordance with the number of switch inputs when INTP1 is at low level (switch is on), after 10 ms have elapsed since an edge was detected.



Note The blinking cycle from the zeroth switch input is repeated after the fourth switch input.

Caution For cautions when using the device, refer to the user's manual of each product (78K0S/KU1+, 78K0S/KY1+, 78K0S/KA1+, 78K0S/KB1+).

[Column] Chattering

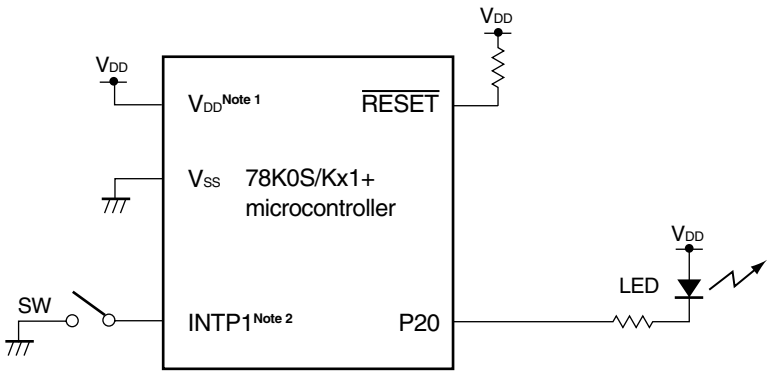
Chattering is a phenomenon in which the electric signal repeats turning on and off due to a mechanical flip-flop of the contacts, immediately after the switch has been pressed.

CHAPTER 2 CIRCUIT DIAGRAM

This chapter describes a circuit diagram and the peripheral hardware to be used in this sample program.

2.1 Circuit Diagram

A circuit diagram is shown below.



Notes 1. Use this in a voltage range of 4.5 V ≤ V_{DD} ≤ 5.5 V.

2. INTP1/P43: 78K0S/KA1+ and 78K0S/KB1+ microcontrollers
INTP1/P32: 78K0S/KY1+ and 78K0S/KU1+ microcontrollers

Cautions 1. Connect the AV_{REF} pin directly to V_{DD} (only for the 78K0S/KA1+ and 78K0S/KB1+ microcontrollers).

2. Connect the AV_{SS} pin directly to GND (only for the 78K0S/KB1+ microcontroller).

3. Leave all unused pins open (unconnected), except for the pins shown in the circuit diagram and the AV_{REF} and AV_{SS} pins.

2.2 Peripheral Hardware

The peripheral hardware to be used is shown below.

(1) Switch (SW)

A switch is used as an input to control the lighting of an LED.

(2) LED

An LED is used as an output corresponding to the interval timer function of 16-bit timer/event counter 00 and switch inputs.

CHAPTER 3 SOFTWARE

This chapter describes the file configuration of the compressed file to be downloaded, internal peripheral functions of the microcontroller to be used, and initial settings and operation overview of the sample program, and shows a flow chart.

3.1 File Configuration

The following table shows the file configuration of the compressed file to be downloaded.

File Name	Description	Compressed (*.zip) File Included		
				
main.asm (Assembly language version) main.c (C language version)	Source file for hardware initialization processing and main processing of microcontroller	●Note 1	●Note 1	
op.asm	Assembler source file for setting the option byte (sets the system clock source)	●	●	
tm00.prw	Work space file for integrated development environment PM+		●	
tm00.prj	Project file for integrated development environment PM+		●	
tm00.pri tm00.prs tm00.prm	Project files for system simulator SM+ for 78K0S/Kx1+		●Note 2	
tm000.pnl	I/O panel file for system simulator SM+ for 78K0S/Kx1+ (used for checking peripheral hardware operations)		●Note 2	●
tm000.wvo	Timing chart file for system simulator SM+ for 78K0S/Kx1+ (used for checking waveforms)			●

Notes 1. “main.asm” is included with the assembly language version, and “main.c” with the C language version.

2. These files are not included among the files for the 78K0S/KU1+ microcontroller.

Remark  : Only the source file is included.

 : The files to be used with integrated development environment PM+ and 78K0S/Kx1+ system simulator SM+ are included.

 : The microcontroller operation simulation file to be used with system simulator SM+ for 78K0S/Kx1+ is included.

3.2 Internal Peripheral Functions to Be Used

The following internal peripheral functions of the microcontroller are used in this sample program.

- Interval timer function: 16-bit timer/event counter 00
- $V_{DD} < V_{LVI}$ detection: Low-voltage detector (LVI)
- Switch input: INTP1[Note] (external interrupt)
- LED output: P20 (output port)

Note INTP1/P43: 78K0S/KA1+ and 78K0S/KB1+ microcontrollers
INTP1/P32: 78K0S/KY1+ and 78K0S/KU1+ microcontrollers

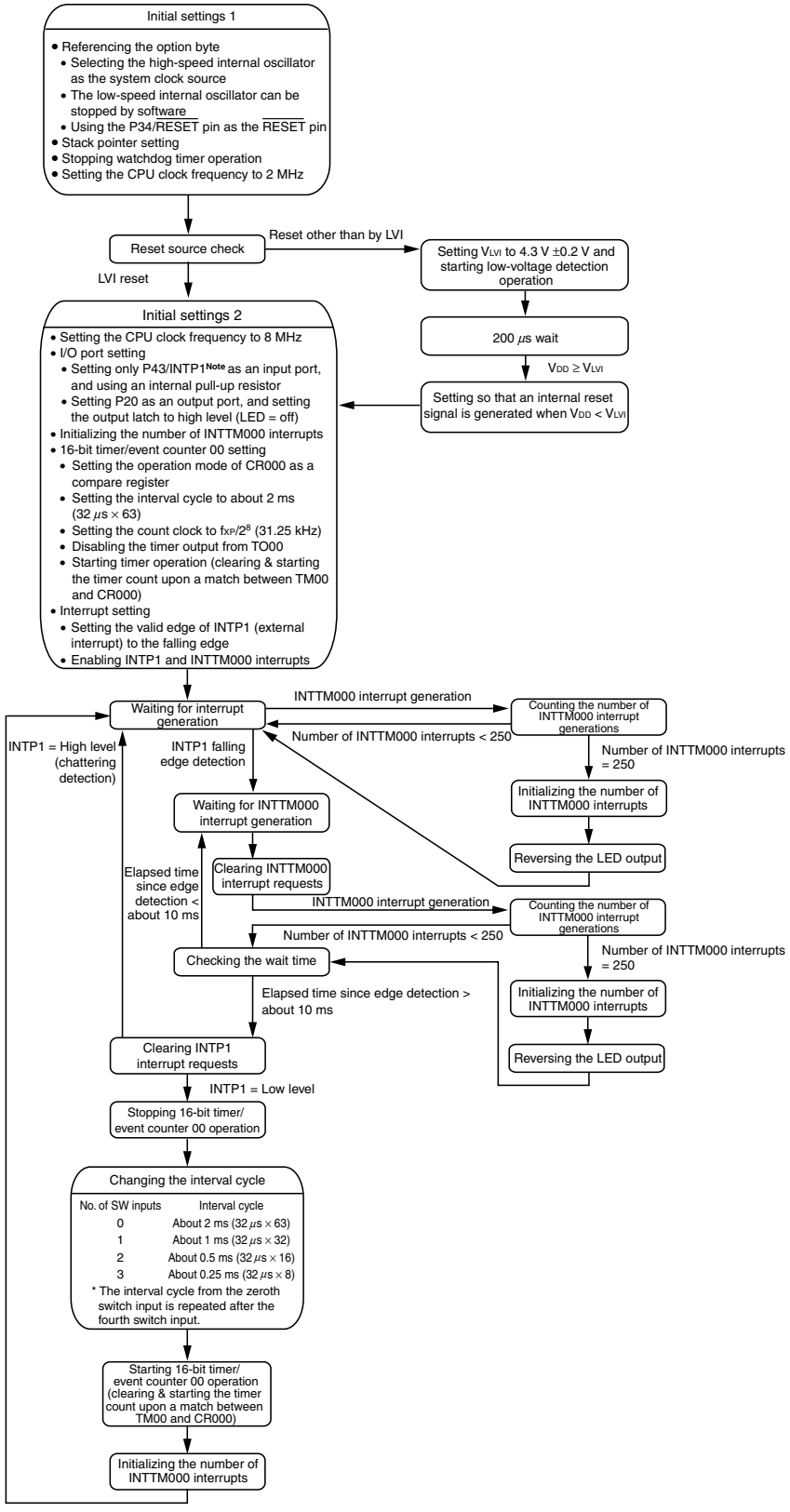
3.3 Initial Settings and Operation Overview

In this sample program, initial settings including the setting of the low-voltage detection function, selection of the clock frequency, setting of the I/O ports, setting of 16-bit timer/event counter 00 (interval timer function), and setting of interrupts are performed.

The LEDs are blinked at fixed cycles by using the generation of a 16-bit timer/event counter 00 interrupt (INTTM000), after completion of the initial settings.

An INTP1 interrupt is serviced when the falling edge of the INTP1 pin, which is generated by switch input, is detected. Chattering is identified when INTP1 is at high level (switch is off), after 10 ms have elapsed since a fall of the INTP1 pin was detected. The blinking cycle of the LEDs is changed in accordance with the number of switch inputs when INTP1 is at low level (switch is on), after 10 ms have elapsed since an edge was detected.

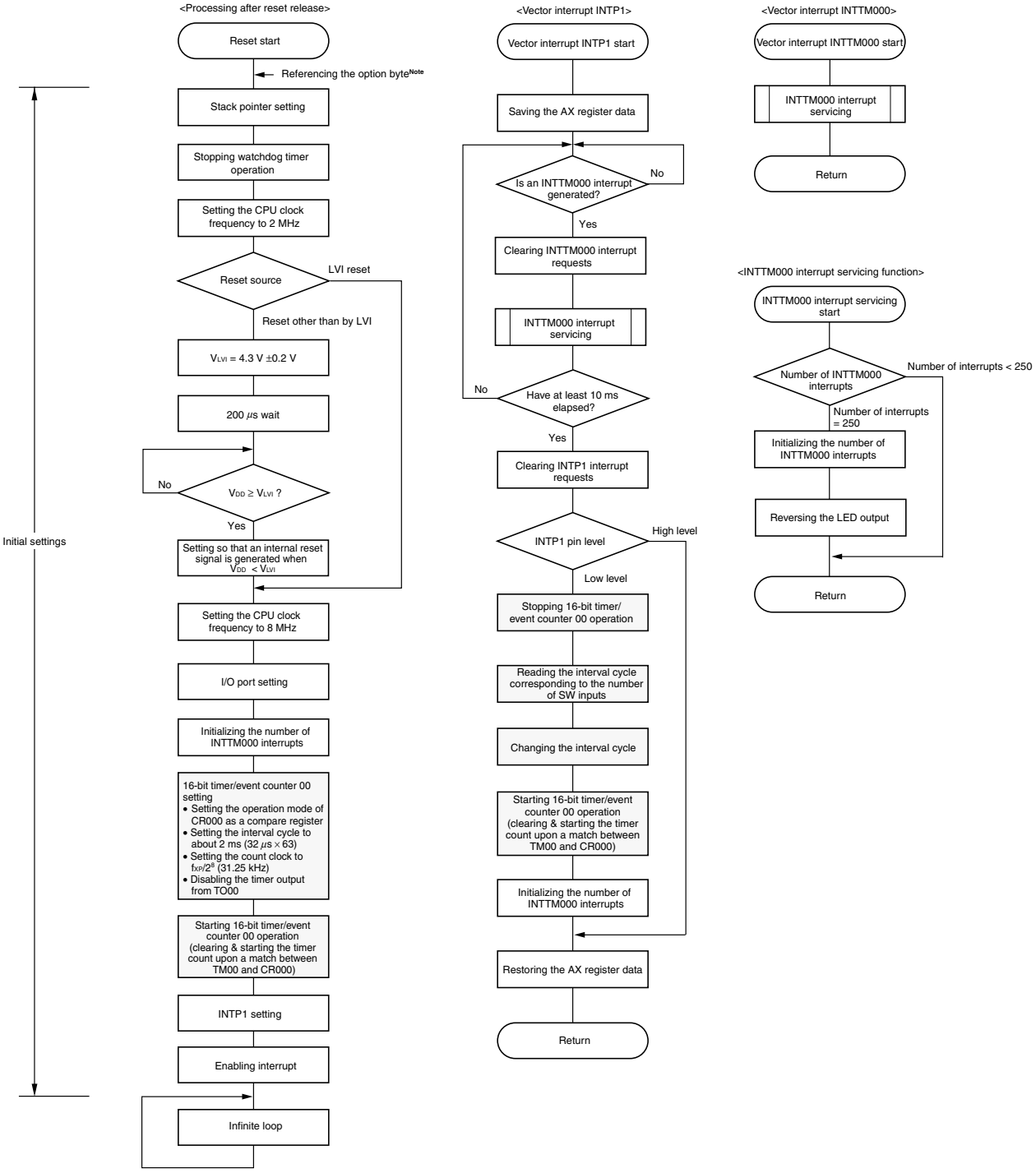
The details are described in the status transition diagram shown below.



Note INTP1/P43: 78K0S/KA1+ and 78K0S/KB1+ microcontrollers
INTP1/P32: 78K0S/KY1+ and 78K0S/KU1+ microcontrollers

3.4 Flow Charts

The flow charts for the sample program are shown below.



Note Referencing the option byte is automatically performed by the microcontroller after reset release. In this sample program, the following contents are set by referencing the option byte.

- Using the high-speed internal oscillation clock (8 MHz (TYP.)) as the system clock source
- The low-speed internal oscillator can be stopped by using software
- Using the P34/$\overline{\text{RESET}}$ pin as the $\overline{\text{RESET}}$ pin

CHAPTER 4 SETTING METHODS

This chapter describes the interval timer function of 16-bit timer/event counter 00.

For other initial settings, refer to the **78K0S/Kx1+ Sample Program (Initial Settings) LED Lighting Switch Control Application Note**. For interrupt, refer to the **78K0S/Kx1+ Sample Program (Interrupt) External Interrupt Generated by Switch Input Application Note**. For low-voltage detection (LVI), refer to the **78K0S/Kx1+ Sample Program (Low-Voltage Detection) Reset Generation During Detection at Less than 2.7 V Application Note**.

For how to set registers, refer to the user's manual of each product (**78K0S/KU1+**, **78K0S/KY1+**, **78K0S/KA1+**, **78K0S/KB1+**).

For assembler instructions, refer to the **78K/0S Series Instructions User's Manual**.

4.1 Setting the Interval Timer Function of 16-bit Timer/Event Counter 00

The following eight types of registers are set when using 16-bit timer/event counter 00 as an interval timer.

A square wave can be output by using the interval timer function when the timer output (TO00 pin output) is enabled by using the TOC00 register.

- Capture/compare control register 00 (CRC00)
- 16-bit timer capture/compare register 000 (CR000)
- Prescaler mode register 00 (PRM00)
- 16-bit timer output control register 00 (TOC00)
- 16-bit timer mode control register 00 (TMC00)
- Port mode register x (PMx)[Note]
- Port register x (Px)[Note]
- Port mode control register x (PMCx)[Note]

Note To use the TO00 pin as the timer output (outputting square wave with the TO00 pin), set it as follows. This setting is not required when not using the TO00 pin as the timer output.

	Px Register	PMx Register	PMCx Register
78K0S/KA1+ and 78K0S/KB1+ microcontrollers	P31 = 0	PM31 = 0	Setting not required
78K0S/KY1+ and 78K0S/KU1+ microcontrollers	P21 = 0	PM21 = 0	PMC21 = 0

<Example of the basic operation setting procedure when using 16-bit timer/event counter 00 as an interval timer>

<1> Setting the CRC00 register

<2> Setting an arbitrary value to the CR000 register

<3> Setting the count clock using the PRM00 register

<4> Setting the TOC00 register

<5> Setting the TMC00 register: starting operation

Caution Steps <1> to <4> may be performed randomly.

(1) Setting the CRC00 register

This register controls the operation of the CR000 and CR010 registers.

Caution CR010 is not used when using 16-bit timer/event counter 00 as an interval timer.

Figure 4-1. Format of Capture/Compare Control Register 00 (CRC00)

CRC00

0	0	0	0	0	CRC002	CRC001	CRC000

CR000 operation mode selection

0	Operates as a compare register.
1	Operates as a capture register.

CR000 capture trigger selection

0	Captures at the valid edge of the TI010 pin.
1	Captures at the reverse phase of the valid edge of the TI000 pin.

CR010 operation mode selection

0	Operates as a compare register.
1	Operates as a capture register.

Cautions 1. The timer operation must be stopped before setting the CRC00 register.

2. Do not specify the CR000 register as a capture register when the clear & start mode has been selected upon a match between TM00 and CR000 by using the TMC00 register.

(2) Setting the CR000 register

This register has the functions of both a capture register and a compare register.

Figure 4-2. Format of 16-bit Timer Capture/Compare Register 000 (CR000)

CR000

When using CR000 as a compare register

The value set to CR000 is constantly compared with the 16-bit timer counter 00 (TM00) count value, and an interrupt request (INTTM000) is generated if they match. It can also be used as the register that holds the interval time when TM00 is set to interval timer operation.

- Interval time = (N + 1)/fsam

Cautions 1. Set a value other than 0000H to the CR000 register in the clear & start mode entered on a match between TM00 and CR000.

2. If the new value of the CR000 register is less than the TM00 counter value, TM00 continues counting, overflows, and then starts counting from 0 again. If the new value of the CR000 register is less than the old value, therefore, the timer must be reset and restarted after the CR000 register value is changed.

3. The value of the CR000 register after the TM00 counter has been stopped is not guaranteed.

4. Capture operation may not be performed for the CR000 register set to the compare mode, even if a capture trigger is input.

5. Changing the CR000 register setting during TM00 counter operation may cause a malfunction.

Remark N: CR000 register setting value (0001H to FFFFH)

fsam: TM00 counter count clock frequency

(3) Setting the PRM00 register

This register is used to set the count clock of the TM00 counter and the valid edges of the TI000 and TI010 pin inputs.

Figure 4-3. Format of Prescaler Mode Register 00 (PRM00)

PRM00

ES110	ES100	ES010	ES000	0	0	PRM001	PRM000

Count clock (fsam) selection

0	0	f_{XP}
0	1	$f_{XP}/2^2$
1	0	$f_{XP}/2^8$
1	1	TI000 pin valid edge[Note]

TI000 pin valid edge selection

0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

TI010 pin valid edge selection

0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

Note The external clock requires a pulse longer than two cycles of the internal clock (f_{XP}).

Remark f_{XP}: Oscillation frequency of the clock supplied to peripheral hardware

Cautions 1. Always set data to the PRM00 register after stopping timer operation.

2. When setting the valid edge of the TI000 pin as the count clock, do not set the clear & start mode with the valid edge of the TI000 pin and the TI000 pin as the capture trigger.

3. In the following cases, note with caution that the valid edge of the TI0n0 pin (n = 0, 1) is detected.

<1> A high level is input to the TI0n0 pin and the TM00 operation is enabled immediately after a system reset.

→ If the rising edge or both the rising and falling edges are specified as the valid edge of the TI0n0 pin, a rising edge is detected immediately after the TM00 operation is enabled.

<2> The TM00 operation is stopped while the TI0n0 pin is at high level and it is then enabled after a low level is input to the TI0n0 pin.

→ If the falling edge or both the rising and falling edges are specified as the valid edge of the TI0n0 pin, a falling edge is detected immediately after the TM00 operation is enabled.

<3> The TM00 operation is stopped while the TI0n0 pin is at low level and it is then enabled after a high level is input to the TI0n0 pin.

→ If the rising edge or both the rising and falling edges are specified as the valid edge of the TI0n0 pin, a rising edge is detected immediately after the TM00 operation is enabled.

Cautions 4. To use the valid edge of TI000 with the count clock, it is sampled with f_{XP} to eliminate noise. The capture operation is not performed until the valid edge is sampled and the valid level is detected twice, thus eliminating noise with a short pulse width.

5. When the TI010/TO00/Pxx pin is used as the input pin (TI010) of the valid edge, it cannot be used as a timer output pin (TO00). When it is used as a timer output pin (TO00), it cannot be used as the input pin (TI010) of the valid edge.

(4) Setting the TOC00 register

This register controls the operation of the 16-bit timer/event counter 00 output controller. It is used to set/reset the timer output F/F, enable or disable output inversion, timer output (TO00 pin output), and one-shot pulse output operation, and set the one-shot pulse output trigger by software.

This setting is not required when not using the TO00 pin as the timer output.

Figure 4-4. Format of 16-bit Timer Output Control Register 00 (TOC00)

TOC00

0	OSPT00	OSPE00	TOC004	LVS00	LVR00	TOC001	TOE00

Timer output control

0	Disables output (fixes output to 0 level).
1	Enables output.

Timer F/F control upon match between CR000 and TM00

0	Disables inversion operation.
1	Enables inversion operation.

Timer output F/F status setting

0	0	Does not change.
0	1	Resets (0) timer output F/F.
1	0	Sets (1) timer output F/F.
1	1	Setting prohibited

Timer F/F control upon match between CR010 and TM00

0	Disables inversion operation.
1	Enables inversion operation.

One-shot pulse output operation control

0	Successive pulse output mode
1	One-shot pulse output mode[Note]

One-shot pulse output trigger control by software

0	Without one-shot pulse output trigger
1	With one-shot pulse output trigger

Note The one-shot pulse output mode operates normally only in the free-running mode and the clear & start mode set with the valid edge of the TI000 pin. In the clear & start mode set upon a match between TM00 and CR000, one-shot pulse output is not possible, because an overflow does not occur.

Cautions 1. The timer operation must be stopped before setting bits other than OSPT00.

2. If LVS00 and LVR00 are read, 0 is read.

3. OSPT00 is automatically cleared after data is set, so 0 is read.

4. Do not set OSPT00 to 1 other than in one-shot pulse output mode.

5. When TOE00 is 0, set TOE00, LVS00, and LVR00 at the same time with the 8-bit memory manipulation instruction. When TOE00 is 1, LVS00 and LVR00 can be set with the 1-bit memory manipulation instruction.

6. When the TI010/TO00/Pxx pin is used as the input pin (TI010) of the valid edge, it cannot be used as a timer output pin (TO00). When it is used as a timer output pin (TO00), it cannot be used as the input pin (TI010) of the valid edge.

(5) Setting the TMC00 register

This register sets the 16-bit timer/event counter 00 operation mode, TM00 counter clear mode, and output timing, and detects overflows.

Figure 4-5. Format of 16-bit Timer Mode Control Register 00 (TMC00)

TMC00

0	0	0	0	TMC003	TMC002	TMC001	OVF00

Overflow detection of 16-bit timer counter 00 (TM00)

0	Overflow not detected.
1	Overflow detected.

			Operation mode and clear mode selection	TO00 inversion timing selection	Interrupt request generation
0	0	0	Operation stop (TM00 cleared to 0)	No change	Not generated
0	0	1			
0	1	0	Free-running mode	Match between TM00 and CR000 or match between TM00 and CR010	<When used as compare register> Generated upon match between TM00 and CR000, or match between TM00 and CR010 <When used as capture register> Generated at valid edge of TI000 pin or TI010 pin
0	1	1		Match between TM00 and CR000, match between TM00 and CR010, or valid edge of TI000 pin	
1	0	0	Clear & start occurs at valid edge of TI000 pin	–	
1	0	1			
1	1	0	Clear & start occurs upon match between TM00 and CR000	Match between TM00 and CR000 or match between TM00 and CR010	
1	1	1		Match between TM00 and CR000, match between TM00 and CR010, or valid edge of TI000 pin	

Cautions 1. The operation of the TM00 counter starts when values other than 0 and 0 (operation stop mode) are set to TMC002 and TMC003, respectively. To stop the operation, set TMC002 and TMC003 to 0 and 0, respectively.

2. Write to the bits other than the OVF00 flag after stopping the timer operation.

3. When the timer is stopped, timer counts and timer interrupts do not occur, even if a signal is input to the TI000/TI010 pin.

4. Except when the valid edge of the TI000 pin is selected as the count clock, stop the timer operation before setting to the STOP mode or system clock stop mode; otherwise the timer may malfunction when the system clock starts.

5. Set the valid edge of the TI000 pin with bits 4 and 5 of the PRM00 register after stopping the timer operation.

6. If the clear & start mode is set upon a match between TM00 and CR000 or at the valid edge of the TI000 pin, or the free-running mode is selected, when the set value of the CR000 register is FFFFH and the TM00 counter value changes from FFFFH to 0000H, the OVF00 flag is set to 1.

7. Even if the OVF00 flag is cleared before the next count clock is counted (before the TM00 counter becomes 0001H) after the TM00 counter overflows, it is re-set and clearing is disabled.

8. Capture operation is performed at the fall of the count clock. An interrupt request (INTTM0n0: n = 0, 1), however, occurs at the rise of the next count clock.

[Example 1] When setting the interval cycle to 2.016 ms and using 16-bit timer/event counter 00 as an interval timer

(Count clock = $f_{XP}/2^8$ (f_{XP} = 8 MHz), no timer output (TO00 pin output))

(Same contents as in this sample program source)

(1) Register settings

<1> CRC00

0	0	0	0	0	x	x	0

CR000 operation mode selection

0	Operates as a compare register.

CR000 capture trigger selection

x	(Invalid setting because CR000 is used as a compare register.)

CR010 operation mode selection

x	(Does not use CR010.)

<2> CR000

Setting value (N): 62

- Count clock fsam = 8 MHz/2^8 = 0.03125 MHz = 31.25 kHz
- Interval cycle 2 ms = (N + 1)/31.25 kHz

→ N = 2 ms × 31.25 kHz − 1 = 61.5 → 62

<3> PRM00

x	x	x	x	0	0	1	0

Count clock (fsam) selection

1	0	$f_{XP}/2^8$

TI000 pin valid edge selection

x	x	(Invalid setting because the TI000 pin is not used. Setting “1, 0”, however, is prohibited.)

TI010 pin valid edge selection

x	x	(Invalid setting because the TI010 pin is not used. Setting “1, 0”, however, is prohibited.)

<4> TOC00

0	0	0	0	0	0	0	0

Timer output control

0	Disables output.

Timer F/F control upon match between CR000 and TM00

0	Disables inversion operation.

Timer output F/F status setting

0	0	Does not change.

Timer F/F control upon match between CR010 and TM00

0	Disables inversion operation.

One-shot pulse output operation control

0	Successive pulse output mode

One-shot pulse output trigger control by software

0	Without one-shot pulse output trigger

<5> TMC00

0	0	0	0	1	1	x	0

Overflow detection of 16-bit timer counter 00 (TM00)

0	Overflow not detected.

			Operation mode and clear mode selection	TO00 inversion timing selection	Interrupt request generation
1	1	0	Clear & start occurs upon match between TM00 and CR000	Match between TM00 and CR000 or match between TM00 and CR010	<When used as compare register> Generated upon match between TM00 and CR000, or match between TM00 and CR010 <When used as capture register> Generated at valid edge of TI000 pin or TI010 pin
1	1	1		Match between TM00 and CR000, match between TM00 and CR010, or valid edge of TI000 pin	

(2) Sample program

In the example below, “x” in **(1) Register settings** is set to “0”.

<1> Assembly language

```
MOV    CRC00, #00000000B
MOVW   CR000, #62
MOV    PRM00, #00000010B
MOV    TOC00, #00000000B
MOV    TMC00, #00001100B
```

<2> C language

```
CRC00 = 0b00000000;
CR000 = 62;
PRM00 = 0b00000010;
TOC00 = 0b00000000;
TMC00 = 0b00001100;
```

[Example 2] When setting the interval cycle to 50 μs and outputting from the TO00 pin a square wave with a cycle of 100 μs (10 kHz)
(Count clock = $f_{XP}/2^2$ (f_{XP} = 8 MHz), initial value of TO00 output is low level)

(1) Register settings

<1> CRC00

0	0	0	0	0	x	x	0

CR000 operation mode selection

0	Operates as a compare register.

CR000 capture trigger selection

x	(Invalid setting because CR000 is used as a compare register.)

CR010 operation mode selection

x	(Does not use CR010.)

<2> CR000

Setting value (N): 99

- Count clock fsam = 2 MHz
- Interval cycle 50 μs = (N + 1)/2 MHz

→ N = 50 μs × 2 MHz − 1 = 99

<3> PRM00

x	x	x	x	0	0	0	1

Count clock (fsam) selection

0	1	$f_{XP}/2^2$

TI000 pin valid edge selection

x	x	(Invalid setting because the TI000 pin is not used. Setting “1, 0”, however, is prohibited.)

TI010 pin valid edge selection

x	x	(Invalid setting because the TI010 pin is not used. Setting “1, 0”, however, is prohibited.)

<4> TOC00

0	0	0	0	0	1	1	1

Timer output control

1	Enables output.

Timer F/F control upon match between CR000 and TM00

1	Enables inversion operation.

Timer output F/F status setting

0	1	Resets (0) timer output F/F.

Timer F/F control upon match between CR010 and TM00

0	Disables inversion operation.

One-shot pulse output operation control

0	Successive pulse output mode

One-shot pulse output trigger control by software

0	Without one-shot pulse output trigger

<5> TMC00

0	0	0	0	1	1	x	0

Overflow detection of 16-bit timer counter 00 (TM00)

0	Overflow not detected.

			Operation mode and clear mode selection	TO00 inversion timing selection	Interrupt request generation
1	1	0	Clear & start occurs upon match between TM00 and CR000	Match between TM00 and CR000 or match between TM00 and CR010	<When used as compare register> Generated upon match between TM00 and CR000, or match between TM00 and CR010 <When used as capture register> Generated at valid edge of TI000 pin or TI010 pin
1	1	1		Match between TM00 and CR000, match between TM00 and CR010, or valid edge of TI000 pin	

<6> Px, PMx, PMCx

	Px Register	PMx Register	PMCx Register
78K0S/KA1+ and 78K0S/KB1+ microcontrollers	P31 = 0	PM31 = 0	Setting not required
78K0S/KY1+ and 78K0S/KU1+ microcontrollers	P21 = 0	PM21 = 0	PMC21 = 0

(2) Sample program

In the example below, “x” in **(1) Register settings** is set to “0”.

<1> Assembly language (when using the 78K0S/KA1+ and 78K0S/KB1+ microcontrollers)

```
CLR1   P3.1
CLR1   PM3.1
MOV    CRC00, #00000000B
MOVW   CR000, #99
MOV    PRM00, #00000001B
MOV    TOC00, #00000111B
MOV    TMC00, #00001100B
```

<2> C language (when using the 78K0S/KA1+ and 78K0S/KB1+ microcontrollers)

```
P3.1 = 0;
PM3.1 = 0;
CRC00 = 0b00000000;
CR000 = 99;
PRM00 = 0b00000001;
TOC00 = 0b00000111;
TMC00 = 0b00001100;
```

[Excerpt from this sample program source]

An excerpt from **APPENDIX A PROGRAM LIST**, which is related to the 16-bit timer/event counter 00 function, is shown below (same contents as in [**Example 1**] mentioned above).

(1) Assembly language

```
XMAIN  CSEG   UNIT
RESET_START:
                    •
                    •
                    •
       MOV    CRC00, #00000000B    ; Use CR000 as a compare register
       MOVW   AX,    #63-1         ; Assign the LED blinking base time initial value
to the AX register
       MOVW   CR000, AX            ; Initialize the LED blinking base time
       MOV    PRM00, #00000010B    ; Count clock = fxp/2^8 = 31.25 kHz
       MOV    TOC00, #00000000B    ; Do not perform timer output
       MOV    TMC00, #00001100B    ; Start the timer operation (clear & start upon a
match between TM00 and CR000)

       MOV    INTM0, #00000000B    ; Set the valid edge of INTP1 to falling edge
       MOV    IF0,   #00H          ; Clear invalid interrupt requests in advance
       CLR1   PMK1                 ; Unmask INTP1 interrupts
       CLR1   TMMK000              ; Unmask INTTM000 interrupts

       EI                          ; Enable vector interrupt

MAIN_LOOP:
       NOP
       BR     $MAIN_LOOP           ; Go to the MAIN_LOOP
                    •
                    •
                    •
       MOV    TMC00, #00000000B    ; Stop the timer operation

       MOV    A,     L             ; Read the lower 8 bits of the table address
       ADD    A,     #2            ; Increment the table address by 2
       AND    A,     #00000111B    ; Mask bits other than bits 0 to 2
       MOV    L,     A             ; Write to the lower 8 bits of the table address
       MOV    A,     [HL]          ; Read the lower 8 bits of the compare value from
the table
       MOV    X,     A
       MOV    A,     [HL+1]        ; Read the higher 8 bits of the compare value from
the table
       MOVW   CR000, AX            ; Change the LED blinking base time

       MOV    TMC00, #00001100B    ; Start the timer operation (clear & start upon a
match between TM00 and CR000)
                    •
                    •
                    •
INTERRUPT_TM000:
       CALL   !SUB_INTERRUPT_TM000; INTTM000 subroutine call
       RETI                        ; Return from interrupt servicing
                    •
                    •
                    •
```

Setting the interval time

Setting the operation mode of CR000 as a compare register

Setting the count clock

Disabling timer output

Starting timer operation

Clearing the INTTM000 interrupt request flag

Enabling INTTM000 interrupt servicing

Setting the CR000 register after stopping timer operation

Starting timer operation

Starting interrupt servicing by INTTM000 interrupt generation

(2) C language

```
void hdwinit(void){
      unsigned char ucCnt200us;  /* 8-bit variable for 200 us wait */
                  •
                  •
                  •
      CRC00 = 0b00000000;        /* Use CR000 as a compare register */
      CR000 = 63-1;              /* Initialize the LED blinking base time */
      PRM00 = 0b00000010;        /* Count clock = fxp/2^8 = 31.25 kHz */
      TOC00 = 0b00000000;        /* Do not perform timer output */
      TMC00 = 0b00001100;        /* Start the timer operation (clear & start upon a
match between TM00 and CR000) */

      INTM0 = 0b00000000;        /* Set the valid edge of INTP1 to falling edge */
      IF0   = 0x00;              /* Clear invalid interrupt requests in advance */
      PMK1  = 0;                 /* Unmask INTP1 interrupts */
      TMMK000 = 0;               /* Unmask INTTM000 interrupts */
      return;
}

void main(void){

      EI();                      /* Enable vector interrupt */

      while (1){
            NOP();
            NOP();
      }
}
                  •
                  •
                  •
      TMC00 = 0b00000000; /* Stop the timer operation */
      CR000 = g_unCR000data[g_ucSWcnt];
                  /* Change the LED blinking base time in accordance
with the number of switch inputs */
      TMC00 = 0b00001100; /* Start the timer operation (clear & start upon a
match between TM00 and CR000) */
                  •
                  •
                  •
interrupt void fn_inttm000(){

      fn_subinttm000();          /* Service the INTTM000 interrupt */

      return;
                  •
                  •
                  •
```

Setting the interval time

Setting the operation mode of CR000 as a compare register

Setting the count clock

Disabling timer output

Starting timer operation

Enabling INTTM000 interrupt servicing

Clearing the INTTM000 interrupt request flag

Setting the CR000 register after stopping timer operation

Starting timer operation

Starting interrupt servicing by INTTM000 interrupt generation

4.2 Setting the LED Blinking Cycle and Chattering Detection Time

The LED blinking cycle and chattering detection time are set as follows in this sample program.

(1) Setting the LED blinking cycle

The LED output is reversed every 250 generations of 16-bit timer/event counter 00 interrupts (INTTM000) in this sample program.

- Interrupt cycle (interval time) = (N + 1)/fsam
- LED output reversal cycle = Interrupt cycle × Number of interrupts
- LED blinking cycle = LED output reversal cycle × 2

Remark N: CR000 register setting value
fsam: Count clock frequency of 16-bit timer/event counter 00

Calculation example: The following values result when the CR000 register setting value is 62 (during operation at fsam = 31.25 kHz).

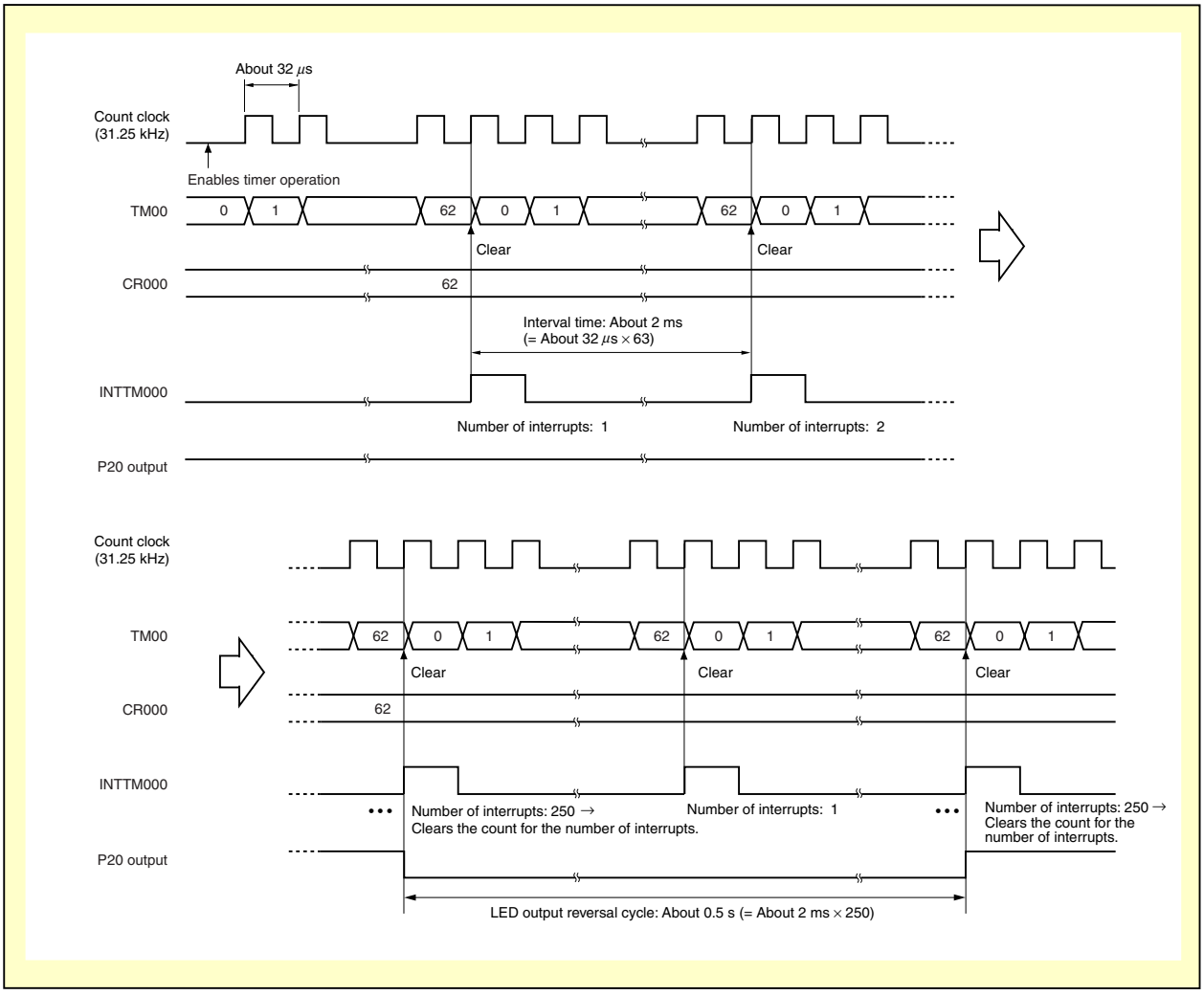
- Interrupt cycle (interval time) = (N + 1)/fsam = (62 + 1)/31.25 kHz = 2 ms
- LED output reversal cycle = Interrupt cycle × Number of interrupts = 2 ms × 250 = 500 ms
- LED blinking cycle = LED output reversal cycle × 2 = 500 ms × 2 = 1 s

Furthermore, the CR000 register setting value is changed in accordance with the number of switch inputs, and the LED blinking cycle is changed.

Number of Switch Inputs[Note]	CR000 Register Setting Value	Interrupt Cycle	LED Blinking Cycle
0	62	2.016 ms ((62 + 1)/31.25 kHz)	1.008 s (2.016 ms × 250 × 2)
1	31	1.024 ms ((31 + 1)/31.25 kHz)	0.512 s (1.024 ms × 250 × 2)
2	15	0.512 ms ((15 + 1)/31.25 kHz)	0.256 s (0.512 ms × 250 × 2)
3	7	0.256 ms ((7 + 1)/31.25 kHz)	0.128 s (0.256 ms × 250 × 2)

Note The blinking cycle from the zeroth switch input is repeated after the fourth switch input.

Figure 4-6. Timing Chart Example of the LED Blinking Cycle (When the LEDs Blink at a Cycle of About 1 s)



Remark The CR000 register setting value is 31, 15, and 7 when the LEDs blink at respective cycles of about 1/2 s, 1/4 s, and 1/8 s.

(2) Setting the chattering detection time

The generation of 16-bit timer/event counter 00 interrupts (INTTM000) is counted to remove chattering of 10 ms or less, in order to handle chattering during switch input (INTP1 interrupt generation) in this sample program.

INTTM000 interrupts can be continuously counted even during chattering detection by using INTTM000 interrupts for chattering detection. Consequently, offsets of the LED blinking cycle, which are caused by switch input, can be suppressed.

- Chattering detection time (T_C) = $T' + T \times (M - 1)$

Remark T: INTTM000 interrupt cycle

T': Time from the start of INTP1 edge detection until the first INTTM000 is generated after INTP1 edge detection ($0 < T' \leq T$)

M: Number of INTTM000 interrupts after INTP1 edge detection

When set such that $T \times (M - 1) = 10$ ms,

$T_C = T' + 10$ ms

$0 < T' \leq T$, therefore,

$10 \text{ ms} < T_C \leq T + 10 \text{ ms}$

↓

Chattering detection time (T_C) > 10 ms

Calculation example: When the interrupt cycle (T) is 2 ms (refer to the calculation example in **(1) Setting the LED blinking cycle**), and the number of INTTM000 interrupts after INTP1 edge detection (M) is 6

$T_C = T' + T \times (M - 1)$

$= T' + 2 \text{ ms} \times (6 - 1)$

$= T' + 10 \text{ ms}$

$0 < T' \leq 2$ ms, therefore,

$10 \text{ ms} < T_C \leq 12 \text{ ms}$

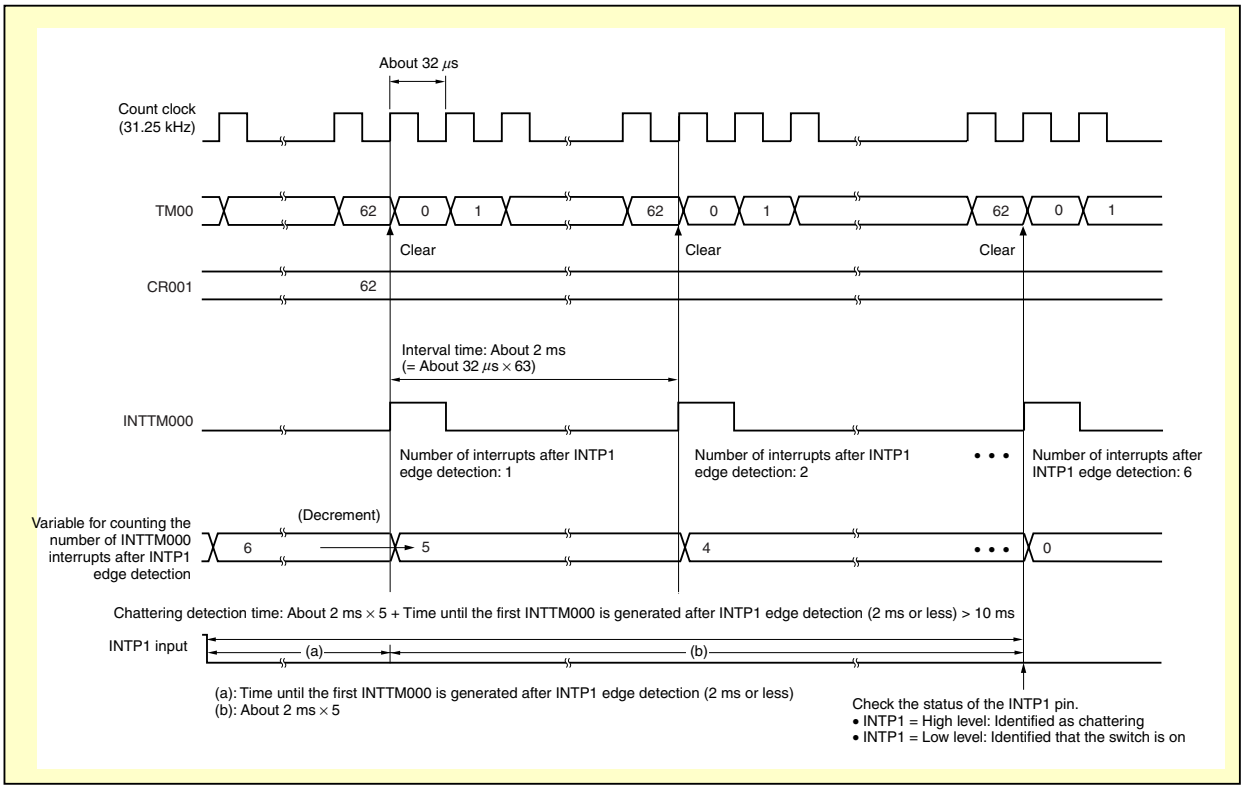
↓

Chattering detection time (T_C) > 10 ms

The following table shows the correspondence between the interrupt cycles during switch input and the number of INTTM000 interrupts after INTP1 edge detection in this sample program.

LED Blinking Cycle	Interrupt Cycle	Number of INTTM000 Interrupts After INTP1 Edge Detection	Chattering Detection Time
1.008 s	2.016 ms	6	$10.08 \text{ ms} < T_C \leq 12.096 \text{ ms}$
0.512 s	1.024 ms	11	$10.24 \text{ ms} < T_C \leq 11.264 \text{ ms}$
0.256 s	0.512 ms	21	$10.24 \text{ ms} < T_C \leq 10.752 \text{ ms}$
0.128 s	0.256 ms	41	$10.24 \text{ ms} < T_C \leq 10.496 \text{ ms}$

Figure 4-7. Timing Chart Example of Chattering Detection (When the LEDs Blink at Cycles of About 1 s During Switch Input)



Remark The variable for counting the number of INTTM000 interrupts after INTP1 edge detection depends on the LED blinking cycle during switch input. The variable is 11, 21, and 41, when the LEDs blink at respective cycles of about 1/2 s, 1/4 s, and 1/8 s.

CHAPTER 5 OPERATION CHECK USING SYSTEM SIMULATOR SM+

This chapter describes how the sample program operates with system simulator SM+ for 78K0S/Kx1+, by using the assembly language file (source files + project file) that has been downloaded by selecting the  icon.

<R> **Caution System simulator SM+ for 78K0S/Kx1+ is not supported with the 78K0S/KU1+ microcontroller (as of July 2008). The operation of the 78K0S/KU1+ microcontroller, therefore, cannot be checked by using system simulator SM+ for 78K0S/Kx1+.**

<R> 5.1 Building the Sample Program

To check the operation of the sample program by using system simulator SM+ for 78K0S/Kx1+ (hereinafter referred to as “SM+”), SM+ must be started after building the sample program. This section describes how to build a sample program by using the assembly language sample program (source program + project file) downloaded by clicking the  icon. See the **78K0S/Kx1+ Sample Program Startup Guide Application Note** for how to build other downloaded programs.

For the details of how to operate PM+, refer to the **PM+ Project Manager User’s Manual**.

[Column] Build errors

Change the compiler option setting according to the following procedure when the error message “A006 File not found ‘C:\NECTOOLS32\LIB78K0S\s0sl.rel’” or “*** ERROR F206 Segment ‘@@DATA’ can’t allocate to memory - ignored.” is displayed, when building with PM+.

<1> Select [Compiler Options] from the [Tool] menu.
<2> The [Compiler Options] dialog box will be displayed. Select the [Startup Routine] tab.
<3> Uncheck the [Using Fixed Area of Standard Library] check box. (Leave the other check boxes as they are.)

A RAM area of 118 bytes that has been secured as a fixed standard library area will be enabled for use when the [Using Fixed Area of Standard Library] check box is unchecked; however, the standard libraries (such as the getchar function and malloc function) will be disabled for use.

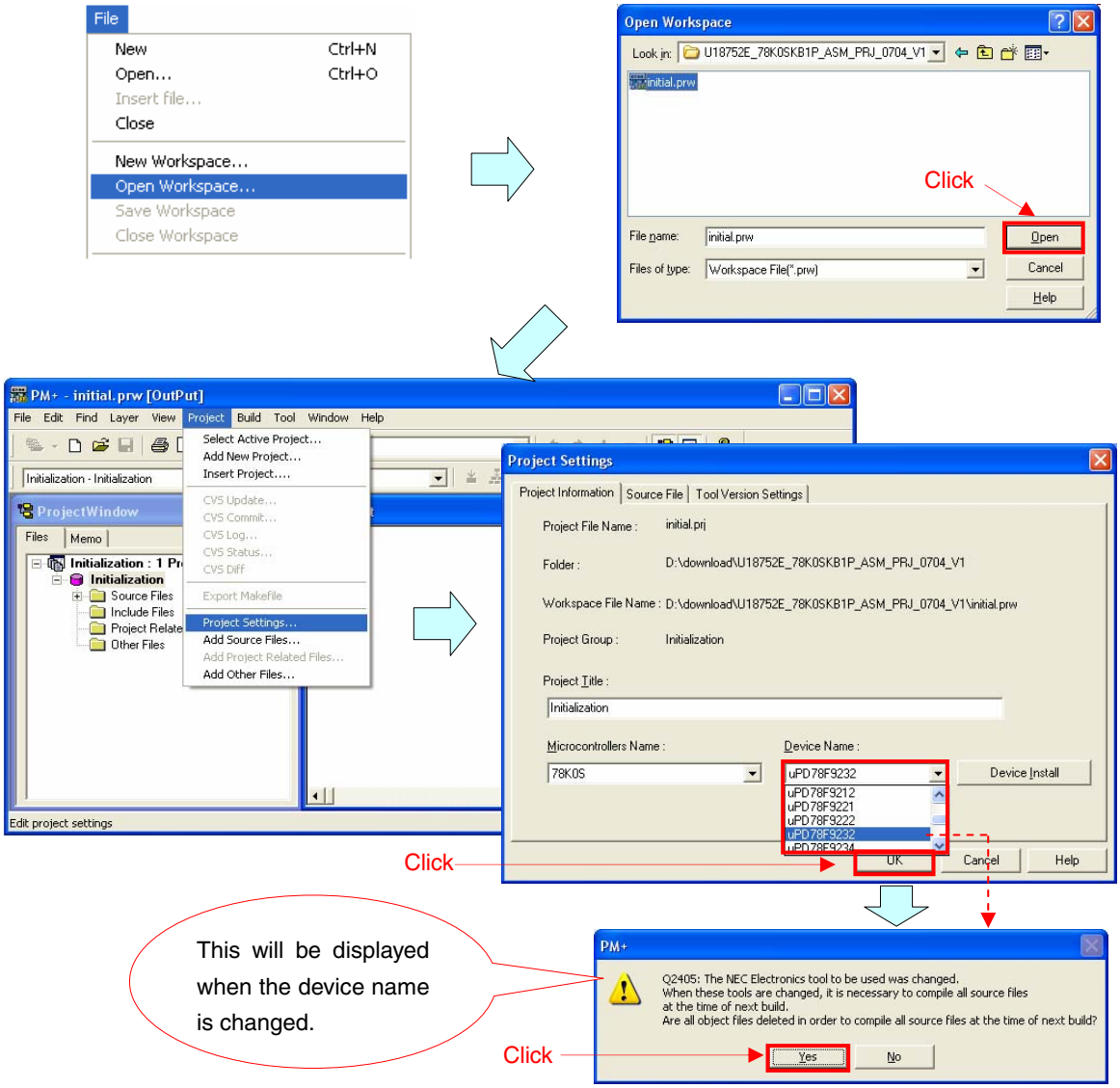
The [Using Fixed Area of Standard Library] check box is unchecked by default when the file that has been downloaded by clicking the  icon is used in this sample program.

(1) Start PM+.

(2) Select “tm00.prw” by clicking [Open Workspace] from the [File] menu and click [Open]. A workspace into which the source file will be automatically read will be created.

(3) Select [Project Settings] from the [Project] menu. When the [Project Settings] window opens, select the name of the device to be used (the device with the largest ROM or RAM size will be selected by default), and click [OK].

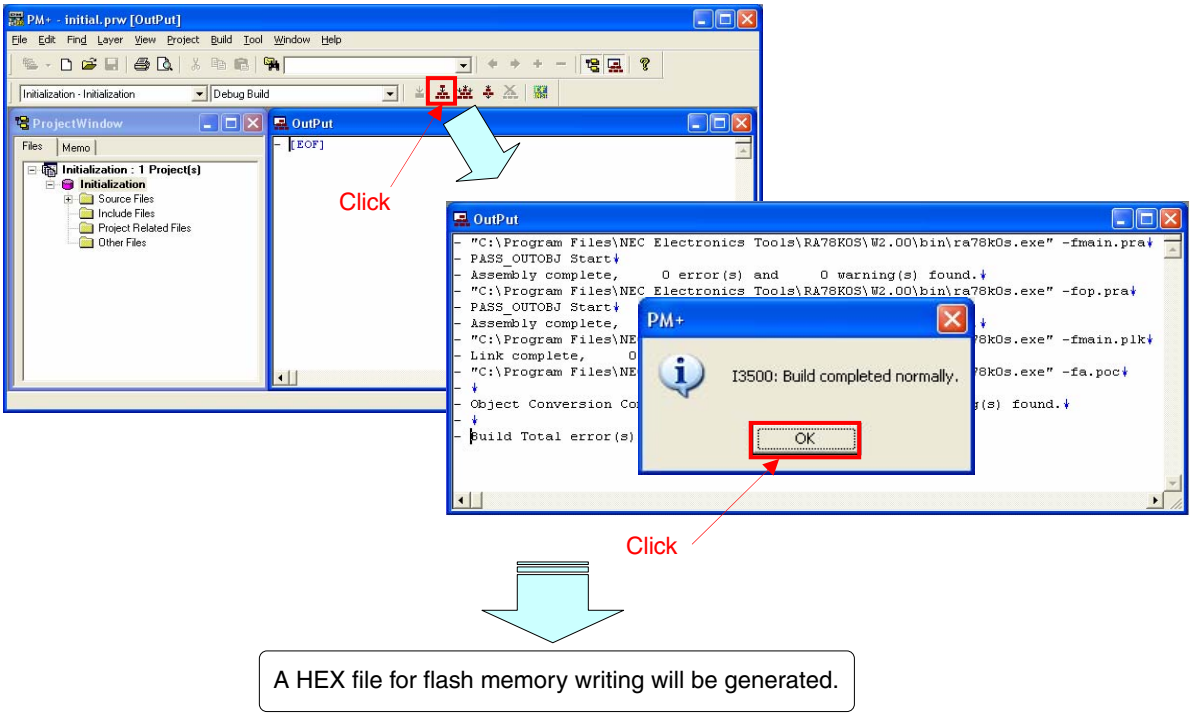
Remark Screenshots of the Sample Program (Initial Settings) LED Lighting Switch Control are shown below.



(4) Click  ([Build] button). When the source files are built normally, the message “I3500: Build completed normally.” will be displayed.

(5) Click the [OK] button in the message dialog box. A HEX file for flash memory writing will be created.

Remark Screenshots of the Sample Program (Initial Settings) LED Lighting Switch Control are shown below.



5.2 Operation with SM+

This section describes examples of checking the operation on the I/O panel window or timing chart window of SM+. For the details of how to operate SM+, refer to the **SM+ System Simulator Operation User’s Manual**.

<R> (1) When SM+ for 78K0S/Kx1+ W1.02 (“SM+” hereafter) is used in the environment of PM+ Ver. 6.30, SM+ cannot be selected as the debugger. In this case, start SM+ via method (a) or (b) described below, while keeping PM+ running after completing building a project.

(a) When starting SM+ in PM+

<1> Select [Register Ex-tool] from the [Tool] menu and register “SM+ for 78K0S/Kx1+”.

<2> Select [Ex-tool Bar] from the [View] menu and add the SM+ icon to the PM+ toolbar.

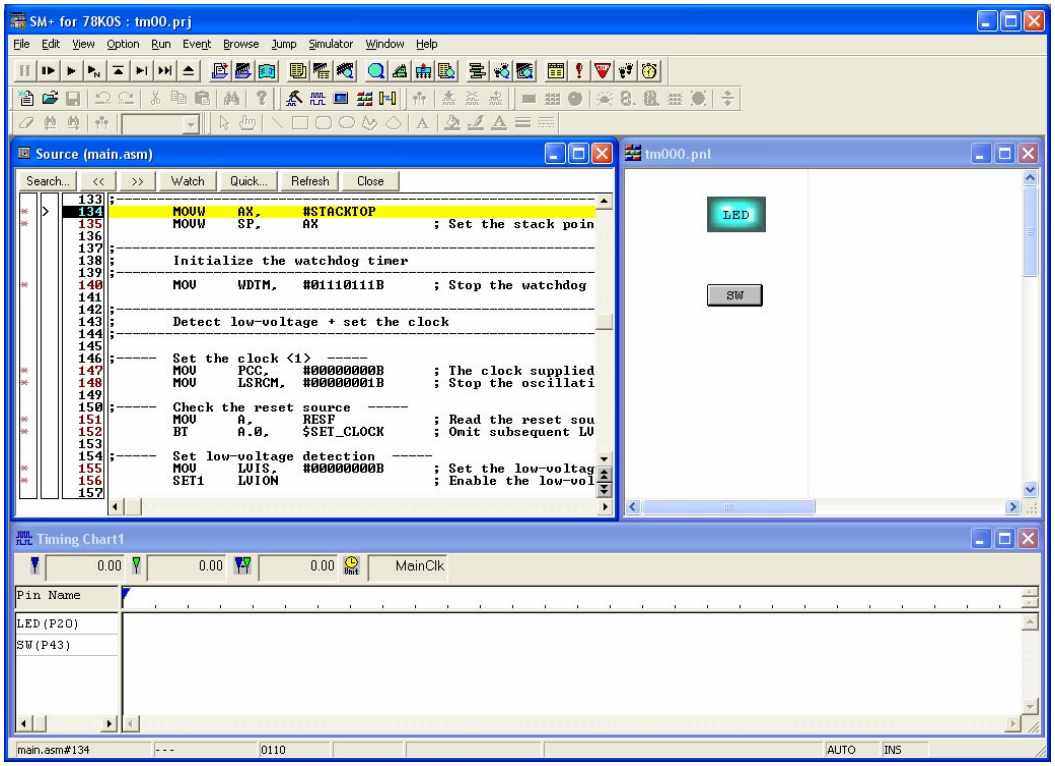
<3> Click the SM+ icon and start SM+.

(See the PM+ help for details on how to register external tools.)

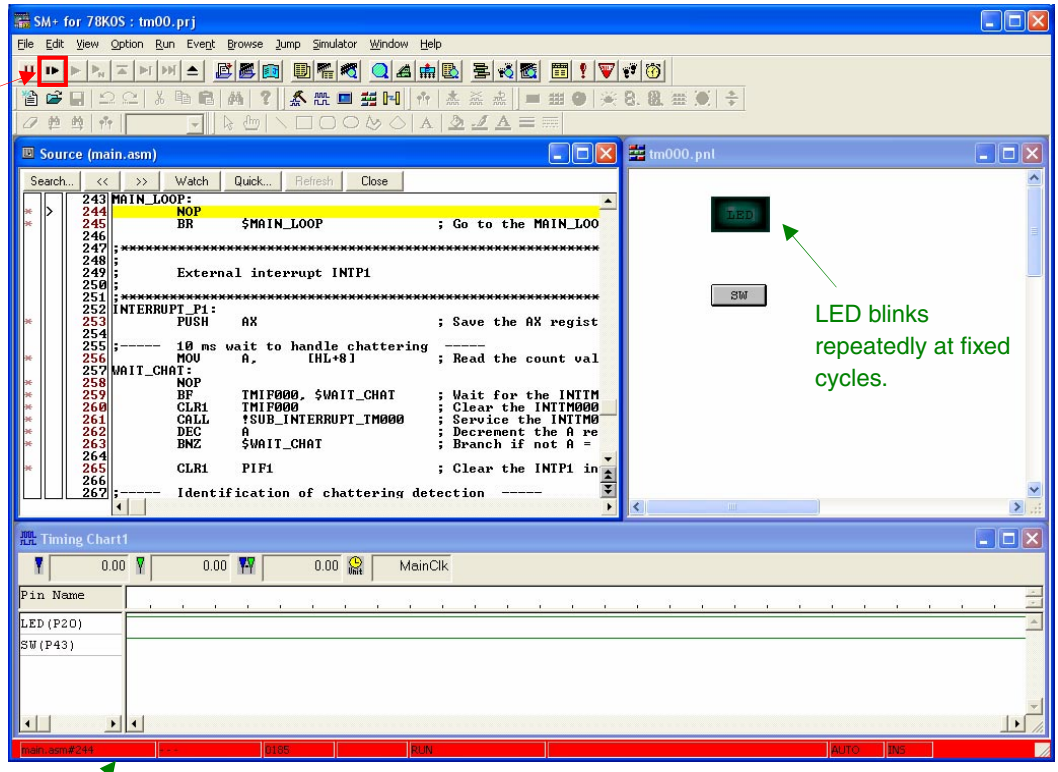
(b) When not starting SM+ in PM+

•Start SM+ from the Windows start menu.

(2) The following screen will be displayed when SM+ is started. (This is a sample screenshot of when an assembly language source file downloaded by clicking the  icon was used.)

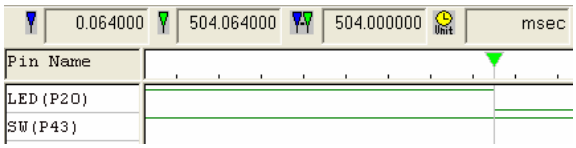
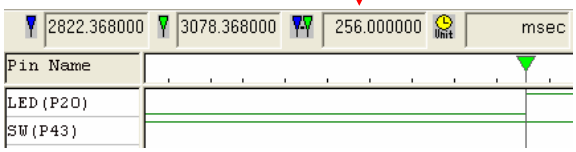
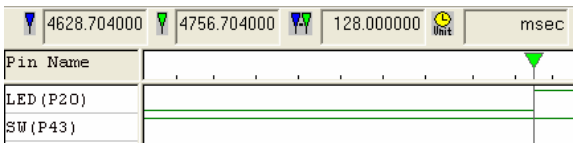
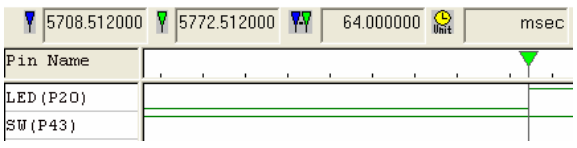


(3) Click  ([Restart] button). The program will be executed after the CPU is reset and the following screen will be displayed.



(4) Click the [SW] button in the I/O panel window, during program execution.
Check that the blinking cycle of [LED] in the I/O panel window and the waveforms in the timing chart window change, depending on the number of [SW] button inputs.

Note 1

I/O panel window	Timing chart window
Blinks at cycles of about 1 s[Note 2]. LED Do not click. SW	The reversal cycle of the LED (P20) is 504 ms. 
Blinks at cycles of about 1/2 s[Note 2]. LED Click once. → SW	The reversal cycle of the LED (P20) is 256 ms. 
Blinks at cycles of about 1/4 s[Note 2]. LED Click twice. → SW	The reversal cycle of the LED (P20) is 128 ms. 
Blinks at cycles of about 1/8 s[Note 2]. LED Click three times. → SW	The reversal cycle of the LED (P20) is 64 ms. 

Notes 1. The blinking cycle from the zeroth [SW] button input is repeated after the fourth [SW] button input.

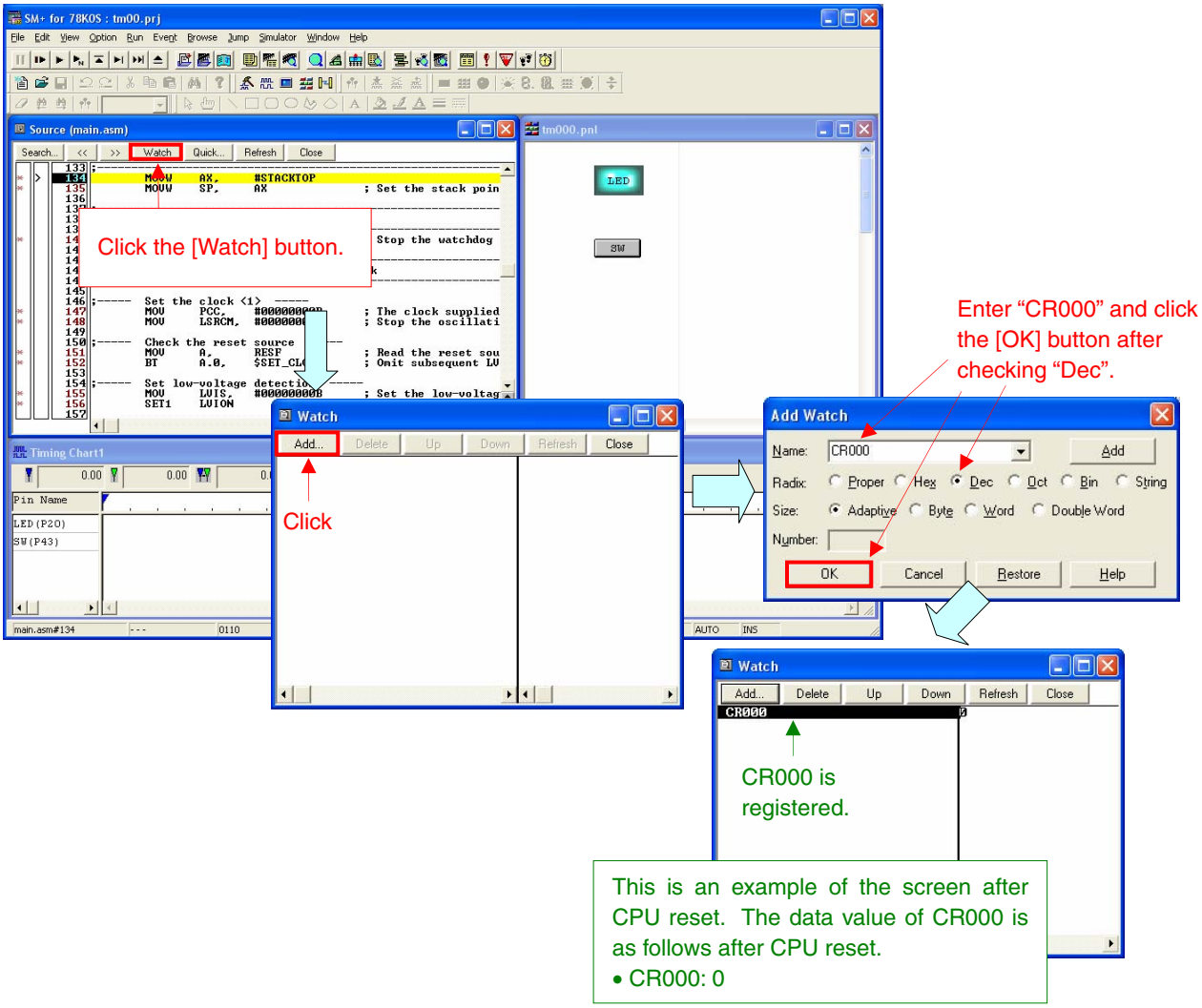
2. This may differ from the actual blinking cycle, depending on the operation environment of the PC used.

[Supplement 1] The changes in the data value of the CR000 register can be checked by using the SM+ watch function.

<1> Click the [Watch] button in the source window to open the [Watch] window.

<2> Click [Add] to open the [Add Watch] window. (At this time, the [Watch] window is kept opened.)

<3> Enter “CR000” in the [Name] field and click the [OK] button after checking “Dec” under Radix. “CR000” will be registered in the [Watch] window and the [Add Watch] window will be closed.



<4> Execute the program and click the [SW] button in the I/O panel window. Check that the data value of CR000 in the [Watch] window changes, depending on the number of [SW] button inputs.

Number of [SW] Button Inputs[Note]	Data Value in [Watch] Window
0	CR000: 62
1	CR000: 31
2	CR000: 15
3	CR000: 7

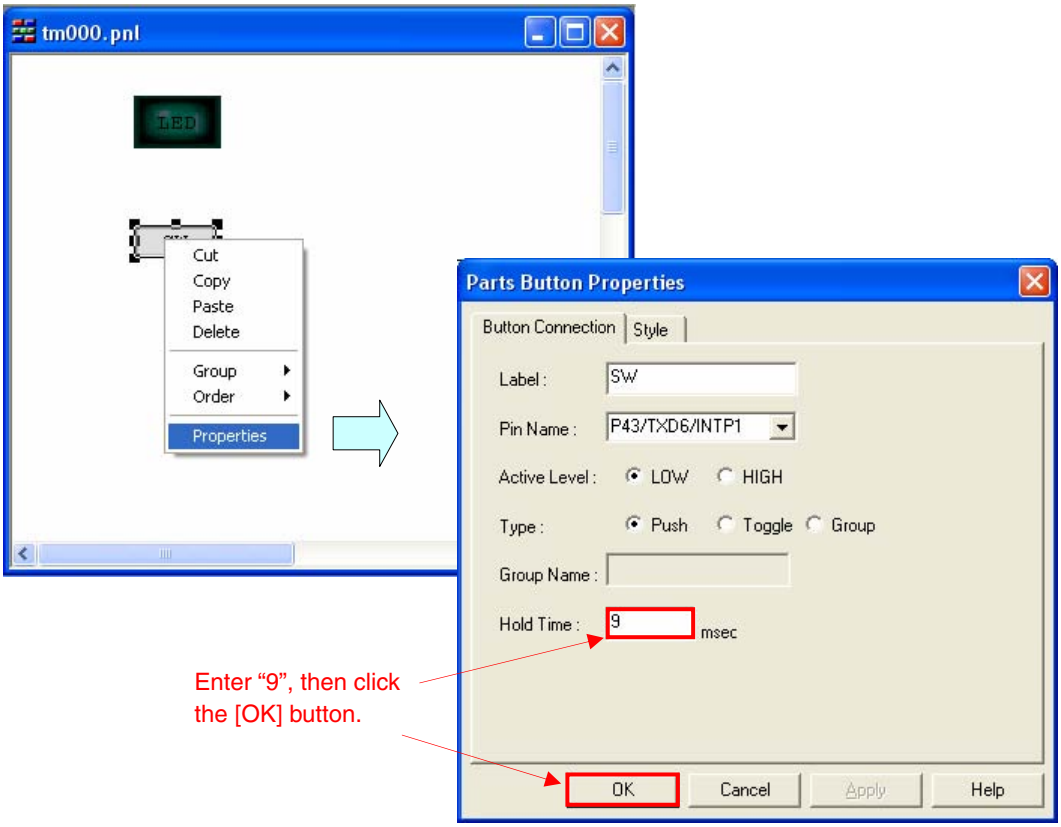
Note The lighting patterns from the zeroth switch input are repeated after the fourth switch input.

[Supplement 2] The [SW] button hold time can be set to less than 10 ms to check whether chattering is being detected.

<1> Select  on the toolbar.

<2> Right-click the [SW] button in the I/O panel window and select [Properties].

<3> Enter “9” for the Hold Time and click the [OK] button.



<4> Select  on the toolbar.

<5> Execute the program and click the [SW] button. Even if the [SW] button is clicked, chattering will be identified and the LED blinking cycle will not change, because the button hold time is 9 ms.

CHAPTER 6 RELATED DOCUMENTS

Document Name			Japanese/English
78K0S/KU1+ User's Manual			PDF
78K0S/KY1+ User's Manual			PDF
78K0S/KA1+ User's Manual			PDF
78K0S/KB1+ User's Manual			PDF
78K/0S Series Instructions User's Manual			PDF
RA78K0S Assembler Package User's Manual		Language	PDF
		Operation	PDF
CC78K0S C Compiler User's Manual		Language	PDF
		Operation	PDF
PM+ Project Manager User's Manual			PDF
SM+ System Simulator Operation User's Manual			PDF
<R> Flash Programming Manual (Basic) MINICUBE2 version		78K0S/KU1+	PDF
		78K0S/KY1+	PDF
		78K0S/KA1+	PDF
		78K0S/KB1+	PDF
78K0S/Kx1+ Application Note	Sample Program Startup Guide		PDF
	Sample Program (Initial Settings) LED Lighting Switch Control		PDF
	Sample Program (Interrupt) External Interrupt Generated by Switch Input		PDF
	Sample Program (Low-Voltage Detection) Reset Generation During Detection at Less than 2.7 V		PDF
	Sample Program (16-bit Timer/Event Counter 00) External Event Counter		PDF
	Sample Program (16-bit Timer/Event Counter 00) Pulse Width Measurement		PDF
	Sample Program (16-bit Timer/Event Counter 00) PPG Output		PDF
	Sample Program (16-bit Timer/Event Counter 00) One-Shot Pulse Output		PDF

APPENDIX A PROGRAM LIST

As a program list example, the 78K0S/KB1+ microcontroller source program is shown below.

● main.asm (Assembly language version)

```
;*******************************************************************************
;
;     NEC Electronics     78K0S/KB1+
;
;*******************************************************************************
;     78K0S/KB1+  Sample program
;*******************************************************************************
;     16-bit timer 00 (interval timer)
;*******************************************************************************
;<<History>>
;     2007.7.--   Release
;*******************************************************************************
;
;<<Overview>>
;
;This sample program presents an example of using the interval timer function
;of 16-bit timer 00.  The LEDs are blinked by reversing the P20 pin output
;through the use of 16-bit timer 00 interrupts.  The LED blinking cycle is
;changed by rewriting the compare register of the timer when a switch input
;interrupt is generated.
;
;
;  <Principal setting contents>
;
;  - Stop the watchdog timer operation
;  - Set the low-voltage detection voltage (VLVI) to 4.3 V +-0.2 V
;  - Generate an internal reset signal (low-voltage detector) when VDD < VLVI
after VDD >= VLVI
;  - Set the CPU clock to 8 MHz
;  - Set the clock supplied to the peripheral hardware to 8 MHz
;  - Set the valid edge of external interrupt INTP1 to falling edge
;  - Set the chattering detection time during switch input to 10 ms
;  - Use the HL register for interrupt servicing (similarly as a global
variable)
;
;
;  <16-bit timer 00 settings>
;  - Operation mode: Clear & start the timer count upon a match between TM00
and CR000
;  - Not performing timer output
;  - Count clock = fxp/2^8 (31.25 kHz)
;  - Initial value of timer cycle = About 2 ms (32[us/clk] x 63[count] =
2.016[ms])
;
;
;  <Number of switch inputs and LED blinking cycles>
;
;    +--------------------------+
;    |  SW Inputs | LED Blinking|
;    |   (P43)    | Cycle (P20) |
;    |------------|-------------|
```

```
;    |   0 times  |    1 second |
;    |   1 time   |  1/2 second |
;    |   2 times  |  1/4 second |
;    |   3 times  |  1/8 second |
;    +------------------------+
;    # The blinking cycle from the zeroth switch input is repeated after the
fourth switch input.
;
;
;<<I/O port settings>>
;
;  Input: P43
;  Output: P00-P03, P20-P23, P30-P33, P40-P42, P44-P47, P120-P123, P130
;  # All unused ports are set as the output mode.
;
;************************************************************************


;========================================================================
;
;     Vector table
;
;========================================================================
XVCT  CSEG  AT    0000H
      DW    RESET_START       ;(00) RESET
      DW    RESET_START       ;(02) --
      DW    RESET_START       ;(04) --
      DW    RESET_START       ;(06) INTLVI
      DW    RESET_START       ;(08) INTP0
      DW    INTERRUPT_P1      ;(0A) INTP1
      DW    RESET_START       ;(0C) INTTMH1
      DW    INTERRUPT_TM000   ;(0E) INTTM000
      DW    RESET_START       ;(10) INTTM010
      DW    RESET_START       ;(12) INTAD
      DW    RESET_START       ;(14) --
      DW    RESET_START       ;(16) INTP2
      DW    RESET_START       ;(18) INTP3
      DW    RESET_START       ;(1A) INTTM80
      DW    RESET_START       ;(1C) INTSRE6
      DW    RESET_START       ;(1E) INTSR6
      DW    RESET_START       ;(20) INTST6

;========================================================================
;
;     Define the ROM data table
;
;========================================================================
XROM  CSEG  AT    0100H
;-----  For setting the timer 00 cycle  -----
      DW    63-1              ; 2 ms interval compare value
      DW    32-1              ; 1 ms interval compare value
      DW    16-1              ; 0.5 ms interval compare value
      DW    8-1               ; 0.25 ms interval compare value
;-----  For handling chattering  -----
      DW    5+1               ; Count value for handling chattering (for 2 ms
interval)
      DW    10+1              ; Count value for handling chattering (for 1 ms
interval)
```

```
      DW    20+1              ; Count value for handling chattering (for 0.5
ms interval)
      DW    40+1              ; Count value for handling chattering (for 0.25
ms interval)

;=============================================================================
;
;     Define the RAM
;
;=============================================================================
XRAM  DSEG  SADDR
CNT_TM000:  DS    1           ; For counting INTTM000 interrupt

;=============================================================================
;
;     Define the memory stack area
;
;=============================================================================
XSTK  DSEG  AT    0FEE0H
STACKEND:
      DS    20H               ; Memory stack area = 32 bytes
STACKTOP:                     ; Start address of the memory stack area = FF00H

;*****************************************************************************
;
;     Initialization after RESET
;
;*****************************************************************************
XMAIN CSEG  UNIT
RESET_START:
;-----------------------------------------------------------------------------
;     Initialize the stack pointer
;-----------------------------------------------------------------------------
      MOVW  AX,   #STACKTOP
      MOVW  SP,   AX          ; Set the stack pointer

;-----------------------------------------------------------------------------
;     Initialize the watchdog timer
;-----------------------------------------------------------------------------
      MOV   WDTM, #01110111B  ; Stop the watchdog timer operation

;-----------------------------------------------------------------------------
;     Detect low-voltage + set the clock
;-----------------------------------------------------------------------------

;-----  Set the clock <1>  -----
      MOV   PCC,  #00000000B  ; The clock supplied to the CPU (fcpu) = fxp (=
fx/4 = 2 MHz)
      MOV   LSRCM,      #00000001B  ; Stop the oscillation of the low-speed
internal oscillator

;-----  Check the reset source  -----
      MOV   A,    RESF        ; Read the reset source
      BT    A.0,  $SET_CLOCK  ; Omit subsequent LVI-related processing and go
to SET_CLOCK during LVI reset

;-----  Set low-voltage detection  -----
      MOV   LVIS, #00000000B  ; Set the low-voltage detection level (VLVI) to
4.3 V +-0.2 V
```

```
      SET1  LVION             ; Enable the low-voltage detector operation

      MOV   A,    #40         ; Assign the 200 us wait count value
;-----  200 us wait  -----
WAIT_200US:
      DEC   A
      BNZ   $WAIT_200US       ; 0.5[us/clk] x 10[clk] x 40[count] = 200[us]

;-----  VDD >= VLVI wait processing  -----
WAIT_LVI:
      NOP
      BT    LVIF, $WAIT_LVI   ; Branch if VDD < VLVI

      SET1  LVIMD             ; Set so that an internal reset signal is
generated when VDD < VLVI

;-----  Set the clock <2>  -----
SET_CLOCK:
      MOV   PPCC, #00000000B  ; The clock supplied to the peripheral hardware
(fxp) = fx (= 8 MHz)
                              ;  -> The clock supplied to the CPU (fcpu) = fxp
= 8 MHz

;---------------------------------------------------------------------------
;     Initialize the port 0
;---------------------------------------------------------------------------
      MOV   P0,   #00000000B  ; Set output latches of P00-P03 as low
      MOV   PM0,  #11110000B  ; Set P00-P03 as output mode

;---------------------------------------------------------------------------
;     Initialize the port 2
;---------------------------------------------------------------------------
      MOV   P2,   #00000001B  ; Set output latches of P21-P23 as low, P20 as
high (turn off LED)
      MOV   PM2,  #11110000B  ; Set P20-P23 as output mode

;---------------------------------------------------------------------------
;     Initialize the port 3
;---------------------------------------------------------------------------
      MOV   P3,   #00000000B  ; Set output latches of P30-P33 as low
      MOV   PM3,  #11110000B  ; Set P30-P33 as output mode

;---------------------------------------------------------------------------
;     Initialize the port 4
;---------------------------------------------------------------------------
      MOV   P4,   #00000000B  ; Set output latches of P40-P47 as low
      MOV   PU4,  #00001000B  ; Connect on-chip pull-up resistor to P43
      MOV   PM4,  #00001000B  ; Set P40-P42 and P44-P47 as output mode, P43 as
input mode

;---------------------------------------------------------------------------
;     Initialize the port 12
;---------------------------------------------------------------------------
      MOV   P12,  #00000000B  ; Set output latches of P120-P123 as low
      MOV   PM12, #11110000B  ; Set P120-P123 as output mode

;---------------------------------------------------------------------------
;     Initialize the port 13
;---------------------------------------------------------------------------
```

```
      MOV   P13,  #00000001B  ; Set output latch of P130 as high

;-------------------------------------------------------------------------
;     Initialize the general-purpose register and RAM
;-------------------------------------------------------------------------
      MOV   CNT_TM000, #250         ; Initialize the number of INTTM000
interrupts
      MOVW  HL,   #0100H            ; Specify the table address to HL (used
for INTP1 interrupt)

;-------------------------------------------------------------------------
;     Set 16-bit timer 00
;-------------------------------------------------------------------------
      MOV   CRC00,      #00000000B  ; Use CR000 as a compare register
      MOVW  AX,   #63-1             ; Assign the LED blinking base time
initial value to the AX register
      MOVW  CR000,      AX          ; Initialize the LED blinking base time
      MOV   PRM00,      #00000010B  ; Count clock = fxp/2^8 = 31.25 kHz
      MOV   TOC00,      #00000000B  ; Do not perform timer output
      MOV   TMC00,      #00001100B  ; Start the timer operation (clear & start
upon a match between TM00 and CR000)

;-------------------------------------------------------------------------
;     Set the interrupt
;-------------------------------------------------------------------------
      MOV   INTM0,      #00000000B  ; Set the valid edge of INTP1 to falling
edge
      MOV   IF0,  #00H              ; Clear invalid interrupt requests in
advance
      CLR1  PMK1                    ; Unmask INTP1 interrupts
      CLR1  TMMK000                 ; Unmask INTTM000 interrupts

      EI                            ; Enable vector interrupt

;*************************************************************************
;
;     Main loop
;
;*************************************************************************
MAIN_LOOP:
      NOP
      BR    $MAIN_LOOP              ; Go to the MAIN_LOOP

;*************************************************************************
;
;     External interrupt INTP1
;
;*************************************************************************
INTERRUPT_P1:
      PUSH  AX                      ; Save the AX register data to the stack

;-----  10 ms wait to handle chattering  -----
      MOV   A,    [HL+8]            ; Read the count value corresponding to
the timer 000 cycle
WAIT_CHAT:
      NOP
      BF    TMIF000, $WAIT_CHAT     ; Wait for the INTTM000 interrupt
      CLR1  TMIF000                 ; Clear the INTTM000 interrupt request
flag
```

```
      CALL  !SUB_INTERRUPT_TM000    ; Service the INTTM000 interrupt
      DEC   A                 ; Decrement the A register by 1
      BNZ   $WAIT_CHAT        ; Branch if not A = 0

      CLR1  PIF1              ; Clear the INTP1 interrupt request

;-----  Identification of chattering detection  -----
      BT    P4.3, $END_INTP1  ; Branch if there is no switch input

;-----  Change the TM00 interval cycle  -----
      MOV   TMC00,      #00000000B  ; Stop the timer operation

      MOV   A,    L           ; Read the lower 8 bits of the table address
      ADD   A,    #2          ; Increment the table address by 2
      AND   A,    #00000111B  ; Mask bits other than bits 0 to 2
      MOV   L,    A           ; Write to the lower 8 bits of the table address
      MOV   A,    [HL]        ; Read the lower 8 bits of the compare value
from the table
      MOV   X,    A
      MOV   A,    [HL+1]      ; Read the higher 8 bits of the compare value
from the table
      MOVW  CR000,      AX    ; Change the LED blinking base time

      MOV   TMC00,      #00001100B  ; Start the timer operation (clear & start
upon a match between TM00 and CR000)

      MOV   CNT_TM000, #250   ; Initialize the number of INTTM000 interrupts

END_INTP1:
      POP   AX                ; Restore the AX register data
      RETI                    ; Return from interrupt servicing

;*************************************************************************
;
;     Interrupt INTTM000
;
;*************************************************************************
INTERRUPT_TM000:
      CALL  !SUB_INTERRUPT_TM000    ; INTTM000 subroutine call
      RETI                    ; Return from interrupt servicing

;-------------------------------------------------------------------------
;     Subroutine for measuring the number of INTTM000 interrupts
;-------------------------------------------------------------------------
SUB_INTERRUPT_TM000:
      DBNZ  CNT_TM000, $END_INTTM000 ; Branch if the number of INTTM000
interrupts < 250
      MOV   CNT_TM000, #250   ; Initialize the number of INTTM000 interrupts

      XOR   P2,   #00000001B  ; Reverse the LED output

END_INTTM000:
      RET                     ; Return from the subroutine

end
```

● main.c (C language version)

```
/************************************************************************

      NEC Electronics     78K0S/KB1+

************************************************************************
      78K0S/KB1+  Sample program
************************************************************************
      16-bit timer 00 (interval timer)
************************************************************************
<<History>>
      2007.7.--   Release
************************************************************************

<<Overview>>

This sample program presents an example of using the interval timer function
of 16-bit timer 00.  The LEDs are blinked by reversing the P20 pin output
through the use of 16-bit timer 00 interrupts.  The LED blinking cycle is
changed by rewriting the compare register of the timer when a switch input
interrupt is generated.


  <Principal setting contents>

  - Declare a function run by an interrupt: INTP1 -> fn_intp1()
  - Declare a function run by an interrupt: INTTM000 -> fn_inttm000()
  - Stop the watchdog timer operation
  - Set the low-voltage detection voltage (VLVI) to 4.3 V +-0.2 V
  - Generate an internal reset signal (low-voltage detector) when VDD < VLVI
after VDD >= VLVI
  - Set the CPU clock to 8 MHz
  - Set the clock supplied to the peripheral hardware to 8 MHz
  - Set the valid edge of external interrupt INTP1 to falling edge
  - Set the chattering detection time during switch input to 10 ms


  <16-bit timer 00 settings>
  - Operation mode: Clear & start the timer count upon a match between TM00
and CR000
  - Not performing timer output
  - Count clock = fxp/2^8 (31.25 kHz)
  - Initial value of timer cycle = About 2 ms (32[us/clk] x 63[count] =
2.016[ms])


  <Number of switch inputs and LED blinking cycles>

    +--------------------------+
    |  SW Inputs | LED Blinking|
    |   (P43)    | Cycle (P20) |
    |------------|-------------|
    |   0 times  |    1 second |
    |   1 time   |  1/2 second |
    |   2 times  |  1/4 second |
    |   3 times  |  1/8 second |
    +--------------------------+
```

```
    # The blinking cycle from the zeroth switch input is repeated after the
fourth switch input.


<<I/O port settings>>

  Input: P43
  Output: P00-P03, P20-P23, P30-P33, P40-P42, P44-P47, P120-P123, P130
  # All unused ports are set as the output mode.

************************************************************************/


/*======================================================================

      Preprocessing directive (#pragma)

======================================================================*/
#pragma     SFR                     /* SFR names can be described at the C
source level */
#pragma     EI                      /* EI instructions can be described at the
C source level */
#pragma     NOP                     /* NOP instructions can be described at
the C source level */
#pragma interrupt INTP1 fn_intp1    /* Interrupt function declaration:INTP1 */
#pragma interrupt INTTM000 fn_inttm000    /* Interrupt function
declaration:INTTM000 */

/*======================================================================

      Declare the function prototype

======================================================================*/
void fn_subinttm000();              /* INTTM000 interrupt subroutine */

/*======================================================================

      Define the global variables

======================================================================*/
sreg unsigned char g_ucSWcnt = 0;   /* 8-bit variable for counting the number
of switch inputs */
sreg unsigned char g_ucTM000cnt = 0;      /* 8-bit variable for counting the
number of INTTM000 interrupts */
const unsigned char g_ucChat[4] = {5+1,10+1,20+1,40+1};     /* 8-bit constant
table for removing chattering */
const unsigned int g_unCR000data[4] = {63-1,32-1,16-1,8-1}; /* 16-bit constant
table for LED blinking base time */

/************************************************************************

      Initialization after RESET

************************************************************************/
void hdwinit(void){
      unsigned char ucCnt200us;     /* 8-bit variable for 200 us wait */

/*----------------------------------------------------------------------
      Initialize the watchdog timer + detect low-voltage + set the clock
```

```
------------------------------------------------------------------------*/
      /* Initialize the watchdog timer */
      WDTM  = 0b01110111;           /* Stop the watchdog timer operation */

      /* Set the clock <1> */
      PCC   = 0b00000000;           /* The clock supplied to the CPU (fcpu) =
fxp (= fx/4 = 2 MHz) */
      LSRCM = 0b00000001;           /* Stop the oscillation of the low-speed
internal oscillator */

      /* Check the reset source */
      if (!(RESF & 0b00000001)){    /* Omit subsequent LVI-related processing
during LVI reset */

            /* Set low-voltage detection */
            LVIS  = 0b00000000;     /* Set the low-voltage detection level
(VLVI) to 4.3 V +-0.2 V */
            LVION = 1;        /* Enable the low-voltage detector operation */

            for (ucCnt200us = 0; ucCnt200us < 9; ucCnt200us++){   /* Wait of
about 200 us */
                  NOP();
            }

            while (LVIF){           /* Wait for VDD >= VLVI */
                  NOP();
            }

            LVIMD = 1;              /* Set so that an internal reset signal is
generated when VDD < VLVI */
      }

      /* Set the clock <2> */
      PPCC  = 0b00000000;           /* The clock supplied to the peripheral
hardware (fxp) = fx (= 8 MHz)
                                       -> The clock supplied to the CPU (fcpu)
= fxp = 8 MHz */

/*------------------------------------------------------------------------
      Initialize the port 0
------------------------------------------------------------------------*/
      P0    = 0b00000000;           /* Set output latches of P00-P03 as low */
      PM0   = 0b11110000;           /* Set P00-P03 as output mode */

/*------------------------------------------------------------------------
      Initialize the port 2
------------------------------------------------------------------------*/
      P2    = 0b00000001;           /* Set output latches of P21-P23 as low,
P20 as high (turn off LED) */
      PM2   = 0b11110000;           /* Set P20-P23 as output mode */

/*------------------------------------------------------------------------
      Initialize the port 3
------------------------------------------------------------------------*/
      P3    = 0b00000000;           /* Set output latches of P30-P33 as low */
      PM3   = 0b11110000;           /* Set P30-P33 as output mode */

/*------------------------------------------------------------------------
      Initialize the port 4
```

```
------------------------------------------------------------------------*/
      P4    = 0b00000000;           /* Set output latches of P40-P47 as low */
      PU4   = 0b00001000;           /* Connect on-chip pull-up resistor to P43
*/
      PM4   = 0b00001000;           /* Set P40-P42 and P44-P47 as output mode,
P43 as input mode */

/*--------------------------------------------------------------------------
      Initialize the port 12
------------------------------------------------------------------------*/
      P12   = 0b00000000;           /* Set output latches of P120-P123 as low
*/
      PM12  = 0b11110000;           /* Set P120-P123 as output mode */

/*--------------------------------------------------------------------------
      Initialize the port 13
------------------------------------------------------------------------*/
      P13   = 0b00000001;           /* Set output latch of P130 as high */

/*--------------------------------------------------------------------------
      Set 16-bit timer 00
------------------------------------------------------------------------*/
      CRC00 = 0b00000000;           /* Use CR000 as a compare register */
      CR000 = 63-1;                 /* Initialize the LED blinking base time
*/
      PRM00 = 0b00000010;           /* Count clock = fxp/2^8 = 31.25 kHz */
      TOC00 = 0b00000000;           /* Do not perform timer output */
      TMC00 = 0b00001100;           /* Start the timer operation (clear &
start upon a match between TM00 and CR000) */

/*--------------------------------------------------------------------------
      Set the interrupt
------------------------------------------------------------------------*/
      INTM0 = 0b00000000;           /* Set the valid edge of INTP1 to falling
edge */
      IF0   = 0x00;                 /* Clear invalid interrupt requests in
advance */
      PMK1  = 0;                    /* Unmask INTP1 interrupts */
      TMMK000 = 0;                  /* Unmask INTTM000 interrupts */

      return;
}

/***************************************************************************

      Main loop

***************************************************************************/
void main(void){

      EI();                         /* Enable vector interrupt */

      while (1){
            NOP();
            NOP();
      }
}

/***************************************************************************
```

```
      External interrupt INTP1

************************************************************************/
__interrupt void fn_intp1(){
      unsigned char ucChat;         /* 8-bit variable for removing chattering
*/

      for (ucChat = g_ucChat[g_ucSWcnt] ; ucChat > 0 ; ucChat--){ /* Wait of
about 10 ms (for removing chattering) */
            while (!TMIF000){ /* Wait for the INTTM000 interrupt request */
                  NOP();
            }

            TMIF000 = 0;            /* Clear the INTTM000 interrupt request
flag */
            fn_subinttm000(); /* Service the INTTM000 interrupt */
      }

      PIF1 = 0;               /* Clear the INTP1 interrupt request */

      if (!P4.3){       /* Processing performed if SW is on for 10 ms or more
*/
            g_ucSWcnt = (g_ucSWcnt + 1) & 0b00000011; /* Update the number of
switch inputs */

            TMC00 = 0b00000000;     /* Stop the timer operation */
            CR000 = g_unCR000data[g_ucSWcnt];   /* Change the LED blinking
base time in accordance with the number of switch inputs */
            TMC00 = 0b00001100;     /* Start the timer operation (clear &
start upon a match between TM00 and CR000) */

            g_ucTM000cnt = 0; /* Clear the number of INTTM000 interrupts */
      }

      return;
}

/************************************************************************

      Interrupt INTTM000

************************************************************************/
__interrupt void fn_inttm000(){

      fn_subinttm000();       /* Service the INTTM000 interrupt */

      return;
}

/*-----------------------------------------------------------------------
      Subroutine for measuring the number of INTTM000 interrupts
-----------------------------------------------------------------------*/
void fn_subinttm000(){

      if (++g_ucTM000cnt == 250){   /* Processing when the number of INTTM000
interrupts is 250 */
            g_ucTM000cnt = 0; /* Clear the number of INTTM000 interrupts */
            P2 ^= 0b00000001; /* Reverse the LED output */
```

```
      }

      return;
}
```

● op.asm (Common to assembly language and C language versions)

```
;=========================================================================
;
;     Option byte
;
;=========================================================================
OPBT  CSEG  AT    0080H
        DB      10011100B       ; Option byte area
;                   ||||
;                   |||+---------- Low-speed internal oscillator can be
stopped by software
;                   |++----------- High-speed internal oscillation clock (8
MHz) is selected for system clock source
;                  +-------------- P34/RESET pin is used as RESET pin

        DB      11111111B       ; Protect byte area (for the self programming
mode)
;               ||||||||
;               ++++++++---------- All blocks can be written or erased

end
```

APPENDIX B REVISION HISTORY

The mark “<R>” shows major revised points. The revised points can be easily searched by copying an “<R>” in the PDF file and specifying it in the “Find what.” field.

Edition	Date Published	Page	Revision
1st edition	November 2007	–	–
2nd edition	September 2008	p.29	CHAPTER 5 OPERATION CHECK USING SYSTEM SIMULATOR SM+ • Modification of description in Caution ((as of August 2007) → (as of July 2008))
		pp.29 to 31	Modification of 5.1 Building the Sample Program
		p.31	5.2 Operation with SM+ • Addition of (1)
		p.36	CHAPTER 6 RELATED DOCUMENTS • Addition of Flash Programming Manual (Basic) MINICUBE2 version

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