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April 1st, 2010
Renesas Electronics Corporation

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78K0R/Kx3 Microcontroller

Sample Program

Operation Manual

(UART Reception (Serial Array Unit),

ASM Source)

This software is for reference only and NEC Electronics does not guarantee its operation.
Thoroughly evaluate this software on your set prior to use.

ZUD-CC-07-0232-E
January, 2008

1st Product Solution Group, Multipurpose Microcomputer Systems Division,
Microcomputer Operations Unit
NEC Electronics Corporation

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M8E 02. 11-1

CONTENTS

1. OVERVIEW

This manual explains the sample program functions of UART (reception mode) for the 78K0R/Kx3.

In this sample program, UART (reception mode) operation is performed.

The communication conditions are as follows.

- f_{CLK} = 20 MHz
- UART0 (unit 0, channel 1) is used.
- 9,600 bps, 8-bit data, stop bit: 1, no parity
- LSB first
- Number of receive data: 10 bytes
- Receive data: (any)
- INTSR0 reception end interrupt servicing is used.

2. RESOURCES USED

Resource	Description	Remark
Main clock specification	Internal high-speed oscillator used (8 MHz (TYP.))	Always oscillated
	High-speed system clock used (20 MHz)	Oscillated by initial processing. Supplied to CPU and peripheral hardware
Subclock	XT1 (32.768 kHz)	Oscillated by initial processing
Related hardware	Peripheral enable register 0 (PER0)	
	Serial clock select register 0 (SPS0)	Clock used: CK00 ($1/2^4$ of main clock), 1.25 MHz (0.8 μs)
	Serial mode register 00 (SMR00)	
	Serial mode register 01 (SMR01)	
	Serial communication operation setting register 00 (SCR00)	Reception only, data length: 8 bits
	Serial data register 00 (SDR00)	Transfer rate: 9,600 bps
	Serial data register 00 (SDR01)	Transfer rate: 9,600 bps
	Serial output level register 0 (SOL0)	Sets output data level.
	Serial channel start register 0 (SS0)	
	Serial channel stop register 0 (ST0)	
	Serial output register 0 (SO0)	
	Serial output enable register 0 (SOE0)	
	Port mode register 1 (PM1)	
	Port register 1 (P1)	
I/O	Data input: RxD0 (P11)	
Interrupt	Reception end interrupt (INTSR0) of UART0	
Others	Not used	

3. SOFTWARE CONFIGURATION

Files

File Name	Processing Outline	Remark
K0R_vct.asm	Vector processing	
K0R_init.asm[Note]	Initialization processing	
K0R_main.asm	Main processing	
K0R_sfr_set.asm	UART processing (reception mode)	

Note This file is commonly used by the sample programs.

4. FUNCTION EXPLANATIONS

[File name]

K0R_main.asm

Function

Function Name	Processing Outline	Argument	Return Value
MMA_STRT	Main routine	None	None

Function explanations

Function name	MMA_STRT
Processing	Main routine
Argument	–
Return value	–
Description	Executes initialization processing and then waits for receive data. Once reception has been completed, the operation is aborted and resumed after a specific time.
Remark	–

[File name]

K0R_sfr_set.asm

Functions

Function Name	Processing Outline	Argument	Return Value
UAR_RVIN	Initializes UART.	None	None
UAR_RVBK	Aborts UART operation.	None	None
UAR_RVRE	Resumes UART operation.	None	None
UAR_RVSP	Stops UART operation.	None	None
UAR_RVIT	UART reception interrupt servicing	None	None

Function explanations

Function name	UAR_RVIN
Processing	Initializes UART.
Argument	–
Return value	–
Description	Executes initialization.
Remark	–

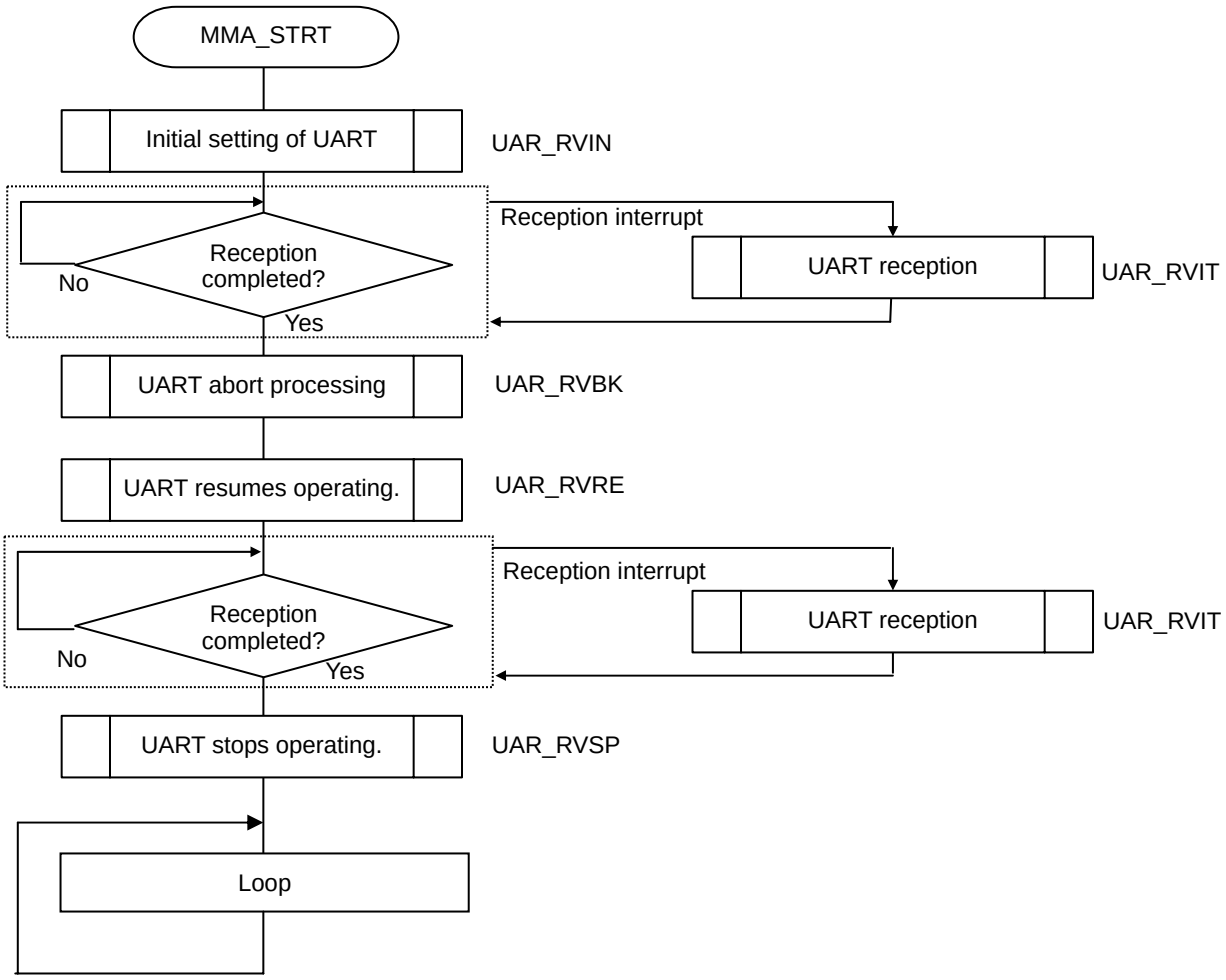
Function name	UAR_RVBK
Processing	Aborts UART operation.
Argument	–
Return value	–
Description	Transits to a communication operation stop state.
Remark	–

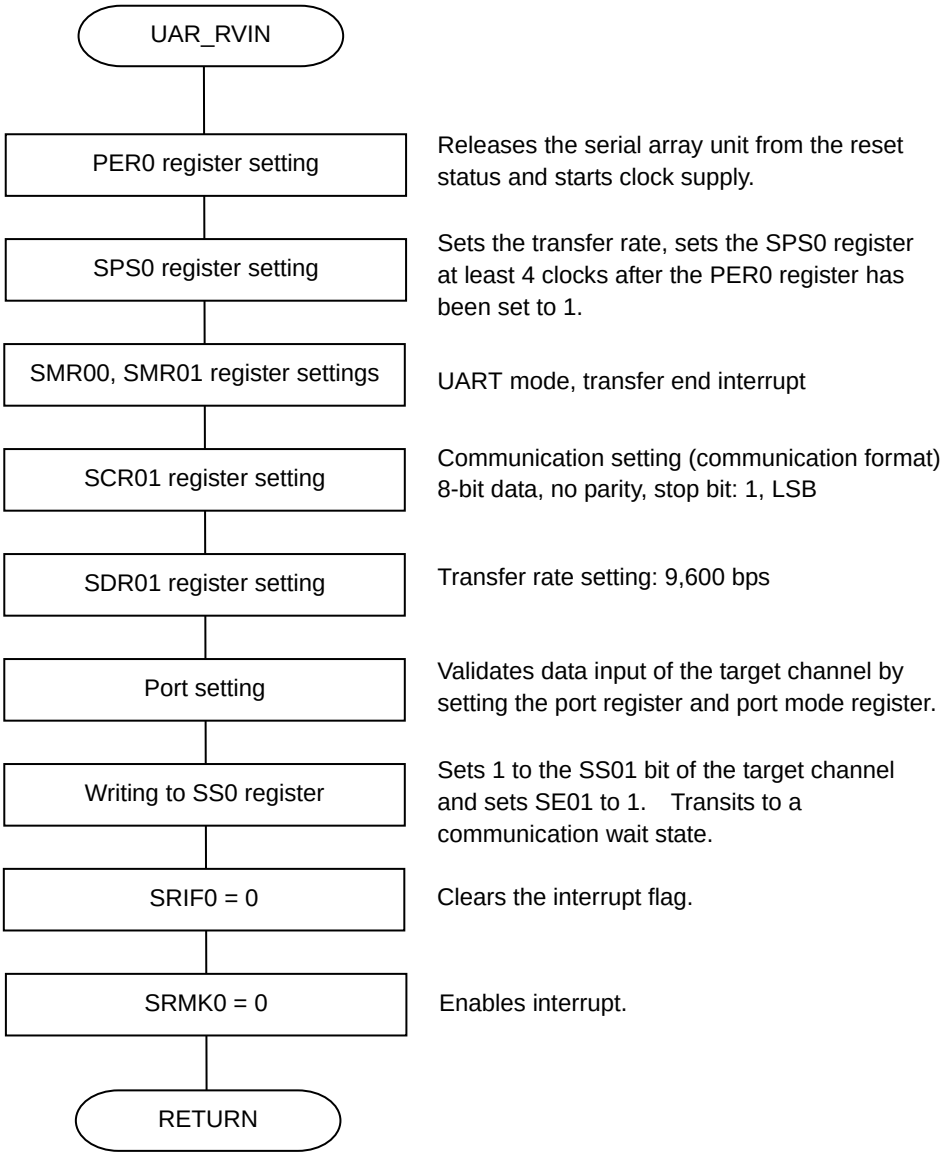
Function name	UAR_RVRE
Processing	Resumes UART operation.
Argument	–
Return value	–
Description	Resumes reception operation.
Remark	–

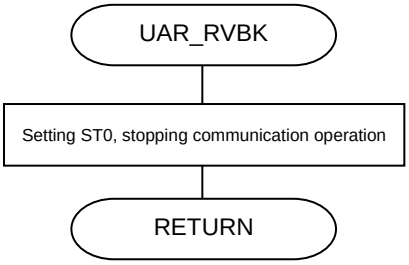
Function name	UAR_RVSP
Processing	Stops UART operation.
Argument	–
Return value	–
Description	Stops clock supply.
Remark	–

Function name	UAR_RVIT
Processing	UART reception interrupt servicing
Argument	–
Return value	–
Description	The start condition is a transfer end interrupt. An interrupt is generated when 1-byte data has been received. When 10 bytes of data have been received, a reception completion flag is set.
Remark	–

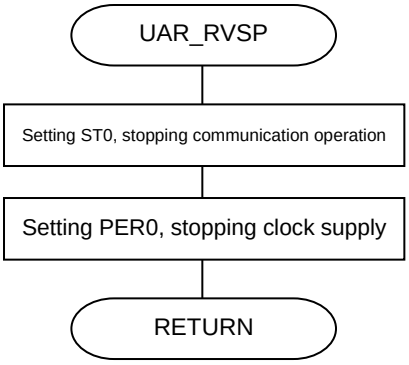
5. FLOWCHARTS




UAR_RVIN
PER0 register setting
Releases the serial array unit from the reset status and starts clock supply.
SPS0 register setting
Sets the transfer rate, sets the SPS0 register at least 4 clocks after the PER0 register has been set to 1.
SMR00, SMR01 register settings
UART mode, transfer end interrupt
SCR01 register setting
Communication setting (communication format) 8-bit data, no parity, stop bit: 1, LSB
SDR01 register setting
Transfer rate setting: 9,600 bps
Port setting
Validates data input of the target channel by setting the port register and port mode register.
Writing to SS0 register
Sets 1 to the SS01 bit of the target channel and sets SE01 to 1. Transits to a communication wait state.
SRIF0 = 0
Clears the interrupt flag.
SRMK0 = 0
Enables interrupt.
RETURN

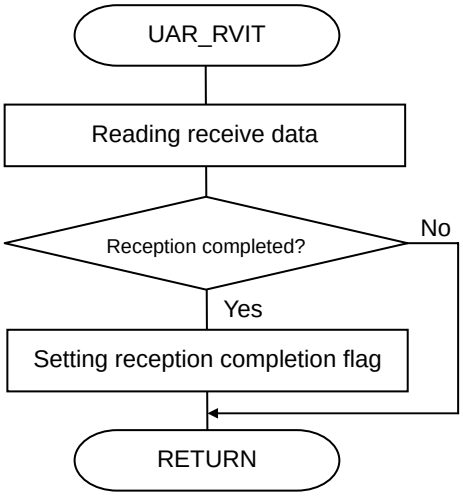


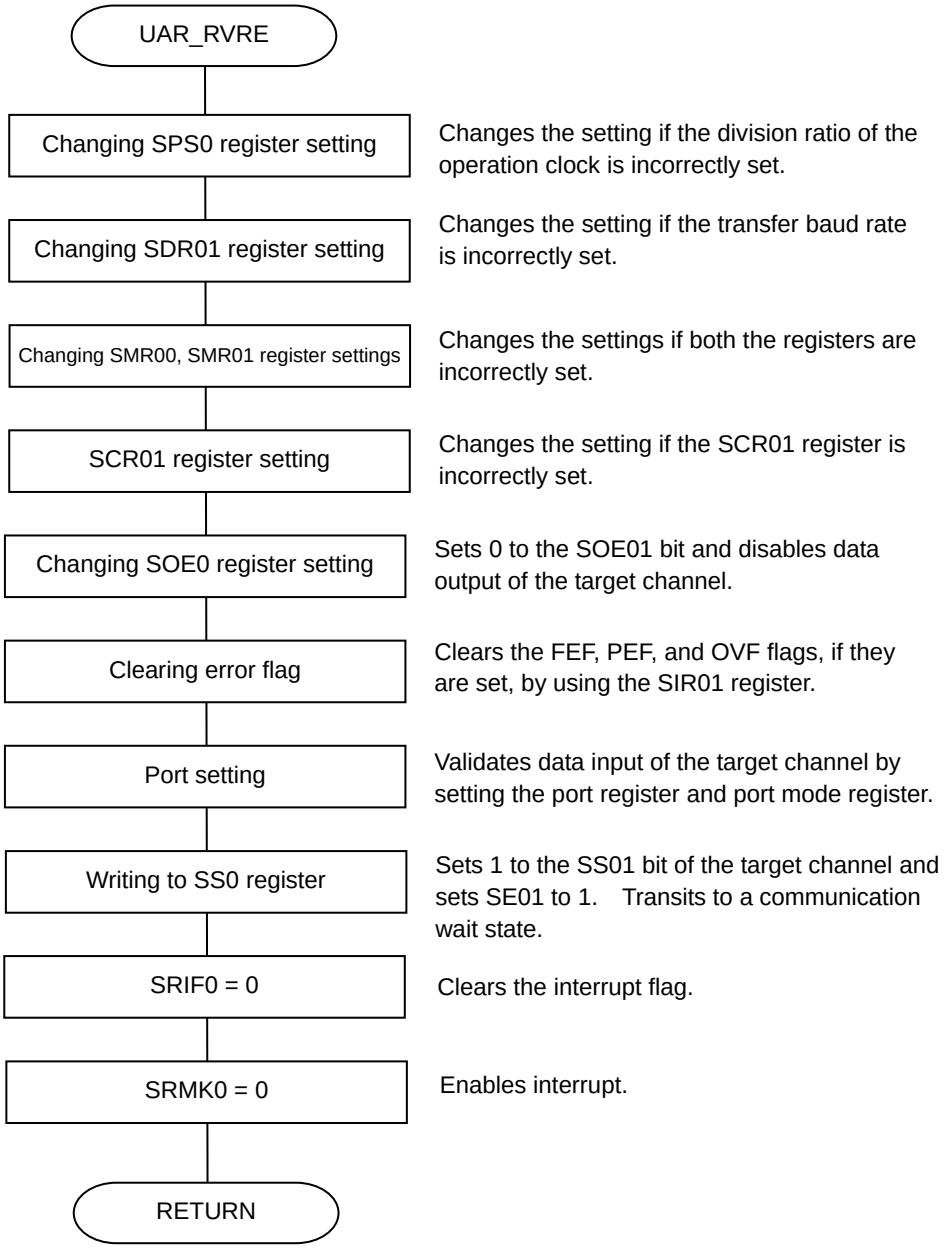
Stops communication operation.



Stops communication operation.

Stops clock supply.




UAR_RVRE
Changing SPS0 register setting
Changes the setting if the division ratio of the operation clock is incorrectly set.
Changing SDR01 register setting
Changes the setting if the transfer baud rate is incorrectly set.
Changing SMR00, SMR01 register settings
Changes the settings if both the registers are incorrectly set.
SCR01 register setting
Changes the setting if the SCR01 register is incorrectly set.
Changing SOE0 register setting
Sets 0 to the SOE01 bit and disables data output of the target channel.
Clearing error flag
Clears the FEF, PEF, and OVF flags, if they are set, by using the SIR01 register.
Port setting
Validates data input of the target channel by setting the port register and port mode register.
Writing to SS0 register
Sets 1 to the SS01 bit of the target channel and sets SE01 to 1. Transits to a communication wait state.
SRIF0 = 0
Clears the interrupt flag.
SRMK0 = 0
Enables interrupt.
RETURN