Enabling Hot-Plug with IDT PCI Express® Gen2 System Interconnect Switches

Application Note AN-720

Notes

By Bryan Le

Introduction

The PCI Express® architecture is designed to natively support both hot-add and hot-removal ("hot-plug") of adapters and provides a "toolbox" of mechanisms that allow different user/operator models to be supported using a self-consistent infrastructure. IDT PCIe® switches support hot-plug on all of its down-stream ports. There are software and hardware elements required to support the Hot Plug environment. The major software elements include the User Interface, Hot-Plug Service, Hot Plug System Driver, and Device Driver. As for major hardware elements, Hot-Plug Controller, Card Slot Power Switching logic, Card Reset logic, Power Indicator, Attention Indicator Attention Button, and Card Present Detect Pins are included.

IDT PCIe Gen2 System Interconnect switches have two ways of implementing hot-plug functionality. Some devices in this switch family offer one ore more ports that support all of the pins needed to implement hot-plug functionality in the device itself. These ports can be called on-chip hot-plug supported ports. The remaining ports can utilize an external SMBus/I^2C bus-based I/O expander connected to the master SMBus interface of the Switch for hot-plug related signals associated with downstream ports as illustrated in Figure 1.

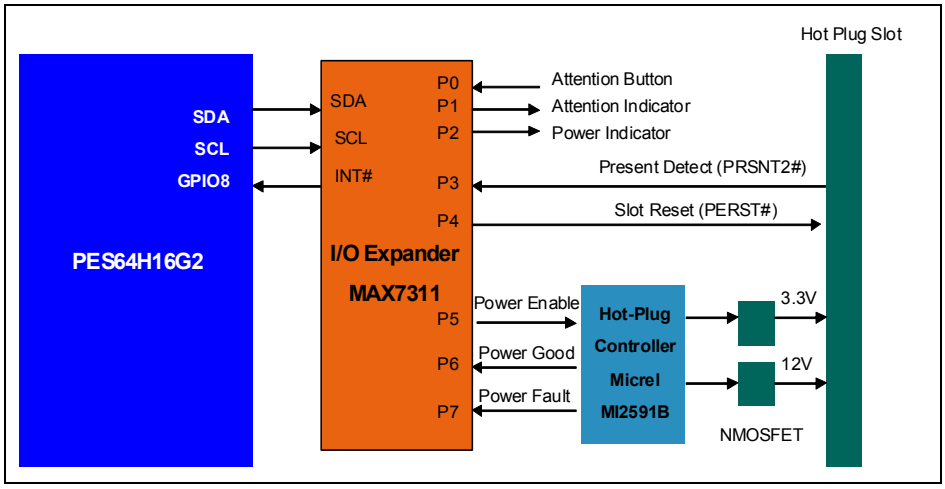

Figure 1 Hot-Plug via I/O Expander Block Diagram

The number of “on-chip” hot-plug ports varies from device to device within this family of switches. As an example, the 89HPES64H16G2 device has two such on-chip hot-plug ports. These hot-plug support pins are implemented as GPIO alternate functions and are illustrated in Figure 2.

Notes

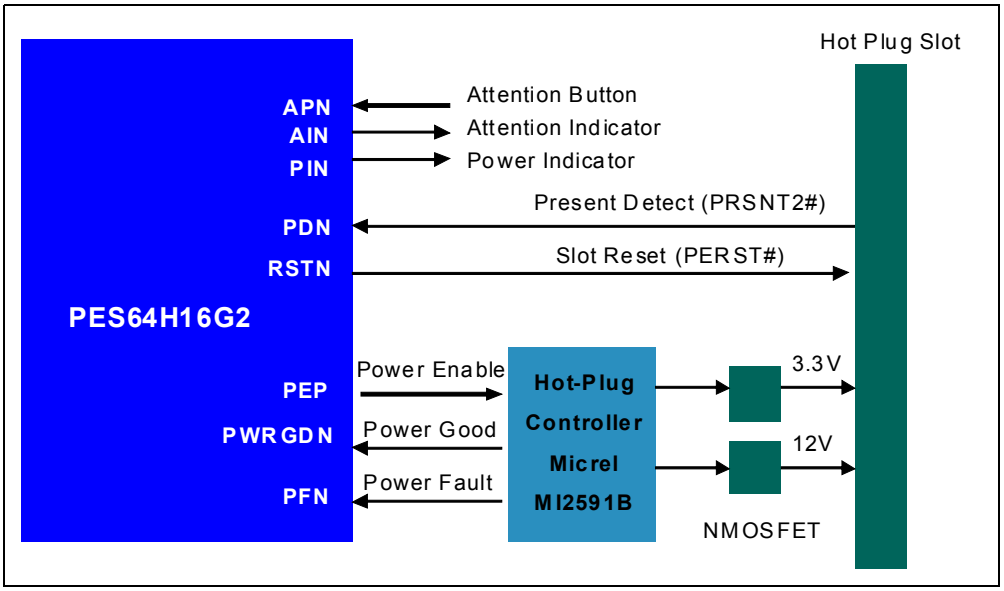

Figure 2 Hot-plug Package Pin Signals Block Diagram

This application note describes how to initialize the PES64H16G2 IDT PCIe Gen2 Switch for a hot-add and hot-removed on one of its downstream ports. This information applies to all devices in this family - PES64H16AG2, PES34H16G2, PES22H16G2, PES48H12AG2, PES48H/T12G2 and PES32H/T8G2.

I/O Expander Initialization

The PES64H16G2 utilizes an external SMBus/I^2C-bus I/O expander connected to the master SMBus interface for hot-plug related signals associated with several of its downstream ports. These I/O expander and Hot-Plug functions are disabled in default mode. Therefore, they must be enabled and initialized prior to the bus enumeration from the root complex via a serial EEPROM. An example of the registers required to prepare the PES64H16G2's Port 2 for a hot-plug process is shown in Table 1. Please refer to the PCIBrowser Manual for information on modifying the PES64H16G2 registers and programming an EEPROM.

Offset	Value	Description
0x0003E000 bit 3	b1	Set Register Unlock field to 1
0x0003EA90 bit 8	b1	Configure GPIO8 as interrupt input (from I/O Expander)
0x0003EA98	0x00000000	Select Alternate Function 0 for GPIO8
0x0003EAD8	0x00000040	Configure I/O Expander 0 Address to 0x20
0x00004040 bit 24	b1	Set Slot Implemented field to 1

Table 1 Hot-Plug EEPROM Image (Page 1 of 2)

Notes

Offset	Value	Description
0x00004054	0x0010005B	Configure PCIESCAP register - Set attention button present field to 1 Set power control present field to 1 Set attention indicator present field to 1 Set power indicator present field to 1 Set hot-plug capable field to 1 Set Physical Slot Number to 0x2
0x00004058	0x000001FB	Configure PCIESCTL register - Enable attention press button Enable power fault detect Enable presence detected change Enable command complete interrupt Turn off attention indicator Turn on power indicator
0x000040D0	0x00810005	Enable MSI

Table 1 Hot-Plug EEPROM Image (Page 2 of 2)

Table 2 shows an example of the registers required to prepare the PES64H16G2's Port 2 for a hot-plug process when the integrated hot-plug package pins are used.

Offset	Value	Description
0x0003E000 bit 3	b1	Set Register Unlock field to 1
0x0003EA90	0xF8000000	Configure GPIO27-31 as alternate function pins
0x0003EA94	0x0000000F	Configure GPIO32-35 as alternate function pins
0x0003EA9C	0x00000000	Select alternate function 0 for GPIO27-31 as hot-plug pins
0x0003EAA0	0x00000000	Select alternate function 0 for GPIO32-35 as hot-plug pins
0x00004040 bit 24	b1	Set Slot Implemented field to 1
0x00004054	0x0010005B	Configure PCIESCAP register - Set attention button present field to 1 Set power control present field Set attention indicator present field to 1 Set power indicator present field to 1 Set hot-plug capable field to 1 Set Physical Slot Number to 0x2
0x00004058	0x000001FB	Configure PCIESCTL register - Enable attention press button Enable power fault detect Enable presence detected change Enable command complete interrupt Turn off attention indicator Turn on power indicator
0x000040D0	0x00810005	Enable MSI

Table 2 Integrated Hot-plug Packages Pins EEPROM Image

Notes

Hot-Removed and Hot-Add Procedures

It should be noted that the procedures described in the following sections assume that the Hot-Plug System Driver is responsible for configuring a newly-installed device. The PCIBrowser will be used instead of the Hot-Plug System Driver to manually turn the slot power OFF/ON and to scan for newly-installed devices via the Windows Device Manager.

Turning Slot Off

The following steps ar required to turn Off a slot that is currently On:

1. Deactivate the link
2. Assert the PERST# signal to the slot.
3. Turn off REFCLK to the slot.
4. Remove power from the slot.

Turning Slot On

The following steps are required to turn On a slot that is currently Off:

1. Apply power to the slot.
2. Turn on REFCLK to the slot.
3. Deassert the PERST signal to the slot.

Hot-Removed Procedure

A number of steps must occur to prepare the software and hardware for safe removal of the card and to control indicators that provide visual evidence of the request to remove the card. The sequence of events is as follows:

1. Initiate the card removal request by pressing the slot's attention button. The PCI Express Slot Status is updated and an interrupt is generated to the root complex.
2. Power indicator LED begins blinking for 10 seconds and goes to steady off and a “Safely remove hardware” message is displayed on the Windows Desktop screen.
3. It is now safe to remove the endpoint from the hot-plug slot.

Hot-Add Procedure

The procedure for installing a new card basically reverses the steps listed above for Hot-Removed. The steps taken to insert and enable a card are as follows:

1. Install the card.
2. Notify the hot-add service that the card has been installed by pressing the attention button. The PCI Express Slot Status is updated and an interrupt is generated to the root complex.
3. Wait for the power LED to go from blinking to steady on.
4. Once link training is complete, the OS commands the Platform Configuration Routine to configure the card function by assigning the necessary resources.

Allocating Resources to Downstream Bridges

When Windows XP encounters multiple downstream bridges (as might be common when a PCIe switch is hot-plugged into a PCIe hot-plug port), all of the memory and I/O resources that are available in the upstream port are allocated to the first downstream bridge that is enumerated, which leaves no resources to assign to additional parallel downstream bridges. Functions attached to those bridges are inoperable because no resources are assigned to them. Figure 3 illustrates this situation.

Notes

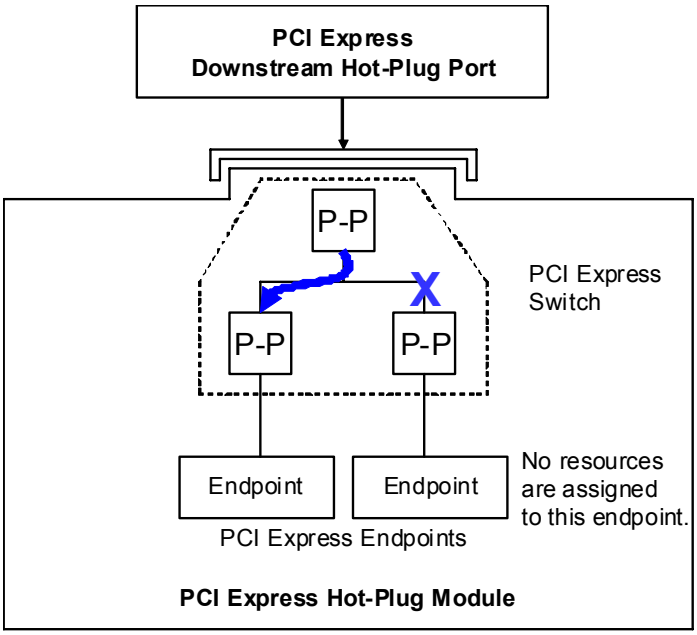

Figure 3 Bridge Resource Assignments Behind a PCIe Switch

As shown in Figure 3, all of the resources available in the upstream bridge (and elsewhere, as this is a bridge characteristic) are assigned to the downstream port on the left of the diagram. No resources are assigned to the downstream port on the right of the diagram. To prevent this, the hot-plug module must be inserted before the system is powered On. As firmware enumerates the PCIe tree, resources are assigned to all functions that are present, thus enabling the previously nonfunctional devices.

If a PCIe hot-plug module is removed after firmware has enumerated and assigned resources to the hot-plugged bridge configuration registers, Windows XP does not alter the resources that were assigned to the system board's downstream hot-plug port. But if the same module is removed and re-inserted during the same power-up session, it demonstrates the same starvation of resources described above.

Resources

IDT 89HPES64H16G2 User Manual

Firmware Support for PCI Express Hot-Plug and Windows

PCI Express Base Specification Revision 2.0

IDT PCIBrowser Manual

Revision History

July 20, 2009: Initial publication.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

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