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DUAL-PORT POWER
DISCUSSION

*APPLICATION
NOTE
AN-255*

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Power consumption on the dual-port higher I/O count devices

This application note refers to the current generation synchronous 32K x 36 dual-port family (IDT70V3579, IDT70V3569, IDT70V3379, and the IDT70V3389). These formulas can be adapted for other dual-ports.

The data sheet for these devices specifies the dynamic operating current (I_{DD}) for these devices as 375mA typical, 460mA maximum. These values are significantly larger than the associated values on IDT's smaller I/O count 3.3V synchronous dual-ports, and so warrant further explanation. It is important to keep in mind the two different currents we are discussing. There is the current the chip actually uses vs. the current consumed by the I/O bus. The 375mA is a combination of the AC and DC components of the circuit.

This application note discusses the power dissipation on the I/O bus of the 70V3579 (32K x 36).

Background

The most significant factors driving the increase in current are the increase in operating speed (from 66MHz to 133MHz), the expansion in width (from 16-bits to 18-bits and 36-bits), and their additional internal data bus. In order to drive a higher number of I/Os at increased frequency on the same supply voltage, one must increase the operating current. When designing this family of devices, IDT made operating speed and quality of signal the primary goals, allowing some increase in the operating current in order to guarantee solid performance at 133MHz.

Temperature

For completeness, the effect of operating temperature on current should be discussed. The I/O current stays constant regardless of the operating temperature. The core current (I_{DD}) varies by the operating temperature. Figure 1 shows the values for the 70V3579 core current versus temperature.
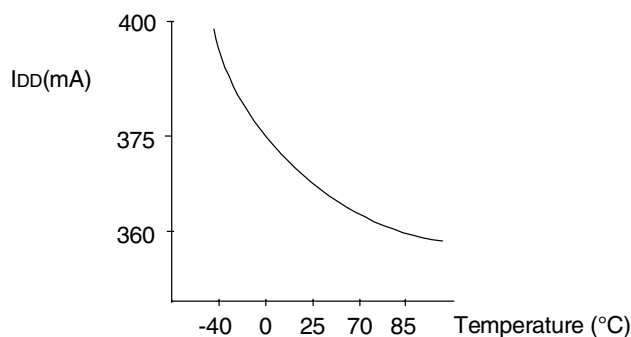

Figure 1.

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Power dissipation: Core vs. I/O

The maximum value indicated for I_{DD} in the data sheet is the worst case value with outputs disabled. It assumes both ports on the chip are enabled, outputs disabled, and frequency is at its maximum level. Worst case power dissipation for the core occurs when both ports are writing continuously at maximum frequency to the memory array. Worst case power dissipation for the I/O bus occurs when both ports are reading continuously at maximum frequency from the array. Since the typical usage for the dual-ported SRAM is normally 50% reads and 50% writes, it is unlikely that either worst-case condition will occur for a significant amount of time.

Statistical I/O Power

Whether a port is reading or writing, the worst case I/O power dissipation occurs when 100% of the I/Os are toggling their logic state at maximum possible frequency. This is unlikely to happen in a typical application.

An I/O can only do one of two things. It can stay in the same logic state, or it can change logic states. By extension, in normal operations, one may assume that the statistical average for all I/O pins changing their logic state at maximum frequency is much closer to 50% than 100%.

Frequency explanation for different cases

Since the worst case power dissipation for the I/O bus occurs during read operations, we will examine these in more detail.

t_{CYC} is the clock cycle in ns. Frequency = $\frac{1}{t_{CYC}}$. If, $t_{CYC} = 7.5$ns then, frequency (f_{CYC}) = $\frac{1}{7.5ns}$ = 133MHz. $2t_{CYC} = 2 \times 7.5$ = 15ns therefore the frequency ($\frac{f_{CYC}}{2}$) = $\frac{1}{15ns}$ = $\frac{133}{2}$ = 66.5MHz.

As Figure 2 indicates, for power dissipation on the I/O bus the theoretical maximum I/O frequency is $2t_{CYC} = \frac{1}{15ns} = \frac{133}{2}$ MHz = 66.5MHz. The clock frequency (f_{CYC}) is 133MHz. The I/O frequency is the time to go from an I/O "1" to an I/O "0", back to a "1", or vice versa. Therefore the maximum I/O cycle frequency is $\frac{f_{CYC}}{2}$ = 66.5MHz. This occurs when both ports are reading and all bits are changing.
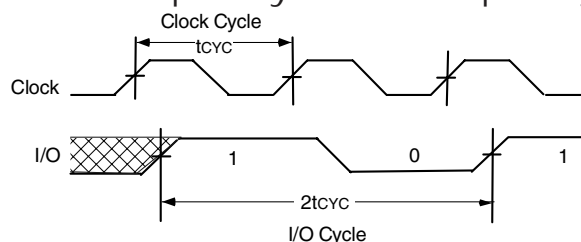
Clock frequency vs. I/O frequency

Figure 2.

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The next case to consider is both ports reading with half the bits changing. The statistical I/O cycle frequency is $\frac{133}{4}$ MHz = 33.25. As indicated above the maximum I/O cycle frequency is $\frac{133}{2}$. Since typically only half the bits change the I/O cycle frequency becomes 50% of $\frac{133}{2}$ MHz.

A more typical case will be the same number of reads and writes with the probability that only half of the bits will be changing at one time, therefore the effective I/O frequency becomes $\frac{133}{8}$ MHz = 16.625MHz.

This is summarized in Table 1.

Power dissipation formula

To calculate the power dissipation here is one common formula:

Power Dissipation = NC$(\Delta V)^2$fequiv
current = NC ΔV fequiv

N = number of outputs loaded with C (reading)
C = capacitance (load + pin)
ΔV = change of voltage on capacitor when switching an I/O pin
fequiv = frequency of signal switching (I/O not clock)

For C, we will use 20pF: 10pF for the load and 10pF for the pin. For ΔV, we will use 3.45: GND to V$_{DD}$. If your system has noise use the actual change of voltage. 3.45V is the maximum value. Typical should be closer to 3.3V.

PD max = 72 x 20pF x $(3.45V)^2$ x $\frac{133}{2}$ MHz
= 72 x $(20x10^{-12})$F x 11.9025V^2 x $(66.5x10^6)$Hz
= 1.14 watts

Refer to Table 1 for different cases.

for C = 20pF ΔV = 3.45V (ΔV^2 = 11.9025)

	All I/O Switching Both Ports Reading	50% of Bits Changing Both Ports Reading	All I/O Switching One Port Reading	50% of Bits Changing 50% Reads and Writes
Name	PD max			PD statistical
N	72	72	36	72
fequiv	$\frac{133}{2}$ MHz	$\frac{133}{4}$ MHz	$\frac{133}{2}$ MHz	$\frac{133}{8}$ MHz
PD	1.14W	.57W	.57W	.285W
current	330mA	165mA	165mA	83mA
Operation	On/Off Test Pattern Reading	Random Reads Both Ports	On/Off Read from One Port	Normal Operation

Table 1. I/O Power Dissipation

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Summary

It should be noted that during actual operation, patterns occur in data. Depending on the pattern, the power dissipation could be even lower for the I/O's.

If we revisit the statement about statistical average, the frequency has been shown to be closer to 12.5% (i.e. $\frac{133}{8}$ MHz) than 100% (i.e. 133MHz).

It is important to keep in mind that the actual current used in a design will be the dynamic operating current (I$_{DD}$) plus the current required when reading ($\overline{OE}$ = V$_{IL}$). The statistical value will be closer to 450mA (375mA+83mA). The current can even be lower as the temperature increases as shown in Figure 1.

If the customer is using this family of devices in an application where power consumption is critical, then the following measures will help to meet those goals:

– Avoid excessive capacitive loading (ideally, use 20 pF or less)
– Hold V$_{DD}$/V$_{DDQ}$ to 3.3V or less (no lower than 3.15V)
– Ensure an adequate decoupling strategy

These measures, in conjunction with the considerations described above, allow for high frequency operations in wider bus widths while keeping power consumption at reasonable levels.

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