THE MOST COMMONLY ASKED QUESTIONS ABOUT SYNCHRONOUS DUAL-PORT SRAMS

APPLICATION NOTE AN-254

By Cheryl Brennan

What is a dual-port?

A dual-port SRAM is a single static RAM array with two sets of address, data, and control signals (typically left and right) for accessing that array.

What is a synchronous dual-port?

As the need for increased bandwidth has evolved greater internal operating speed in dual-ports was needed. The solution was introduced by IDT in 1992. Synchronous dual-ports use external clocking and internal counters to allow designers to run at faster speeds than that which can be achieved from standard asynchronous dual-ports. These dual-ports respond to the rising edge of the clock signal in order to implement changes to address and control pins.

What are the differences between the Flow-through and Pipelined synchronous options?

The difference can be summed up in two words. Registered outputs. When in a Pipelined mode the device has a registered output (refer to Figure 1). This causes a one clock cycle latency for the first read cycle of burst READs. Data moves into the input and output registers on the same clock edge. Since there is no output register on the Flow-through mode, the data is read on the same clock edge (refer to Figure 2).

The benefit of pipeline access is a very fast clock-to-data access time (as fast as 4.2ns on our 133MHz dual ports). The benefit of flow-through is no latency on the first read in a burst. There is no difference between Flow-through and Pipelined mode when doing a write.

Refer to Table 1 for the Flow-through and Pipelined Offerings.

Flow-through vs. Pipelined

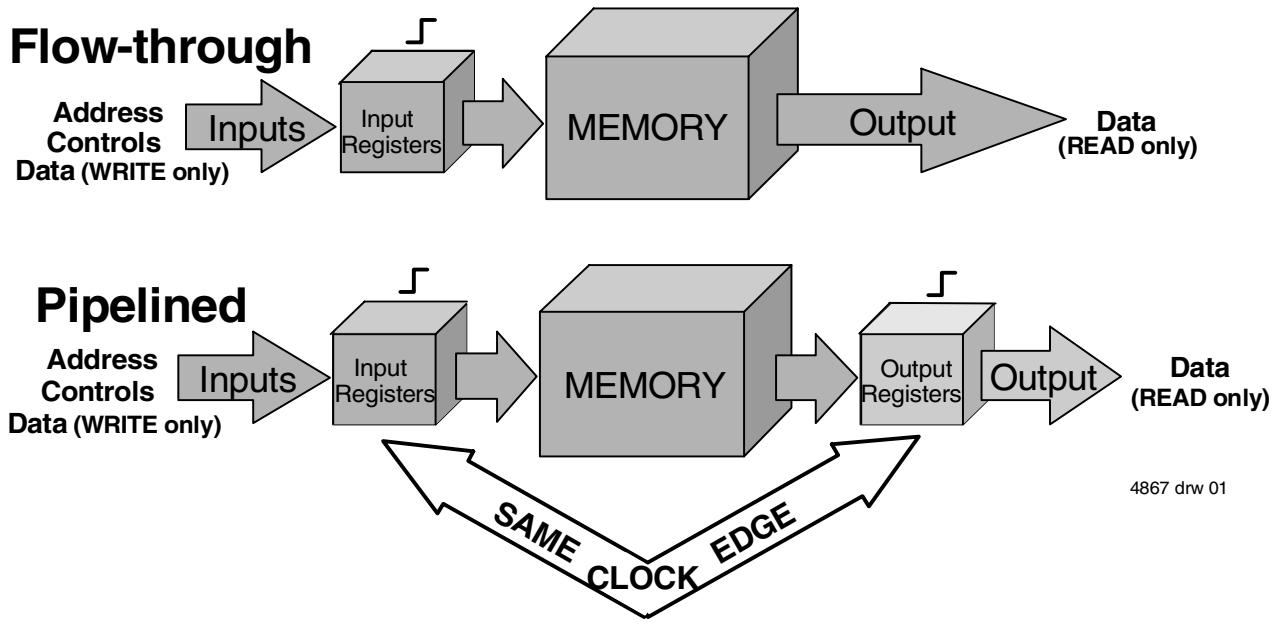

Figure 1.

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How do you put the part in these different modes?

Refer to Table 1.

- Most of our synchronous devices have the option of being pipelined or flow-through on porth ports.
- The devices listed as PL are Pipelined only.
- The devices listed as FT are Flow-through only.

Whay are the packages larger than the pin count needed?

It was determined by IDT designers that in order to achieve the higher speeds needed by board designers we needed to make our parts fast and quiet. To achieve this objective our 3.3V offerings have additional ground and power pins. Also we found many of our customers like the ability to have drop-in upgrades for future generations. Some of the current NC pins will support these future upgrades.

What are the different pin configurations used?

IDT's older generation of products have what we refer to as a legacy pinout, where left port and right port I/Os were separated on opposite sides of the device. In order to achieve speeds greater than 100MHz, it was determined that a different I/O pinout scheme was needed. The IDT chip designers chose to interleave our I/Os. This optimizes speed by equalizing internal transmission lines.

Refer to Table 1 for the interleaved vs. legacy pinout offerings.

Flow-through vs. Pipelined READ (Cycle Time Comparison)

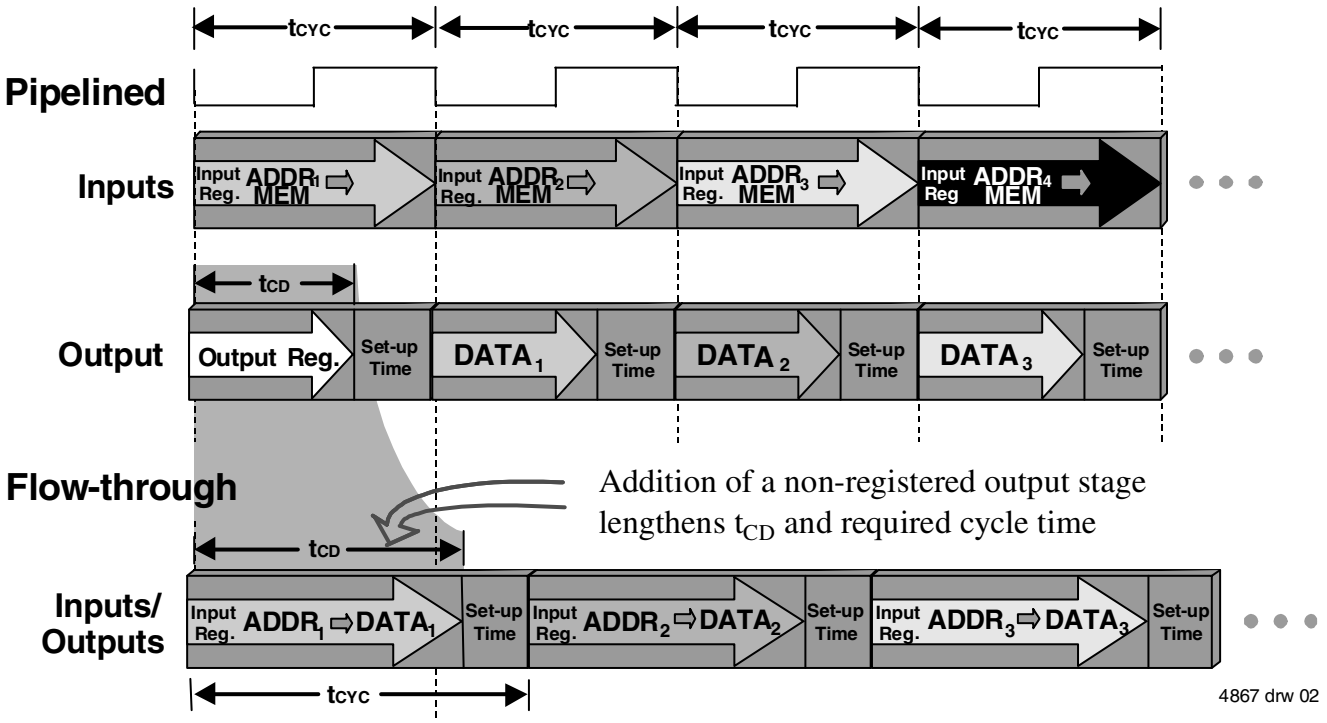

Figure 2.

Device	Config	Voltage	FT/PL	Pkg	Pinout	Speed
709079	32Kx8	5V	PL/FT	PN100	Legacy	66MHz
70V9079	32Kx8	3.3V	PL/FT	PN100	Legacy	66MHz
709089	64Kx8	5V	PL/FT	PN100	Legacy	66MHz
70V9089	64Kx8	3.3V	PL/FT	PN100	Legacy	66MHz
709099	128Kx8	5V	PL/FT	PN100	Legacy	83MHz
70V9099	128Kx8	3.3	PL/FT	PN100	Legacy	100MHz
70914	4Kx9	5V	FT	PN80/PL68	Legacy	66MHz
709149	4Kx9	5V	PL	PN80	Legacy	75MHz
709189	64Kx9	5V	PL/FT	PN100	Legacy	83MHz
70V9189	64Kx9	3.3V	PL/FT	PN100	Legacy	100MHz
709199	128Kx9	5V	PL/FT	PN100	Legacy	83MHz
70V9199	128Kx9	3.3V	PL/FT	PN100	Legacy	100MHz
709269	16Kx16	5V	PL/FT	PN100	Legacy	66MHz
70V9269	16Kx16	3.3V	PL/FT	PK128	Legacy	66MHz
709279	32Kx16	5V	PL/FT	PN100	Legacy	66MHz
70V9279	32Kx16	3.3V	PL/FT	PK128	Legacy	66MHz
709289	64Kx16	5V	PL/FT	PN100	Legacy	83MHz
70V9289	64Kx16	3.3V	PL/FT	PK128	Legacy	100MHz
70V3379	32Kx18	3.3V	PL	PK128/BF208	Interleaved	133MHz
709379	32Kx18	5V	PL/FT	PN100	Legacy	83MHz
70V9379	32Kx18	3.3V	PL/FT	PK128	Legacy	100MHz
70V3389	64Kx18	3.3V	PL	PK128/BF208	Interleaved	133MHz
709389	64Kx18	5V	PL/FT	PN100	Legacy	83MHz
70V9389	64Kx18	3.3V	PL/FT	PK128	Legacy	100MHz
70V3569	16Kx36	3.3V	PL	DR208/BF208/BC256	Interleaved	133MHz
70V3579	32Kx36	3.3V	PL	DR208/BF208/BC256	Interleaved	133MHz

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Table 1.

How do you handle depth and width expansion?

The best way to approach this may be to take each case individually. This does not preclude the fact that these devices can be placed in an array in which both depth and width expansion is performed, exactly like a standard SRAM array.

Depth expansion

Figure 3 depicts the connections required to expand a device like this in depth. It is very straight forward, and is handled exactly as you would a standard SRAM.

Width expansion

Figure 4 depicts the connection required for width expansion. Here again the devices are connected exactly as you would a standard SRAM.

What parts are pin compatible for upgrades in depth?

It is important when designing for this type of upgrade that all functions be investigated. These devices have the same package and almost the same pinout.

Here are your options:

- 70914 and 709149 (4K x 9) are stand-alone devices.
- 709079 (32K x 8) TQFP is able to be upgraded to 709089 (64K x 8) and 709099 (128K x 8).
- 709189 (64K x 9) TQFP is able to be upgraded to 709199 (128K x 9).

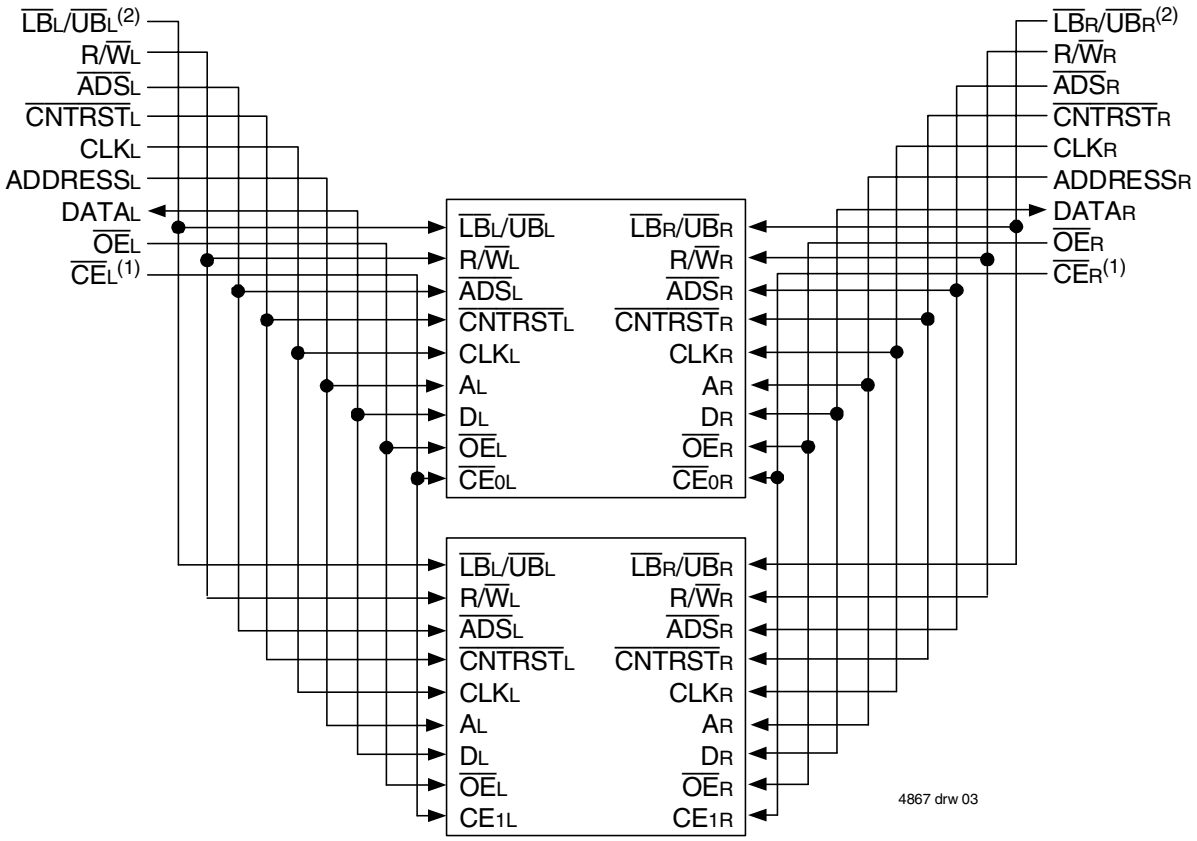

Figure 3. Depth Expansion

NOTE:
1. $\overline{CE}$ is the last address number.
2. The x36 devices have $\overline{BE}_{0-3}$.

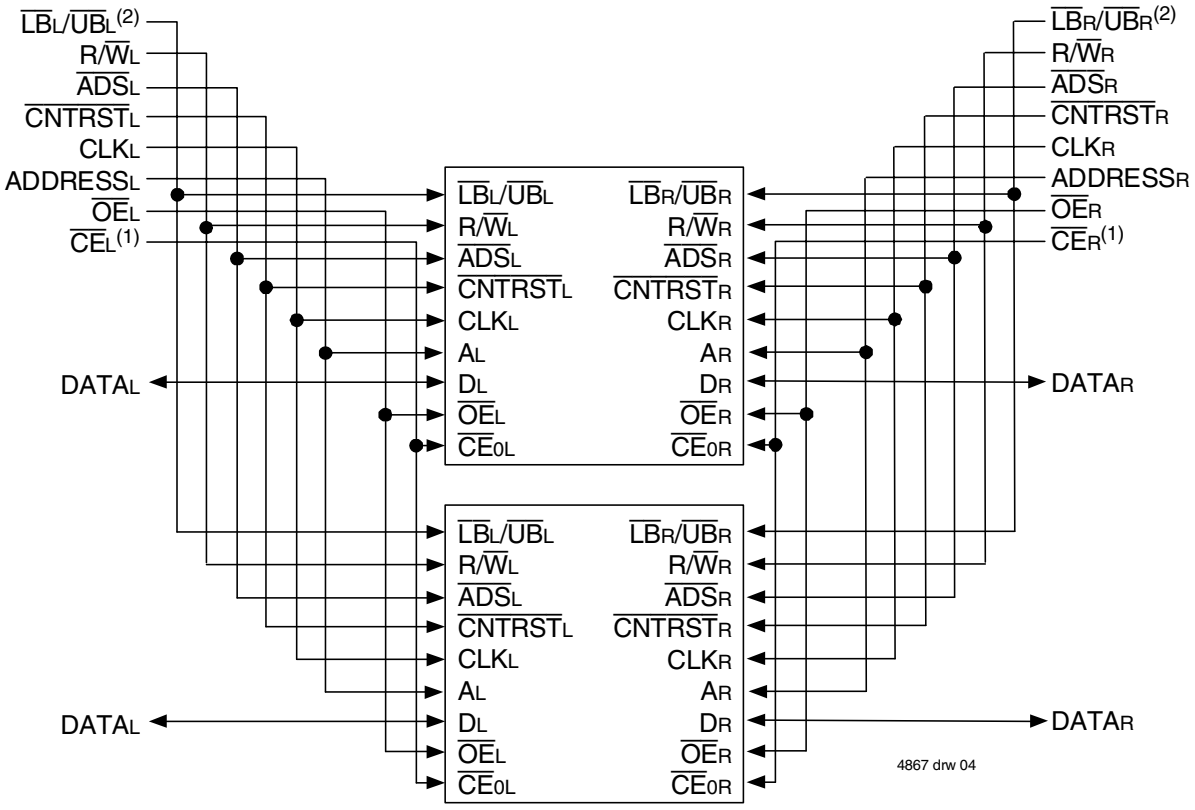

Figure 4. Width Expansion

NOTE:
1. $\overline{CE}$ is the last address number.
1. The x36 devices have $\overline{BE}_{0-3}$.

- 709269 (16K x 16) TQFP is able to be upgraded to 709279 (32K x 16) and 709289 (64K x 16).
- 70V9269 (16K x 16) RTQFP is able to be upgraded to 70V9279 (32K x 16) and 70V9289 (64K x 16).
- 709379 (32K x 18) TQFP is able to be upgraded to 709389 (64K x 18)
- 70V9379 (32K x 18) PQFP is able to be upgraded to 70V9389 (64K x 18)
- 70V3379 (32K x 18) is able to be upgraded to 70V3389 (64K x 18).
- 70V3569 (16K x 36) is able to be upgraded to 70V3579 (32K x 36).

As with any summary, this is a snapshot in time and will be continually updated.

Are there any special layout considerations I should take in using a device in which 16 or 18 outputs can be switching at once?

In short, YES.

The first thing to remember about any of IDT's devices is that they are CMOS devices. Because of this, a number of standard design practices should be followed, some of these are as follows:

1) **Do not leave any inputs floating or undetermined.** This means that all inputs are recommended to be either driven at all times or pulled through a resistor to V_{CC} or GND. This is even true if the device is driven by a tri-state driver that will tri-state for any period of time. If this practice is not followed, both the pull-up and pull-down stages on the input of the device can turn on simultaneously, causing the device to draw an extreme amount of current and/or causing the device to oscillate.

2) **Use a good decoupling scheme for the device.** Here again, if the specifications of the device are examined closely, it is clear that, when

enabled, the almost instantaneous current requirement of the device can go from as little as a few hundred micro amps to close to 200mA. With this type of current requirement it is necessary to consider the value of the capacitor (standard values like 0.1µF and 0.01µF work well most of the time), as well as the frequency response of the capacitor. It is best to decouple at least every device and, if the device has multiple V_{CC} inputs, one for each of these is ideal. I am sure that there are a few who would like to argue over where the capacitor should be placed, near the V_{CC} or near the GND. I am merely suggesting that decoupling should be used as liberally as possible.

3) Somewhere on the board there should be some bulk decoupling such as a large tantalum capacitor. This is usually placed near the power input for the module and helps decouple low frequency backplane and power supply noise from the board.

4) V_{CC} and GND planes are still considered a recommendation but should be considered a necessity. The planes are needed as a source and sink for current, as a means for controlling etch impedance,and isolating critical signals from cross-coupling.

5) Capacitive loading effects on address access time is a tricky question. In general, the RAM-based products from IDT tend to derate at an average of .05ns/pF over the specified data sheet load. In the case of the CMOS RAMs this is 30pF. So if an output on your RAM has 50pF of load the access time would be [t_{AA} + (50-30)*.05] = (T_{aa}+1ns).

Why should I use a dual-port over a RAM and some logic?

The potential benefits of using dual-ports are:

a) Performance
b) Improved Bandwidth
c) Logic savings
d) Power savings
e) Reliability improvements
f) Upgrade path
g) Design time

Let's discuss each of these topics individually:

Performance/Improved Bandwidth

CPU's must take turns for access to the SRAM, requiring two cycles plus the delay associated with multiplexing. Access to the dual-port is simultaneous, effectively doubling the bandwidth. Typically, a multiplexed SRAM must operate at 3ns to acheive bandwidth equivalent to a 10ns dual-port.

Logic savings

The logic savings are relatively straightforward. If the functionality of the dual port RAM is duplicated using SRAM, the design would require some form of comparator, which could get rather large if it were to compare every address. At a minimum some form of arbitration logic is required. There are many schemes to this with some of the more basic approaches being handled in a PAL, as with any scheme like this, questions of metastability and settling time must be addressed.

It is also a hidden factor that the cost of a logic solution may look a slight bit less expensive but if you add in the additional board savings, PAL documentation, PAL fusing, parts inventory, and manufacturing cost, you will find a significant savings in designing with a device like a dual port.

Power savings

The actual amount of power savings will be purely dependant on how complex the support logic has to be around the SRAM array. If there is a requirement of full address arbitration and/or any of the other logic functions, such as semaphore logic, it can get quite extensive. For instance, if PALs are used to perform these functions, the higher speed PALs can draw significant current.

Reliability improvements

The reliability (MTBF) of a circuit is dependent on many factors such as circuit complexity, power dissipation, number of pins, maturity of product, and even the P.C. board used. In many of these systems a dual port can be a plus. As mentioned earlier, it is very possible that the complexity of a logic implementation of this device can be quite high. This could significantly impact the MTBF of your design.

Upgrade path

As mentioned earlier, many of the dual-port products provide a range of densities and many of them are pin-compatible. This provides an easy upgrade path. In addition multiple speed grades are available which allow for additional circuit margining in the same footprint

Design time

Here again, the thought is not to say that the design of the logic surrounding a dual-ported memory is incredibly complex, but it can take a significant amount of time to design, simulate, create timing diagrams, PAL equations, do the board layout, and system debug. It can lead to a loss of design time for other more complex portions of your design. As with many functions these days, a greater amount of integration leads to faster, more confident, design times, with less time spent on the standard functions like RAM arrays.

What advantage does a dual-port have over a FIFO?

Dual-ports have a very similar set of usages as does a FIFO when the applications of a dual port are examined. It can be used for passage of critical data from one higher speed device to a slower device, it can be used to pass data in multiprocessor environments, etc. But the major advantage of a dual-port is that the data is accessible in a random fashion, and is retrievable if multiple reads of the same data is required. A FIFO allows only sequential access of the data and in most cases the data can be read only once.

What Applications Do You See These Devices Going Into?

As far as IDT is concerned, dual ports should be used in every electronic device known to man. In actuality there are some key areas that we have been strong in and others that just make sense for a device like this. Some examples of these are:

- Cellular Base Stations
- Cellular Handsets
- Multi-Protocol Routers
- Internet Appliances
- LAN/WAN Switches
  - ATM
  - Ethernet
  - Fast Ethernet
  - Gigabit Ethernet
- PBXs
- RAIDs
- Set-top Boxes
- Video Conferencing
- Audio Video Editing
- Call Distribution Systems
- Graphics Accelerators
- Ultrasound Imaging
- Satellite Encoders
- Cable Modems
- Aerospace Instrumentation
- Flight Simulators
- Industrial Controls

Wherever data needs to be shared between "thinking" devices.

Summary

Many different concerns regarding the use of dual ports have been addressed here. It you have more, please contact your local IDT applications engineer. We hope that these questions have shed some light for you into how the dual ports offered by IDT operate. Good luck designing!

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