

Abstract

Crossbar switches are essential components of high-speed data transmission applications such as computer backplanes, LAN's, digital voice, and serial digital video. The QuickSwitch CMOS Bus Exchange Switch by Quality Semiconductor is a high-speed TTL bus connect device with nibble swap capability that can be used as a high-speed, low power, low cost crossbar switch.

Background

Figure 1 shows the QS3383 bus exchange switch used to connect four CPUs and four memories in a crossbar configuration. By appropriate selection of the QS3383 bus exchange controls, this configuration provides a non-blocking architecture that makes all memories available to all CPUs, but prevents multiple CPUs from accessing the same memory simultaneously and vice versa. A 2 x 3 matrix of QS3383 bus exchange switches is required for the 4-way crossbar shown below. A 3 x 4 matrix

will be required for a 6-way crossbar, 4 x 5 for an 8-way, etc.

Bus reconfiguration time is independent of crossbar size and is less than 6.5ns. Since the QuickSwitch is bidirectional, no additional setup time is required for direction control. Propagation delay through the crossbar is less than 250ps per layer of QuickSwitch which allows the 4 x 4 crossbar example shown below, to have a total propagation delay of less than 75ps. This represents almost no delay difference from direct connection of the RAM to the CPU.

The QuickSwitch introduces no skew of its own so the CPU sees a simple RAM interface without the complicated timing skew requirements which might be imposed by using bus transceivers instead of 3383 switches. Also, the QuickSwitch is very low power, consuming less than 10mW per device when in the data transmission mode.

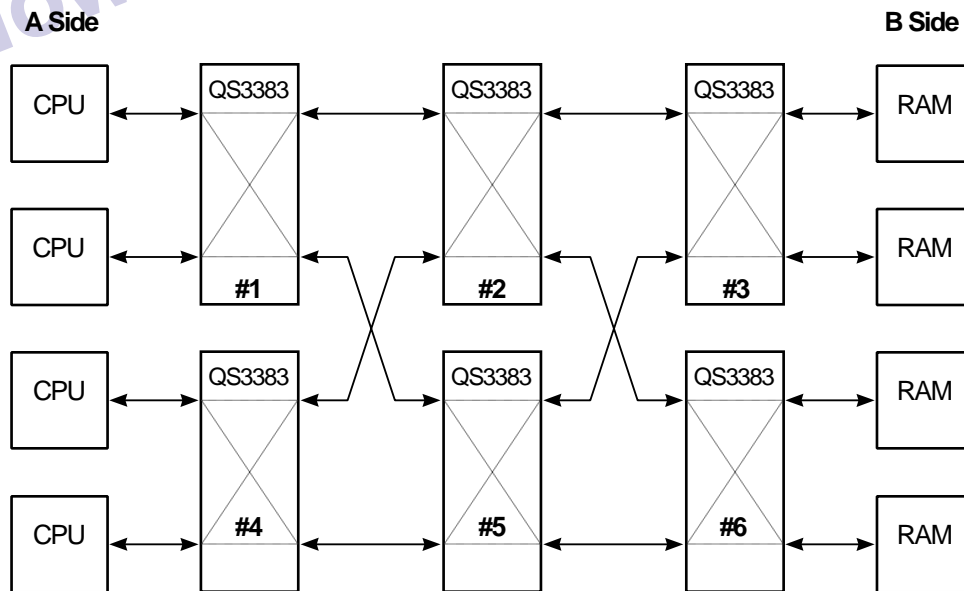


Figure 1. 4 x 4 Crossbar Using QuickSwitch

QuickSwitch for Crossbar Is Easy to Use

In the example of the 4 x 4 crossbar switch in Figure 1, each QS3383 depicted has 5-bit connect/exchange capability. Using the two control pins for each QS3383 QuickSwitch (\overline{BE} for bus enable, BX for bus exchange), it is possible to provide connection from any combination of CPUs to any combination of RAMs, while at the same time not allowing any CPUs to be connected to two RAMs simultaneously or vice versa. The number of possible combinations

for a crossbar switch is $N!$ ($1 \times 2 \times 3 \times \dots \times N$) where N equals the size of the crossbar switch. In the example of the 4 x 4 crossbar switch, N equals four. The 24 possible combinations ($1 \times 2 \times 3 \times 4 = 24$) for connecting the four CPUs to the four RAMs of Figure 1 are listed below along with the polarity required on each of the QuickSwitches to make the connections.

| 4 x 4 Crossbar Connection Combinations | QS3383 BX pins | | | | | |
|---|----------------|----|----|----|----|----|
| | #1 | #2 | #3 | #4 | #5 | #6 |
| A1B1, A2B2, A3B3, A4B4 | 0 | 0 | 0 | 0 | 0 | 0 |
| A1B1, A2B2, A3B4, A4B3 | 0 | 0 | 0 | 0 | 0 | 1 |
| A1B1, A2B3, A3B2, A4B4 | 0 | 0 | 0 | 1 | 1 | 1 |
| A1B1, A2B3, A3B4, A4B2 | 0 | 0 | 0 | 0 | 1 | 1 |
| A1B1, A2B4, A3B2, A4B3 | 0 | 0 | 0 | 1 | 1 | 0 |
| A1B1, A2B4, A3B3, A4B2 | 0 | 0 | 0 | 0 | 1 | 0 |
| A1B2, A2B1, A3B3, A4B4 | 0 | 0 | 1 | 0 | 0 | 0 |
| A1B2, A2B1, A3B4, A4B3 | 0 | 0 | 1 | 0 | 0 | 1 |
| A1B2, A2B3, A3B1, A4B4 | 1 | 1 | 0 | 0 | 0 | 0 |
| A1B2, A2B3, A3B4, A4B1 | 1 | 1 | 0 | 1 | 0 | 0 |
| A1B2, A2B4, A3B1, A4B3 | 1 | 1 | 0 | 0 | 0 | 1 |
| A1B2, A2B4, A3B3, A4B1 | 1 | 1 | 0 | 0 | 1 | 1 |
| A1B3, A2B1, A3B2, A4B4 | 1 | 0 | 0 | 1 | 1 | 1 |
| A1B3, A2B1, A3B4, A4B2 | 1 | 0 | 0 | 0 | 1 | 1 |
| A1B3, A2B2, A3B1, A4B4 | 1 | 0 | 1 | 1 | 1 | 1 |
| A1B3, A2B2, A3B4, A4B1 | 1 | 0 | 1 | 0 | 1 | 1 |
| A1B3, A2B4, A3B1, A4B2 | 1 | 1 | 0 | 0 | 1 | 1 |
| A1B3, A2B4, A3B2, A4B1 | 1 | 1 | 1 | 0 | 1 | 1 |
| A1B4, A2B1, A3B2, A4B3 | 1 | 0 | 0 | 1 | 1 | 0 |
| A1B4, A2B1, A3B3, A4B2 | 1 | 0 | 0 | 0 | 1 | 0 |
| A1B4, A2B2, A3B1, A4B3 | 1 | 0 | 1 | 1 | 1 | 0 |
| A1B4, A2B2, A3B3, A4B1 | 1 | 0 | 1 | 0 | 1 | 0 |
| A1B4, A2B3, A3B1, A4B2 | 1 | 1 | 0 | 0 | 1 | 0 |
| A1B4, A2B3, A3B2, A4B1 | 1 | 1 | 0 | 1 | 1 | 0 |

QuickSwitch Functions as a High-Speed Switch

A block diagram of the QS3383 CMOS Bus Exchange Switch is shown in Figure 2. This device consists of two banks of ten switches arranged to gate through or exchange two banks of five signals. This allows the QS3384 to be used as a 10-bit switch or as a 5-bit, two way bus exchange device. This part is particularly useful for exchange and routing operations such as byte swap, crossbar matrices, and RAM sharing.

Each switch consists of an N channel MOS transistor driven by a CMOS gate. When the switch is enabled, the gate of the N channel transistor is at V_{CC} (+5V) and the device is on. These devices have an on resistance of less than 5Ω for voltages near ground and will drive in excess of 64 mA each. The resistance rises somewhat as the I/O voltage rises from a TTL LOW of 0.0V to a TTL HIGH of 2.4V. In this region the A and B pins are solidly connected, and the bus switch is specified in the same manner as a TTL device over this range. As the I/O voltage rises to approximately 4.0V, the transistor turns off. This corresponds to a typical TTL HIGH of 3.5 to 4.0V.

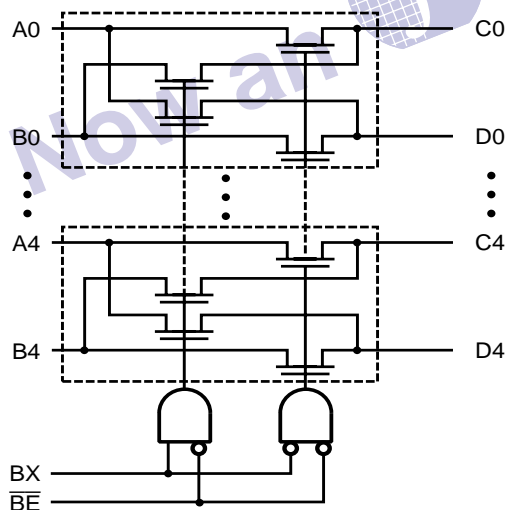


Figure 2. QS3383 CMOS Bus Exchange Switch Block Diagram

QuickSwitch Provides High-Speed Solution

The propagation delay of the QuickSwitch is determined only by the channel resistance and the total load capacitance on the channel. The on resistance of the channel is approximately 5Ω and the capacitance due to the QuickSwitch is a maximum of 10pF. This gives the QuickSwitch a very low propagation delay. The 250ps maximum propagation delay specified for the QS3383 and QS3384 assume a total load of 50pF which means that if the system has less than 40pF of capacitance on the QuickSwitch, the actual propagation delay will be even lower. Some high-speed data transmission applications require data rates as high as 1GBits/S which requires devices with propagation delays of 1ns or less which is easily within the QuickSwitch's capabilities. The QuickSwitch can pass signals with little or no attenuation at data rates as high as 3GBits/S as shown in Figure 3.

Table 1. Pin Description

| Name | I/O | Function |
|-----------------|-----|-------------------|
| A4-A0, B4-B0 | I/O | Buses A, B |
| C4-C0, D4-D0 | I/O | Buses C, D |
| \overline{BE} | I | Bus Switch Enable |
| BX | I | Bus Exchange |

Table 2. Function Table

| \overline{BE} | BX | A4-A0 | B4-B0 | Function |
|-----------------|----|-------|-------|------------|
| H | X | Hi-Z | Hi-Z | Disconnect |
| L | L | C4-C0 | D4-D0 | Connect |
| L | H | D4-D0 | C4-C0 | Exchange |

It is possible for the QuickSwitch to attain this high-performance because it is passing signals, not driving them. The QuickSwitch acts as a solid state relay with a 6.5ns turn-on time and a 5.5ns turn-off time. Because the QuickSwitch has no drive capability, no noise is introduced into the system. The 5Ω channel resistance actually helps reduce some of the system noise that is present. Figure 3 shows a high-speed waveform passed through the QuickSwitch. No crosstalk or groundbounce is present.

QuickSwitch is Expandable for Wide Applications

The QSQS3383 QuickSwitch is configured to connect/exchange two 5-bit buses as shown in Figure 4. For wider buses, multiple QuickSwitches are necessary. Two QuickSwitches are used to get a 10-bit bus, three QuickSwitches for a 15-bit bus, etc. For any level of parallel expansion, the control pins for each block of QuickSwitches are tied together. For a 4 x 4 x 32 bit crossbar switch, seven QuickSwitches in parallel would provide 35 available bits and when the seven \overline{BE} pins are tied together and the seven BX pins are tied together, the seven QuickSwitches act as a single device with only two control pins as shown below.

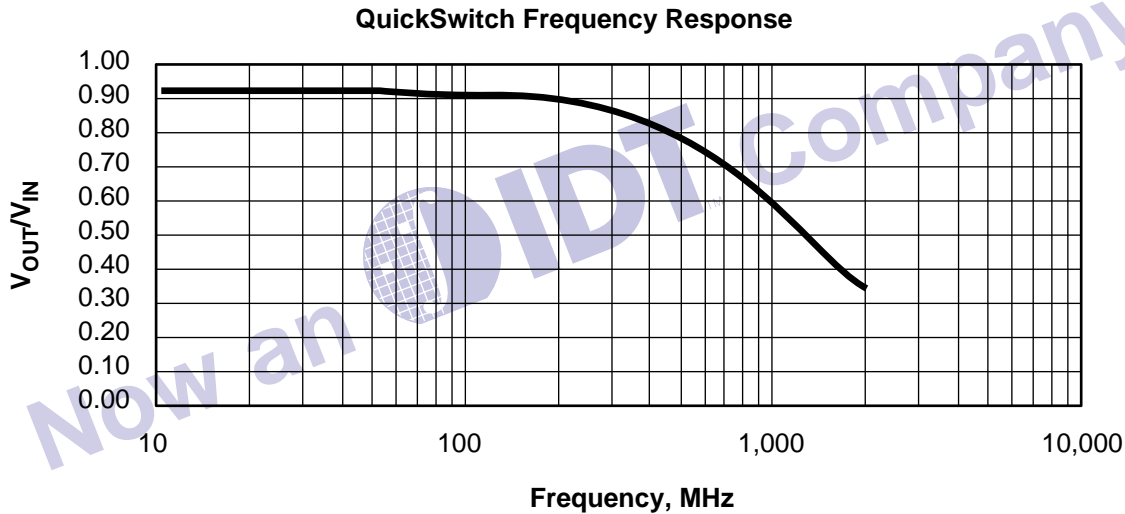


Figure 3. QuickSwitch Attenuation vs. Frequency

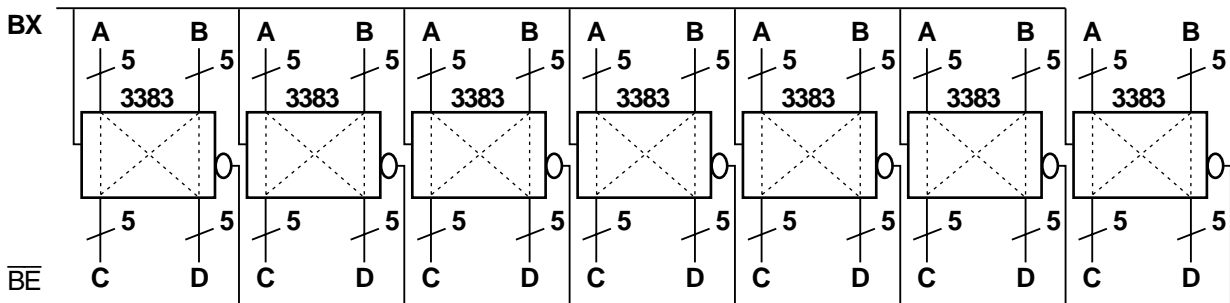


Figure 4. 35 Bit Width Expansion of QuickSwitch

Conclusion

A 4 x 4 x 32 bit crossbar switch on a single chip would require close to 300 pins. With the QuickSwitch, 42 QS3383's would be required (2x3 matrix X 7 QuickSwitches for 35 bits). However, with QSI's low cost high-performance CMOS technology, 42 QuickSwitches would not only be competitively priced but in many cases, substantially less expensive than a single chip solution.

The QSI developed, industry standard Quarter Size Outline Package (QSOP) provides a very compact solution to board space problems and gives

additional benefits as a high-performance package. Using the QuickSwitch in a 24-pin QSOP has several advantages over a single chip crossbar switch solution. In addition to the small space required, the QSOP solution offers the flexibility of moving individual QuickSwitch devices to improve board layout efficiency. The QSOP's can be mounted on modules to further reduce board space requirements. The maximum frequency of the QSOP package is also substantially higher than a large package such as QFP or PGA.

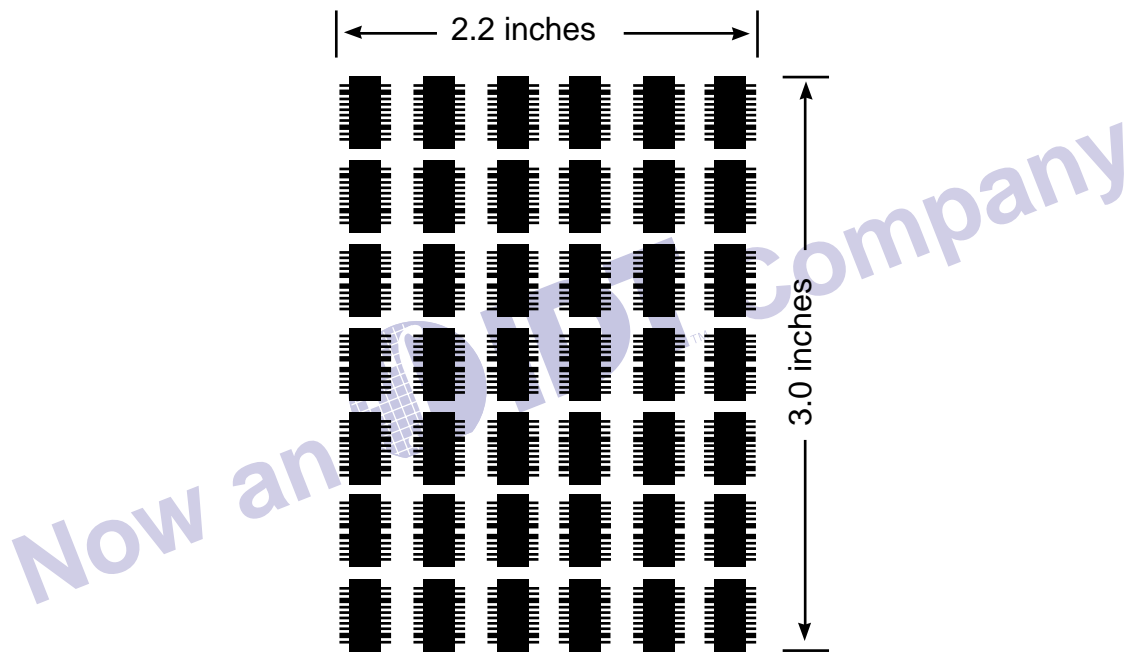


Figure 4. 4 x 4 x 32-Bit Crossbar Using QuickSwitch in QSOP Package
(Actual Size)