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Renesas Electronics Corporation

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H8/300L SLP Series

1/4-Duty-Cycle Driving of the LCD

Introduction

A five-digit number is displayed on an LCD panel using the segment-type LCD control circuit, LCD driver, and power supply circuit of the H8/38024 Series.

Target Device

H8/38024

Contents

1. Specifications

1. A five-digit number is displayed on an LCD panel using the segment-type LCD control circuit, LCD driver, and power supply circuit of the H8/38024 Series.
2. 1/4-duty-cycle driving of LCD is implemented using four common signals and 12 segment signals.
3. An example of LCD module connection and LCD display for this sample task is shown in figure 1.1.

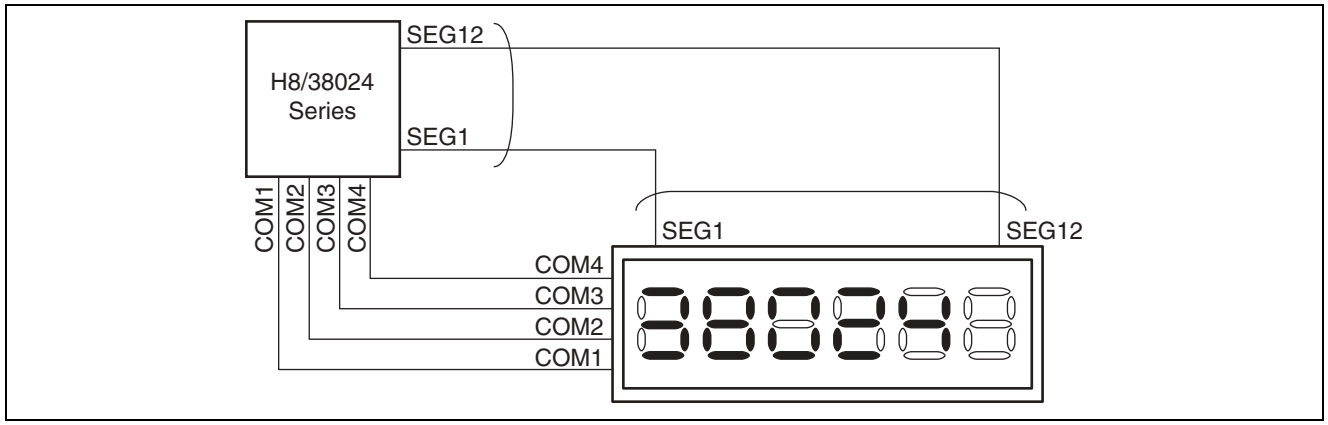


Figure 1.1 Example of LCD Display

2. Description of Functions

1. In this sample task, the LCD controller/driver is used for LCD display. The features of the LCD controller/driver are described below.
   - Display capacity
     A. Duty cycle: Static
        Internal driver: 32 segments
     B. Duty cycle: 1/2
        Internal driver: 32 segments
     C. Duty cycle: 1/3
        Internal driver: 32 segments
     D. Duty cycle: 1/4
        Internal driver: 32 segments
   - LCD RAM capacity: 16 bytes
   - LCD RAM is word-accessible.
   - Every unit of four segment output pins can be used individually as port pins.
   - The common output pins not used because of the specified duty cycle can be used for common double-buffering (parallel connection).
   - Display is possible in all operating modes other than standby mode.
   - Frame frequency can be selected from among 11 values.
   - A power supply split-resistance is built-in for supply of LCD drive power.
   - When not used, this LCD module alone can be placed in a standby state by the module standby mode.
   - A or B waveform can be selected by software.

2. Figure 2.1 is a block diagram of the LCD controller/driver used in this sample task.

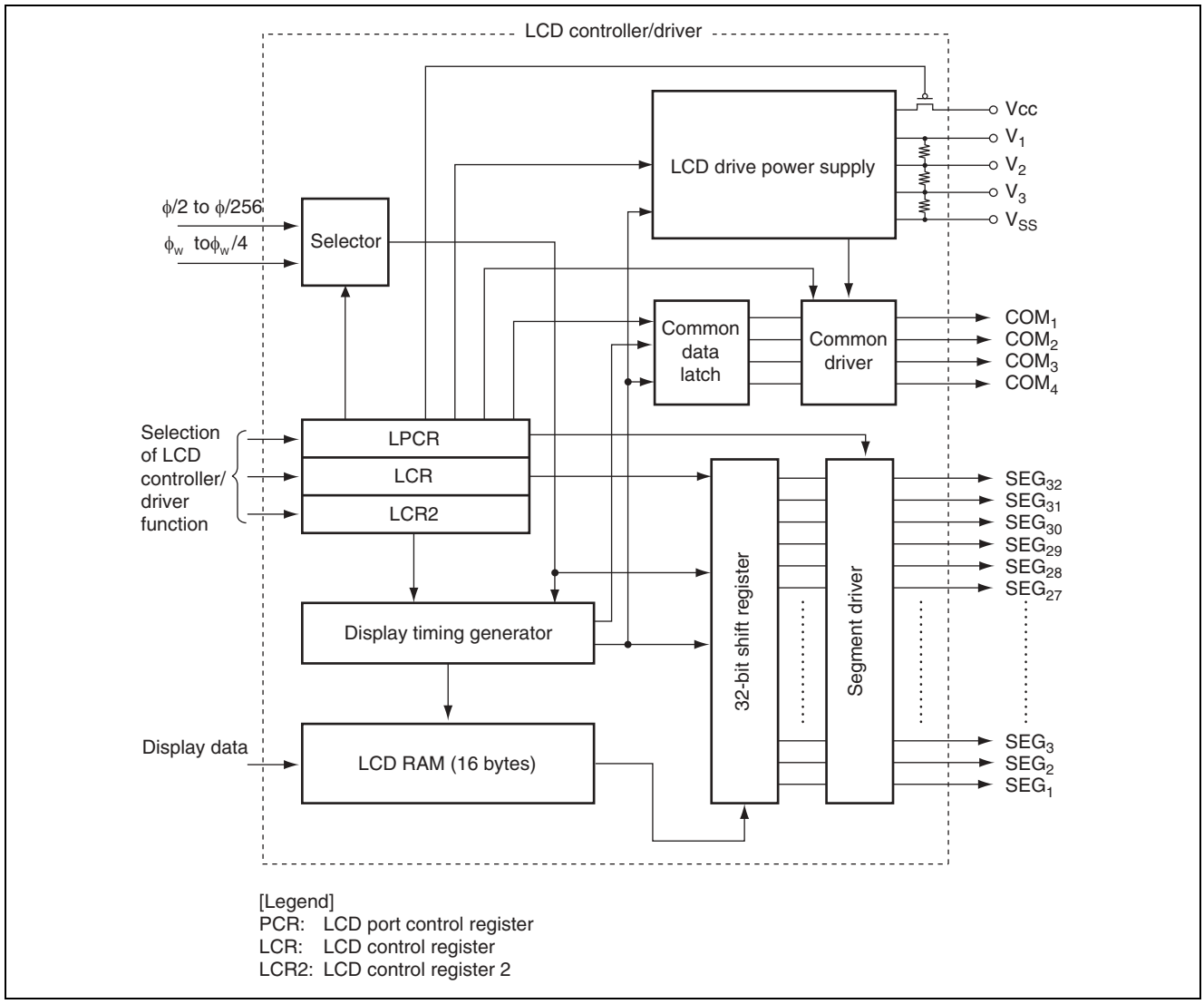


Figure 2.1 Block Diagram of LCD Controller/Driver

3. Functions of the LCD controller/driver are explained in table 2.1.

Table 2.1 LCD Controller/Driver Functions

Register/Pin	Function
LCD port control register (LPCR)	LPCR is an 8-bit readable/writable register which selects the duty cycle, the LCD driver, and pin functions. LPCR is initialized to H'00 upon a reset.
LCD control register (LCR)	LCR is an 8-bit readable/writable register which turns on and off the LCD drive power supply, controls display data, and selects the frame frequency. LCR is initialized to H'80 upon a reset.
LCD control register 2 (LCR2)	LCR2 is an 8-bit readable/writable register which controls switching between A and B waveforms. LCR2 is initialized to H'60 upon a reset.
Segment output pins (SEG_{32} to SEG_1)	These are pins used for driving LCD segments; all these pins are multiplexed as port pins (setting is programmable).
Common output pins (COM_4 to COM_1)	These are LCD common driving output pins; under static or 1/2-duty cycle driving, they can be used in parallel.
LCD power supply pins (V_1, V_2, V_3)	These pins are used when connecting an external bypass capacitor or when using an external power supply circuit.
LCD RAM	Display data is placed here. The relation between the LCD RAM and the display segments differs according to the duty cycle setting. Display is started in this way: after the registers necessary for display have been set, write data in the locations corresponding to the given duty cycle using the same instructions as those for writing to ordinary RAM, and then turn the display on. Word/byte access instructions can be used to set data in the LCD RAM.

4. In this sample task, a 6-digit 7-segment LCD is driven by 1/4-duty-cycle driving. Figure 2.2 is a diagram showing connections for segment signals and common signals for the 6-digit 7-segment LCD used in this sample task.

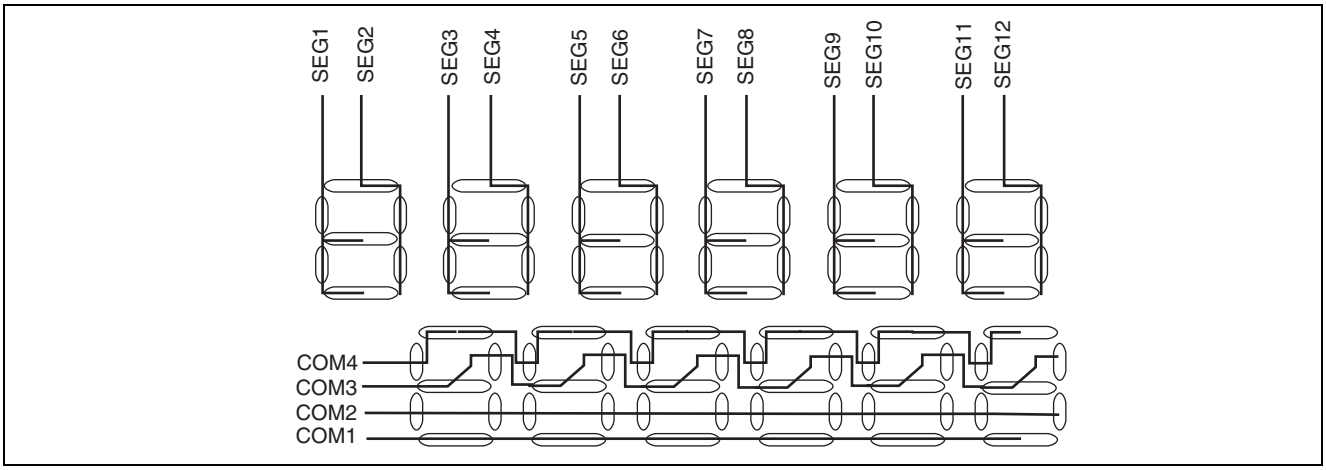


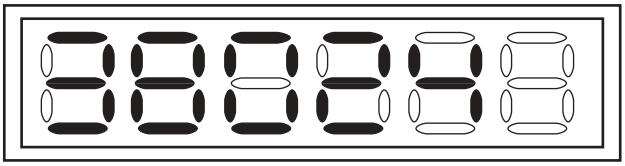
Figure 2.2 Connections of Segment Signals and Common Signals for the 6-Digit 7-Segment LCD Used in this Sample task

5. Figure 2.3 shows the LCD RAM mapping under 1/4-duty-cycle driving.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
H'F740	SEG_2	SEG_2	SEG_2	SEG_2	SEG_1	SEG_1	SEG_1	SEG_1
H'F741	SEG_4	SEG_4	SEG_4	SEG_4	SEG_3	SEG_3	SEG_3	SEG_3
H'F742	SEG_6	SEG_6	SEG_6	SEG_6	SEG_5	SEG_5	SEG_5	SEG_5
H'F743	SEG_8	SEG_8	SEG_8	SEG_8	SEG_7	SEG_7	SEG_7	SEG_7
H'F744	SEG_{10}	SEG_{10}	SEG_{10}	SEG_{10}	SEG_9	SEG_9	SEG_9	SEG_9
H'F745	SEG_{12}	SEG_{12}	SEG_{12}	SEG_{12}	SEG_{11}	SEG_{11}	SEG_{11}	SEG_{11}
H'F746	SEG_{14}	SEG_{14}	SEG_{14}	SEG_{14}	SEG_{13}	SEG_{13}	SEG_{13}	SEG_{13}
H'F747	SEG_{16}	SEG_{16}	SEG_{16}	SEG_{16}	SEG_{15}	SEG_{15}	SEG_{15}	SEG_{15}
H'F748	SEG_{18}	SEG_{18}	SEG_{18}	SEG_{18}	SEG_{17}	SEG_{17}	SEG_{17}	SEG_{17}
H'F749	SEG_{20}	SEG_{20}	SEG_{20}	SEG_{20}	SEG_{19}	SEG_{19}	SEG_{19}	SEG_{19}
H'F74A	SEG_{22}	SEG_{22}	SEG_{22}	SEG_{22}	SEG_{21}	SEG_{21}	SEG_{21}	SEG_{21}
H'F74B	SEG_{24}	SEG_{24}	SEG_{24}	SEG_{24}	SEG_{23}	SEG_{23}	SEG_{23}	SEG_{23}
H'F74C	SEG_{26}	SEG_{26}	SEG_{26}	SEG_{26}	SEG_{25}	SEG_{25}	SEG_{25}	SEG_{25}
H'F74D	SEG_{28}	SEG_{28}	SEG_{28}	SEG_{28}	SEG_{27}	SEG_{27}	SEG_{27}	SEG_{27}
H'F74E	SEG_{30}	SEG_{30}	SEG_{30}	SEG_{30}	SEG_{29}	SEG_{29}	SEG_{29}	SEG_{29}
H'F74F	SEG_{32}	SEG_{32}	SEG_{32}	SEG_{32}	SEG_{31}	SEG_{31}	SEG_{31}	SEG_{31}
	↓	↓	↓	↓	↓	↓	↓	↓
	COM_4	COM_3	COM_2	COM_1	COM_4	COM_3	COM_2	COM_1

Figure 2.3 LCD RAM Mapping under 1/4-Duty-Cycle Driving

6. Figure 2.4 shows the relation between the display on the 6-digit 7-segment LCD used in this sample task and data set in the LCD RAM. The numeric characters "38024" is displayed on the 6-digit 7-segment LCD by setting the LCD RAM as shown in figure 2.4.



	Bit 7	Bit 6	Bit 5	Bit 4*1	Bit 3	Bit 2	Bit 1	Bit 0	
H'F740	1	1	1	0	0	1	0	1	Display data for "3"
H'F741	1	1	1	0	1	1	1	1	Display data for "8"
H'F742	1	1	1	0	1	0	1	1	Display data for "0"
H'F743	1	1	0	0	0	1	1	1	Display data for "2"
H'F744	0	1	1	0	1	1	0	0	Display data for "4"
H'F745	0	0	0	0	0	0	0	0	Display data for " " *2
H'F746	0	0	0	0	0	0	0	0	
H'F747	0	0	0	0	0	0	0	0	
H'F748	0	0	0	0	0	0	0	0	
H'F749	0	0	0	0	0	0	0	0	
H'F74A	0	0	0	0	0	0	0	0	
H'F74B	0	0	0	0	0	0	0	0	
H'F74C	0	0	0	0	0	0	0	0	
H'F74D	0	0	0	0	0	0	0	0	
H'F74E	0	0	0	0	0	0	0	0	
H'F74F	0	0	0	0	0	0	0	0	

Note: 1. Bit 4 is not used and is always set to 0.
2. " "denotes a blank.

Figure 2.4 Relation between LCD Display and LCD RAM Settings

7. Figure 2.5 shows the relationship between SEG_1 and SEG_2 display on the 6-digit 7-segment LCD and the corresponding LCD RAM bits. As shown in figure 2.5, when the LCD RAM bits for segments 0 to 7 are set to 1, the corresponding segments are lit; when cleared to 0, the corresponding segments are unlit.

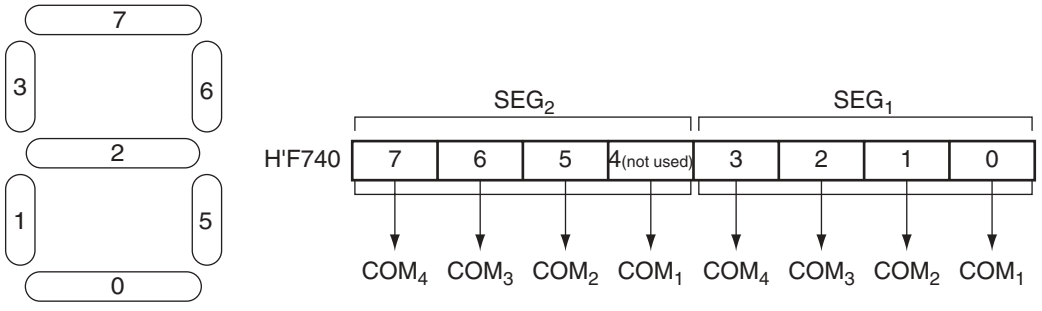


Figure 2.5 Relationship between LCD Lit/Unlit States and LCD RAM Settings

8. Table 2.2 shows examples of display data for display by SEG_1 and SEG_2 on the 6-digit 7-segment LCD.

Table 2.2 Display Data Examples

Symbol	Display	Address	Display Data							
		H'F740	0	0	0	0	0	0	0	0
–		H'F740	0	0	0	0	0	1	0	0
0		H'F740	1	1	1	0	1	0	1	1
1		H'F740	0	1	1	0	0	0	0	0
2		H'F740	1	1	0	0	0	1	1	1
3		H'F740	1	1	1	0	0	1	0	1
4		H'F740	0	1	1	0	1	1	0	0
5		H'F740	1	0	1	0	1	1	0	1
6		H'F740	1	0	1	0	1	1	1	1
7		H'F740	1	1	1	0	1	0	0	0
8		H'F740	1	1	1	0	1	1	1	1
9		H'F740	1	1	1	0	1	1	0	1
A		H'F740	1	1	1	0	1	1	1	0
B		H'F740	0	0	1	0	1	1	1	1
C		H'F740	1	0	0	0	1	0	1	1
D		H'F740	0	1	1	0	0	1	1	1
E		H'F740	1	0	0	0	1	1	1	1
F		H'F740	1	0	0	0	1	1	1	0

9. Table 2.3 shows assignment of functions in this sample task.

Table 2.3 Function Assignment

Function	Assignment
LPCR	Selects duty cycle, LCD driver, and pin functions.
LCR	Turns LCD drive power supply on and off, controls display data, and selects frame frequency.
LCR2	Switches between A and B waveforms.
SEG_{12} to SEG_1	Used as segment driver pins.
COM_4 to COM_1	Used as a common driver pin.
LCD RAM	Sets the LCD display data.

3. Description of Operation

1. Software settings for LCD display are described below.
   A. Duty cycle selection
      By setting DTS1 and DTS0, duty cycle can be selected from among "static", 1/2, 1/3, and 1/4.
   B. Segment driver selection
      SGS3 to SGS0 are used to select the segment drivers to be used.
   C. Frame frequency selection
      By setting CKS3 to CKS0, the frame frequency can be selected. The frame frequency should be selected according to the LCD panel specifications.
   D. Selection of A or B waveforms
      LCDAB can be used to select either the A or the B waveform for use as the LCD waveform.

2. Figure 3.1 shows the waveforms of segment drive signals, which illustrate the operation of this sample task.

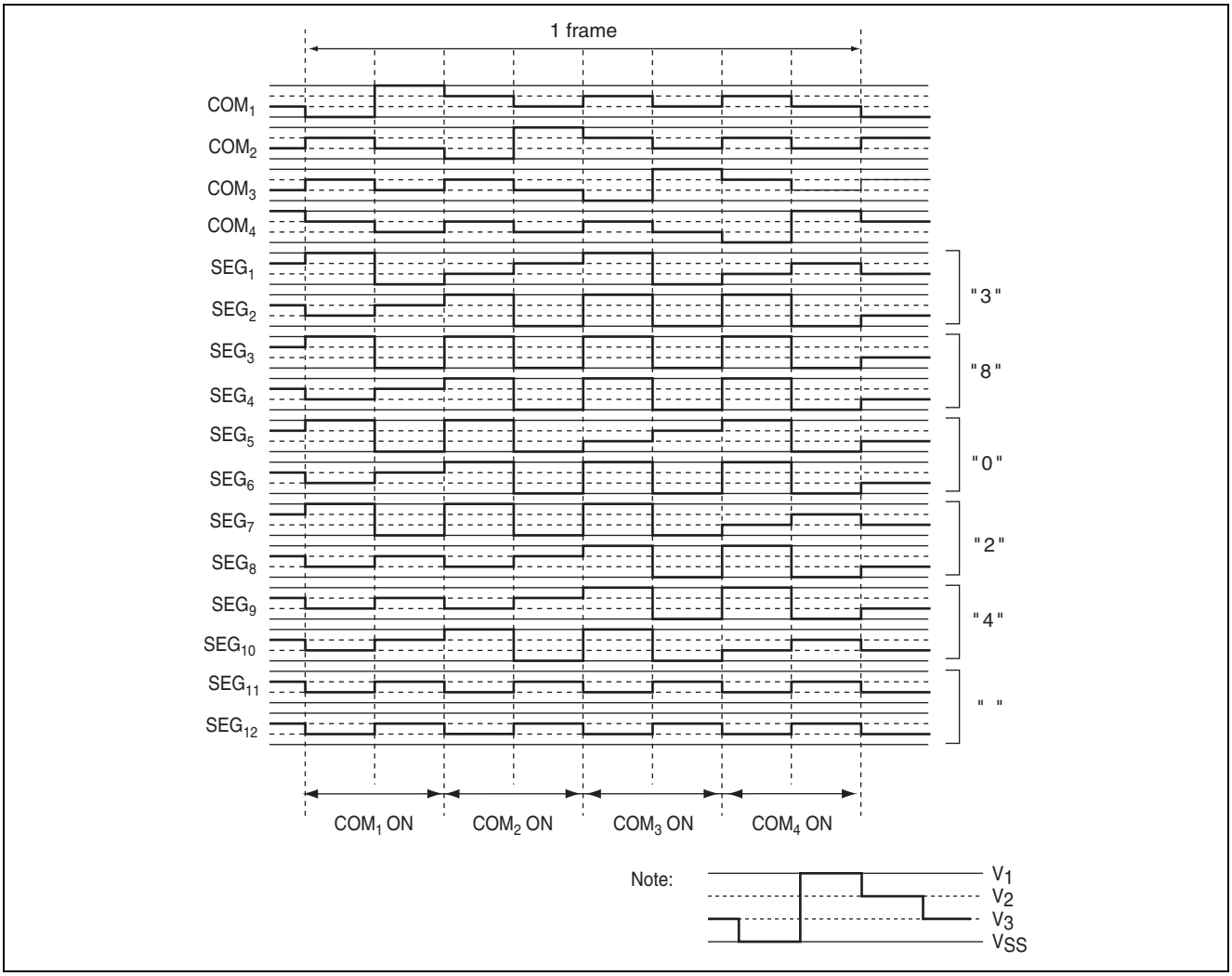


Figure 3.1 Waveforms of Segment Drive Signals

4. Description of Software

4.1 Module

Table 4.1 shows the module in this sample task.

Table 4.1 Description of Module

Module	Label	Function
Main routine	Main	Initializes LCD RAM and LCD controller/driver and enables interrupts.

4.2 Arguments

In this sample task, no arguments are used.

4.3 Internal Registers

Table 4.2 shows the internal registers used in this sample task.

Table 4.2 Description of Internal Registers

Register		Function	Address	Setting
LPCR	DTS1, DTS0	LCD Port Control Register (Duty Cycle Selection 1, 0) Selects a duty cycle from among "static", 1/2, 1/3, and 1/4 by the settings of DTS1 and DTS0 in combination. When DTS1 = 0 and DTS0 = 0, static drive is selected. When DTS1 = 0 and DTS0 = 1, 1/2 duty cycle is selected. When DTS1 = 1 and DTS0 = 0, 1/3 duty cycle is selected. When DTS1 = 1 and DTS0 = 1, 1/4 duty cycle is selected.	H'FFC0 Bit 7 Bit 6	DTS1 = 1 DTS0 = 1
LPCR	CMX	LCD Port Control Register (Common Function Selection) Selects whether the same waveform is output from several pins in order to increase the common driving capacity when common pins are not used with the given duty cycle. If CMX = 0, the same waveform is not output from multiple common pins not used with that duty cycle. If CMX = 1, the same waveform is output from multiple common pins not used with that duty cycle.	H'FFC0 Bit 5	0

Register		Function	Address	Setting
LPCR	SGS3 SGS2 SGS1 SGS0	LCD Port Control Register (Segment Driver Selection) Selects the segment driver to be used. When SGX = 0, SGS3 = 0, SGS2 = 0, SGS1 = 0 and SGS0 = 0, pins SEG_{32} to SEG_1 function as ports. When SGX = 0, SGS3 = 0, SGS2 = 0, SGS1 = 0 and SGS0 = 1, pins SEG_{32} to SEG_1 function as ports. When SGX = 0, SGS3 = 0, SGS2 = 0, SGS1 = 1 and SGS0 = *, pins SEG_{32} to SEG_{25} function as segment drivers and pins SEG_{24} to SEG_1 function as ports. When SGX = 0, SGS3 = 0, SGS2 = 1, SGS1 = 0 and SGS0 = *, pins SEG_{32} to SEG_{17} function as segment drivers and pins SEG_{16} to SEG_1 function as ports. When SGX = 0, SGS3 = 0, SGS2 = 1, SGS1 = 1 and SGS0 = *, pins SEG_{32} to SEG_9 function as segment drivers and pins SEG_8 to SEG_1 function as ports. When SGX = 0, SGS3 = 1, SGS2 = *, SGS1 = * and SGS0 = *, pins SEG_{32} to SEG_1 function as segment drivers. Note: * Don't care	H'FFC0 Bit 3 Bit 2 Bit 1 Bit 0	SGS3 = 1 SGS2 = 0 SGS1 = 0 SGS0 = 0
LCR	PSW	LCD Control Register (LCD Drive Power Supply On/Off Control) The LCD drive power supply can be turned off using this bit when LCD display is not used in power-down mode or when an external power supply is used. However, when the ACT bit is cleared to 0 or when in standby mode, the LCD drive power supply is always turned off regardless of setting of this bit. If PSW = 0, the LCD drive power supply is turned off. If PSW = 1, the LCD drive power supply is turned on.	H'FFC1 Bit 6	1
	ACT	LCD Control Register (Display Function Activate) Selects whether the LCD controller/driver is to be used or not. By clearing this bit to 0, LCD controller/driver operation is halted. In addition, regardless of the value of PSW, the LCD drive power supply is turned off. However, the register contents are retained. If ACT = 0, LCD controller/driver operation is halted. If ACT = 1, LCD controller/driver operates.	H'FFC1 Bit 5	1

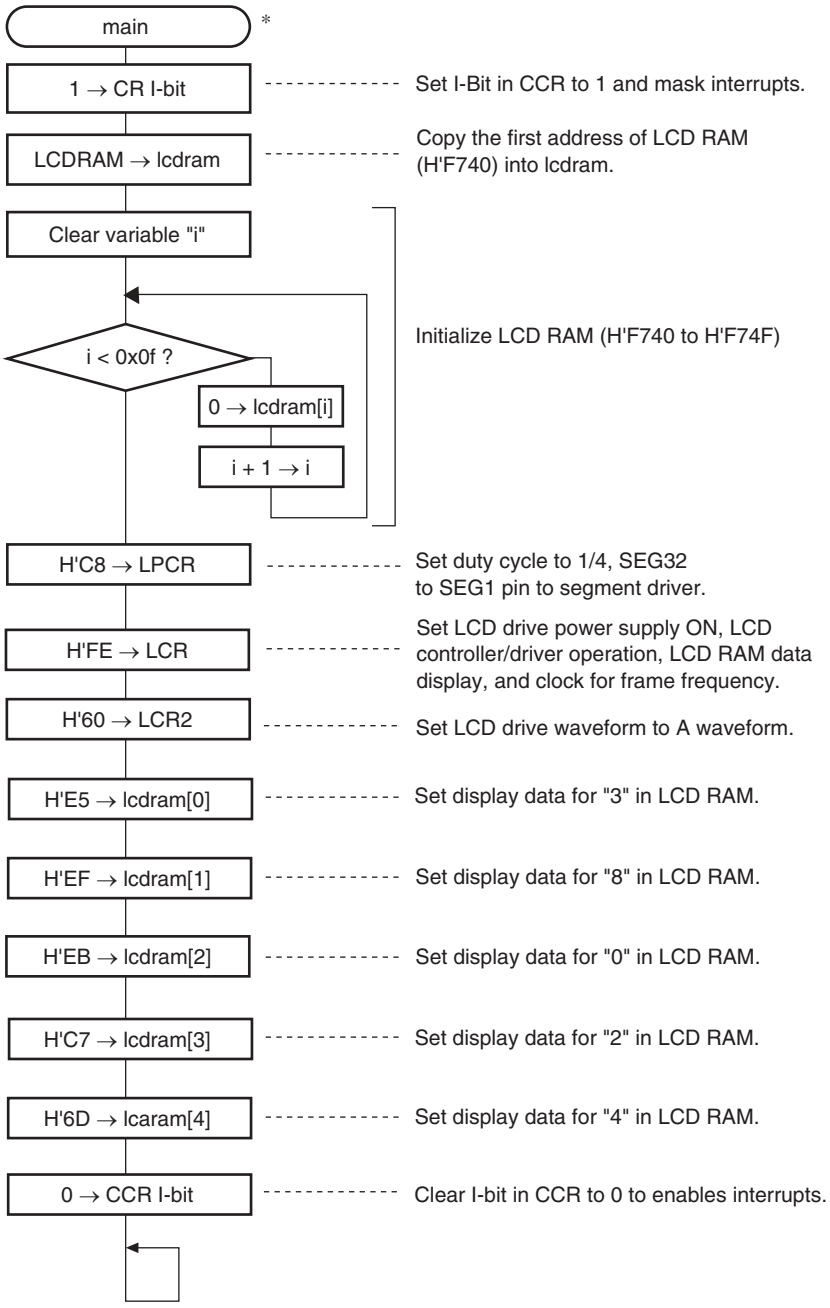
Register		Function	Address	Setting
LCR	DISP	LCD Control Register (Display Data Control) DISP selects whether to display data in LCD RAM or display blank regardless of LCD RAM contents. If DISP = 0, blank is displayed If DISP = 1, LCD RAM data is displayed	H'FFC1 Bit 4	1
	CKS3 CKS2 CKS1 CKS0	LCD Control Register (Frame Frequency Select 3 to 0) Selects a clock to obtain a desired frame frequency. When CKS3 = 0, CKS2 = *, CKS1 = 0 and CKS0 = 0, ϕ_w is selected as operating clock When CKS3 = 0, CKS2 = *, CKS1 = 0 and CKS0 = 1, $\phi_w/2$ is selected as operating clock When CKS3 = 0, CKS2 = *, CKS1 = 1 and CKS0 = *, $\phi_w/4$ is selected as operating clock When CKS3 = 1, CKS2 = 0, CKS1 = 0 and CKS0 = 0, $\phi/2$ is selected as operating clock When CKS3 = 1, CKS2 = 0, CKS1 = 0 and CKS0 = 1, $\phi/4$ is selected as operating clock When CKS3 = 1, CKS2 = 0, CKS1 = 1 and CKS0 = 0, $\phi/8$ is selected as operating clock When CKS3 = 1, CKS2 = 0, CKS1 = 1 and CKS0 = 1, $\phi/16$ is selected as operating clock When CKS3 = 1, CKS2 = 1, CKS1 = 0 and CKS0 = 0, $\phi/32$ is selected as operating clock When CKS3 = 1, CKS2 = 1, CKS1 = 0 and CKS0 = 1, $\phi/64$ is selected as operating clock When CKS3 = 1, CKS2 = 1, CKS1 = 1 and CKS0 = 0, $\phi/128$ is selected as operating clock When CKS3 = 1, CKS2 = 1, CKS1 = 1 and CKS0 = 1, $\phi/256$ is selected as operating clock Note: * Don't care	H'FFC1 Bit 3 Bit 2 Bit 1 Bit 0	CKS3 = 1 CKS2 = 1 CKS1 = 1 CKS0 = 0
LCR2	LCDAB	LCD Control Register 2 (A Waveform/B Waveform Switching Control) Selects whether the A or B waveform is to be used as the LCD drive waveform. If LCDAB = 0, the LCD is driven using the A waveform If LCDAB = 1, the LCD is driven using the B waveform	H'FFC2 Bit 7	0

4.4 Description of RAM

In this sample task, RAM is not used.

5. Flowchart

1. Main routine



Note: * In this sample task, the stack pointer is set in INIT.SRC (assembly language).

6. Program Listing

INIT.SRC (Program listing)

```
    .EXPORT   _INIT
    .IMPORT   _main
;
    .SECTION  P,CODE
_INIT:
    MOV.W     #H'FF80,R7
    LDC.B     #B'10000000,CCR
    JMP       @_main
;
    .END
```

```
/************************************************************************************************************************/
/*                                                                                                                      */
/*     H8/300L Super Low Power Series                                                                                   */
/*     -H8/38024 Series-                                                                                                */
/*     Application Note                                                                                                 */
/*                                                                                                                      */
/*     'Liquid Crystal Display                                                                                          */
/*      -1/4 Duty Drive, Internal Driver-'                                                                              */
/*                                                                                                                      */
/*     Function: LCD Controller / Driver                                                                                */
/*                                                                                                                      */
/*     External Clock : 10MHz                                                                                           */
/*     Internal Clock : 5MHz                                                                                            */
/*     Sub Clock      : 32.768kHz                                                                                       */
/*                                                                                                                      */
/************************************************************************************************************************/

#include    <machine.h>

/************************************************************************************************************************/
/*  Symbol Definition                                                                                                   */
/************************************************************************************************************************/
struct BIT {
    unsigned char   b7:1;       /* bit7 */
    unsigned char   b6:1;       /* bit6 */
    unsigned char   b5:1;       /* bit5 */
    unsigned char   b4:1;       /* bit4 */
    unsigned char   b3:1;       /* bit3 */
    unsigned char   b2:1;       /* bit2 */
    unsigned char   b1:1;       /* bit1 */
    unsigned char   b0:1;       /* bit0 */
};

#define     LPCR        *(volatile unsigned char *)0xFFC0       /* LCD Port Control Register               */
#define     LCR         *(volatile unsigned char *)0xFFC1       /* LCD Control Register                    */
#define     LCR2        *(volatile unsigned char *)0xFFC2       /* LCD Control Register 2                  */
#define     LCDRAM      (volatile unsigned char *)0xF740        /* LCD RAM                                 */
```

```
/************************************************************************************************************************/
/*  Function define                                                                                                     */
/************************************************************************************************************************/
extern void INIT ( void );                                      /* SP Set                                               */
void        main ( void );

/************************************************************************************************************************/
/*  Vector Address                                                                                                      */
/************************************************************************************************************************/
#pragma section     V1                                          /* Vector Section Set                                   */
void (*const VEC_TBL1[])(void) = {
    INIT                                                        /* 0x0000 Reset Vector                                  */
};

#pragma section                                                 /* P                                                    */
/************************************************************************************************************************/
/*  Main Program                                                                                                        */
/************************************************************************************************************************/
void    main ( void )
{
    int i;
    unsigned char *lcdram;

    set_imask_ccr(1);                                           /* Interrupt Disable                                    */

    lcdram = LCDRAM;
    for ( i = 0; i < 0x0F; i++ ){
        lcdram[i] = 0;
    }

    LPCR = 0xC8;                                                /* 1/4 Duty ,Select SEG32-SEG1                          */
    LCR  = 0xFE;                                                /* LCD ON                                               */
    LCR2 = 0x60;

    lcdram[0] = 0xe5;     /* "3" */
    lcdram[1] = 0xef;     /* "8" */
    lcdram[2] = 0xeb;     /* "0" */
    lcdram[3] = 0xc7;     /* "2" */
    lcdram[4] = 0x6c;     /* "4" */

    set_imask_ccr(0);                                           /* Interrupt Enable                                     */

    while (1) {
        ;
    }
}
```

Link address specifications

Section Name	Address
CV1	H'0000
P	H'0100

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Dec.19.03	—	First edition issued

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