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SH7211 Group

12-Bit A/D Converter:

Example of Settings for Conversion in Continuous Scan Mode

Introduction

This application note describes an example of settings for the 12-bit A/D converter in continuous scan mode as a sample application for the A/D converter of the SH7211.

Target Device

SH7211

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1. Preface

1.1 Specifications

- A/D conversion in continuous scan mode by the 12-bit A/D converter
- Three rounds of A/D conversion are performed on analog input channels 0 to 3 (AN0 to AN3), and the converted data are stored in RAM.

1.2 Module Used

- 12-bit A/D converter (12-bit A/D)

1.3 Applicable Conditions

- MCU SH7211 (R5F7211)
- Clock operating mode 6
- Operating frequency Internal clock: 160 MHz
Bus clock: 40 MHz
Peripheral clock: 40 MHz
- C compiler SuperH RISC Engine Family C/C++ Compiler Package Ver.9.0.3.0
from Renesas Technology
- Compiler options Default settings of the High-performance Embedded Workshop
(-cpu = sh2a -debug -gbr = auto -global_volatile = 0 -opt_range = all
-infinite_loop = 0 -del_vacant_loop = 0 -struct_alloc = 1)

1.4 Related Application Note

None

2. Description of the Sample Application

The sample program employs the continuous scan mode of the 12-bit A/D converter to perform three rounds of A/D conversion on input channels 0 to 3 (AN0 to AN3), and then stores converted data in RAM.

2.1 Operational Overview of Module Used

The operating modes of the 12-bit A/D converter are single-cycle scan mode and continuous scan mode. In single-cycle scan mode, A/D conversion is performed once on each of one or more specified channels and then ends. The ADST bit is automatically cleared to 0. In continuous scan mode, A/D conversion is performed sequentially on one or more specified channels until the ADST bit is cleared to 0 by software.

A/D conversion is started by one of the following three methods.

1. Setting the ADST bit by software
2. A/D conversion triggers (TRGAN, TRG0N, TRG4AN, and TRG4BN from MTU2; TRGAN, TRG4AN, and TRG4BN from MTU2S)
3. Input of an external trigger: Falling edge on the $\overline{\text{ADTRG}}$ pin

Additionally, channels 0 to 2 have dedicated sample-and-hold circuits, so multiple channels are capable of simultaneous sampling.

Table 1 gives an overview of the module used in this sample application (i.e. the A/D converter) and figure 1 is a block diagram of the 12-bit A/D converter. For details on the 12-bit A/D converter, see the section on the A/D converter in the *SH7211 Group Hardware Manual* (REJ09B0344).

Table 1 Overview of the Module (A/D Converter) Used in the Sample Application

Item	Description
Resolution	12 bits
Minimum conversion time	1.25 μs per channel
Number of modules	1
Input channels	8
Operating modes	Single-cycle scan mode Continuous scan mode
Sample-and-hold function	Common to 0 to 2 channels: 1 circuit Dedicated for individual channels: 1 circuit each for ch0 to ch2 (3 in all)
Sources for activation of A/D conversion	Software: Setting of the ADST bit Timers: TRGAN, TRG0N, TRG4AN, and TRG4BN signals from the MTU2 module TRGAN, TRG4AN, and TRG4BN signals from the MTU2S module External trigger: $\overline{\text{ADTRG}}$

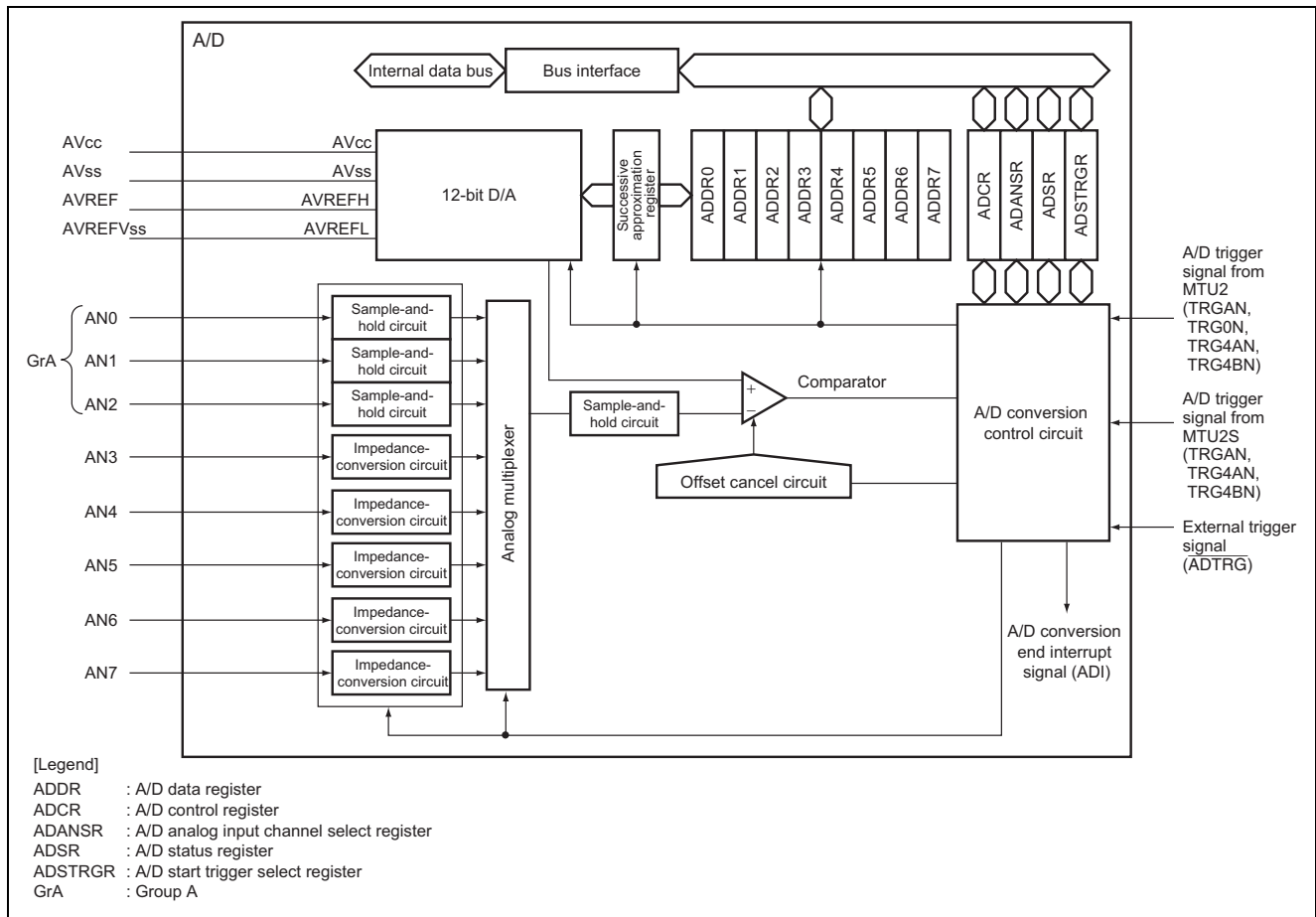


Figure 1 Block Diagram of the 12-Bit A/D Converter

2.2 Procedure for Setting Module Used

Figure 2 shows an example of the initialization sequence for A/D conversion in continuous scan mode. For details on the settings of individual registers, see the *SH7211 Group Hardware Manual (REJ09B0344)*.

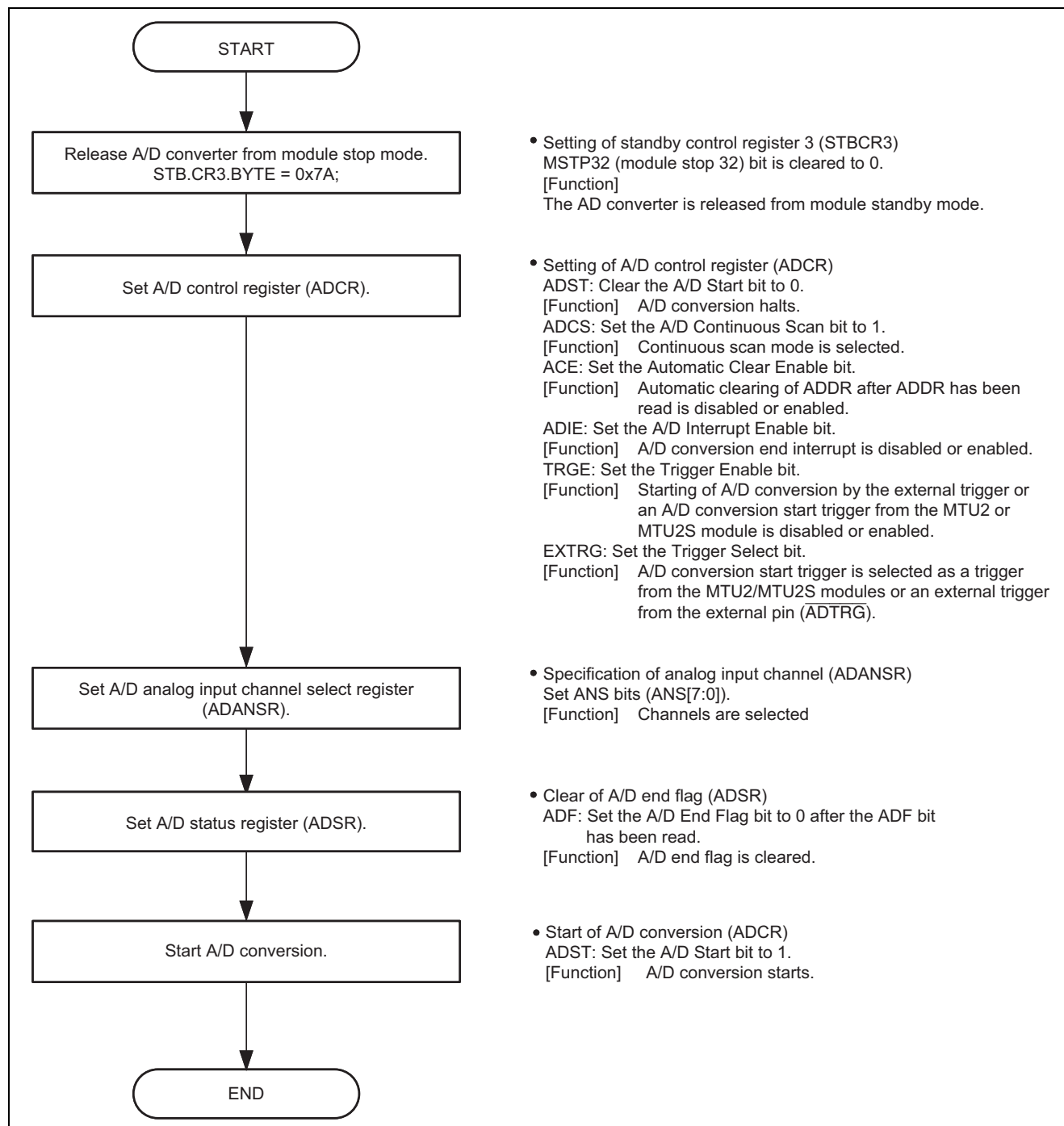


Figure 2 Initialization Sequence for 12-Bit A/D Conversion

2.3 Operation of the Sample Program

In this sample program, A/D conversion in continuous scan mode is performed on channels 0 to 3 (AN0 to AN3). The A/D converter is activated by software and converted data are stored in RAM. This processing is repeated three times.

Table 2 gives a description of RAM usage in this sample program.

Table 2 Variable Used in the Sample Program

Variable Name	Description	Area	Name of Employing Module
Ad_data[AD][CH]	Array for storing A/D-converted data (2 bytes/datum)	On-chip RAM	io_ad_conv (void)

2.4 Sequence of Processing by the Sample Program

Table 3 gives settings for registers used in the sample program and figure 3 shows the flow of handling the sample program.

Table 3 Register Settings Used in Sample Program

Register Name	Address	Setting	Description
A/D control register (ADCR)	H'FFFF E800	H'00	<ul style="list-style-type: none"> ADCS = 1: Continuous scan ACE = 0: Disables automatic clearing of ADDR after reading of ADDR. ADIE = 0: Disables A/D conversion end interrupt. TRGE = 0: Disables starting of A/D conversion by an external trigger or by the MTU2 and MTU2S modules.
A/D analog input channel select register (ADANSR)	H'FFFF E820	H'0F	<ul style="list-style-type: none"> Selects AN0 to AN3.

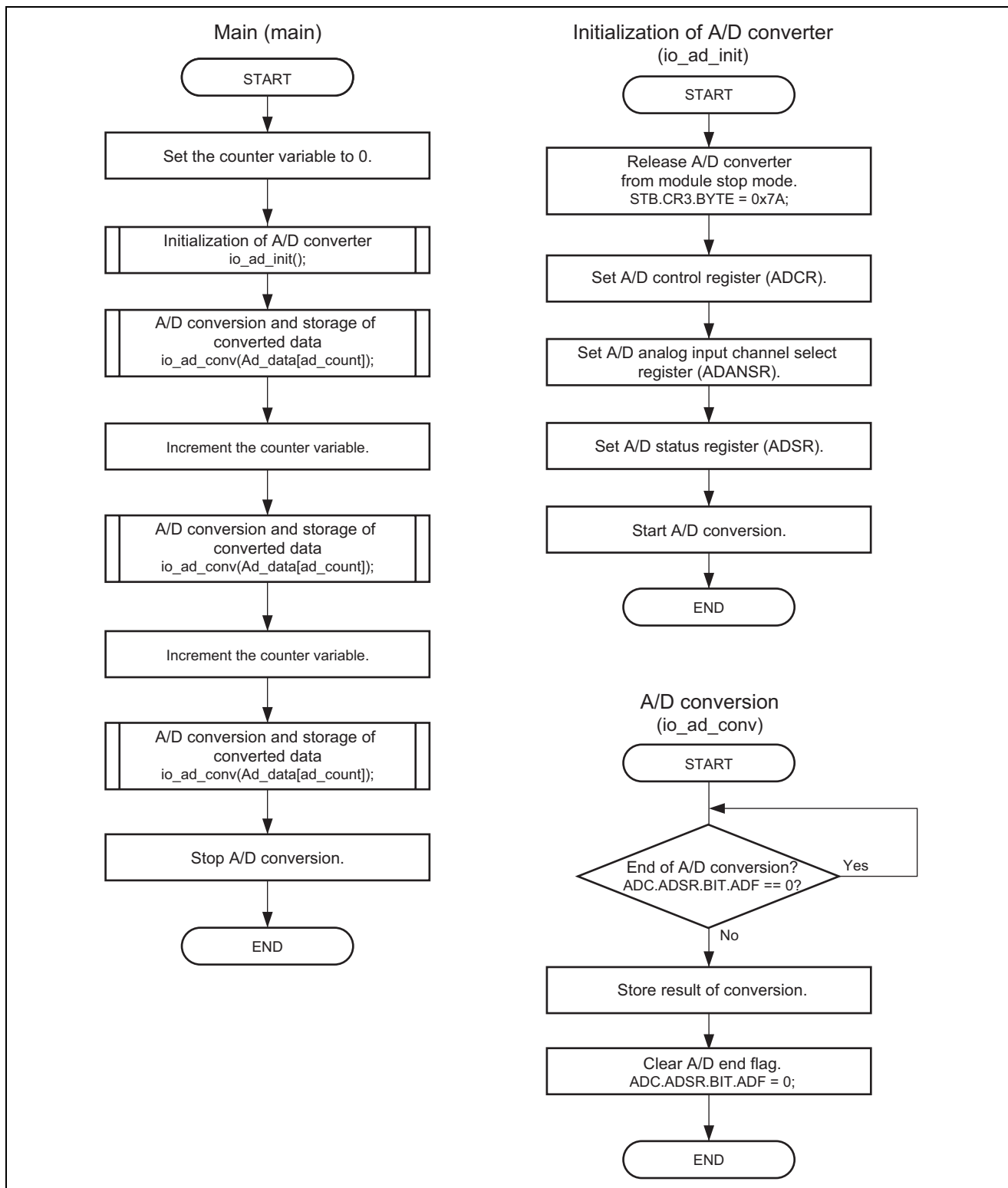


Figure 3 Flow of Handling the Sample Program

3. Listing of Sample Program

1. Sample program listing: "main.c" (1)

```

1      /*"FILE COMMENT"*****
2      *
3      * System Name   : SH7211 Sample Program
4      * File Name    : main.c
5      * Contents     : Sample program for A/D conversion in continuous scan mode
6      * Version      : 1.00.00
7      * Model        : M3A-HS11
8      * CPU          : SH7211
9      * Compiler     : SHC9.0.3.0
10     * note         : A/D conversion in continuous scan mode is performed by the A/D
11     *               converter. Three rounds of A/D conversion on analog input channels
12     *               0 to 3 (AN0 to AN3) proceed, and the converted data are stored in RAM.
13     *
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18     *
19     * Copyright (C) 2007 Renesas Technology Corp. All Rights Reserved
20     * AND Renesas Solutions Corp. All Rights Reserved
21     *
22     * History : 2007.09.04 ver.1.00.00
23     *"FILE COMMENT END"*****/
24     #include <machine.h>
25     #include "iodefine.h"      /* SH7211 iodefine */
26
27
28     /* ==== prototype declaration ==== */
29     void main(void);
30     void io_ad_init(void);
31     void io_ad_conv(unsigned short *ad_buf);
32
33     /* ==== symbol definition ==== */
34     #define AD 3
35     #define CH 4
36
37     /* ==== RAM allocation variable declaration ==== */
38     unsigned short Ad_data[AD][CH];
39     unsigned char ad_count;
40
41

```

2. Sample program listing: "main.c" (2)

```

42  /*"FUNC COMMENT"*****
43  * Outline      : main
44  *-----
45  * Include     : #include "iodefine.h"
46  *             : #include <machine.h>
47  *-----
48  * Declaration : void main(void);
49  *-----
50  * Function    : AD conversion with continuous scan mode
51  *-----
52  * Argument    : none
53  *-----
54  * Return Value : none
55  *-----
56  * Note       : none
57  *"FUNC COMMENT END"*****/
58  void main(void)
59  {
60
61      ad_count = 0;
62
63      /* ==== Initial setting of ADC ==== */
64      io_ad_init();
65
66      /* ==== A/D convert ==== */
67      io_ad_conv(Ad_data[ad_count]);
68      ad_count++;
69      io_ad_conv(Ad_data[ad_count]);
70      ad_count++;
71      io_ad_conv(Ad_data[ad_count]);
72
73      ADC.ADCR.BIT.ADST = 0;      /* A/D conversion stop */
74
75      while(1){
76          /* loop */
77      }
78
79  }
80

```

3. Sample program listing: "main.c" (3)

```

81  /*"FUNC COMMENT"*****
82  * Outline      : Initial setting of ADC
83  *-----
84  * Include      : #include "iodefine.h"
85  *-----
86  * Declaration  : void ad_init(void);
87  *-----
88  * Function     : Initial setting of ADC
89  *-----
90  * Argument     : none
91  *-----
92  * Return Value : none
93  *-----
94  * Note        : none
95  /*"FUNC COMMENT END"*****/
96  void io_ad_init(void)
97  {
98      /* ==== Release of module standby(ADC) ==== */
99      STB.CR3.BYTE = 0x7A;
100
101      /* ==== Setting of ADC ==== */
102      /* ---- A/D Control Register(ADCR) ---- */
103      ADC.ADCR.BYTE = 0x40;
104          /* 7 = b'0      : A/D End Flag                */
105          /* 6 = b'1      : Continuous scan                */
106          /* 5 = b'0      : Automatic clearing of ADDR
107             after being read is disabled                */
108          /* 4 = b'0      : Generation of A/D conversion end
109             interrupt is disabled                */
110          /* 3-2 = b'0    : reserve                */
111          /* 1 = b'0      : A/D conversion start by the external trigger
112             or an A/D conversion start trigger from
113             the MTU or MTU2S is disabled                */
114          /* 0 = b'0      : A/D converter is started by the A/D conversion
115             start trigger from the MTU2 or MTU2S                */
116
117      /* ---- A/D Analog Input Channel Select Register(ADANSR) ---- */
118      ADC.ADANSR.BYTE = 0x0F; /* AN0-AN3 */
119
120      /* ---- A/D Status Register(ADSR) ---- */
121      ADC.ADSR.BIT.ADF &= 0; /* ADF clear */
122
123      ADC.ADCR.BIT.ADST = 1; /* A/D conversion start */
124
125  }
126

```

4. Sample program listing: "main.c" (4)

```

127  /*"FUNC COMMENT"*****
128  * Outline      : A/D convert
129  *-----
130  * Include      : #include "iodefine.h"
131  *-----
132  * Declaration  : void ad_conv(unsigned short *ad_buf);
133  *-----
134  * Function     : Clearing the ADF flag, storing converted data
135  *-----
136  * Argument    : none
137  *-----
138  * Return Value : none
139  *-----
140  * Note        : none
141  /*"FUNC COMMENT END"*****/
142  void io_ad_conv(unsigned short *ad_buf)
143  {
144
145      while(ADC.ADSR.BIT.ADF == 0){
146          /* A/D conversion completion waiting */
147      }
148
149      *ad_buf++ = ADC.ADDR0;      /* AN0 */
150      *ad_buf++ = ADC.ADDR1;      /* AN1 */
151      *ad_buf++ = ADC.ADDR2;      /* AN2 */
152      *ad_buf++ = ADC.ADDR3;      /* AN3 */
153      ADC.ADSR.BIT.ADF = 0;      /* ADF clear */
154
155  }
156
157  /* End of File */
158

```

4. Documents for Reference

- Software Manual (REJ09B0051)
SH-2A, SH2A-FPU Software Manual
The most up-to-date version of this document is available on the Renesas Technology Website.
- Hardware Manual
SH7211 Group Hardware Manual (REJ09B0344)
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