

Introduction

An acoustic relay can be used to control devices (light switcher, electric heater, air cooler etc.) in response to a sound, or series of sounds.

How does it work?

An acoustic relay changes its output state only after some predefined number of acoustic signals (in our case it is equal to 2 claps), which should come sequentially for some period of time. If number of claps is greater, less, or the pause between claps is greater than defined, the acoustic relay won't change its output state.

After a simple modification, this device can be used as an acoustic controller. It will monitor the number of acoustic signals and change its output state accordingly. For example, if one acoustic sound comes, a light will be turned on, if two – heater, if three – air conditioner. Illumination can be controlled in the room, air conditioner mode can be chosen, motor speed can be controlled, etc.

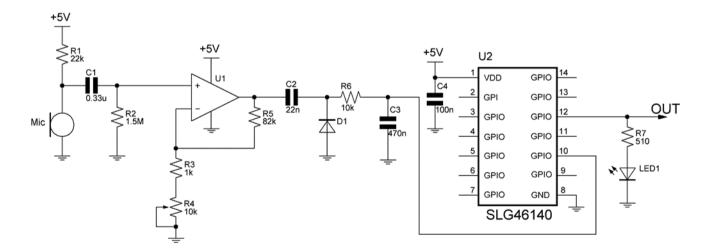
System description

This acoustic relay consists of a microphone, noninverting amplifier, diode detector, low frequency filter, and analyzing circuit.

Device operating principles

A clap generates a short, large amplitude pulse on the microphone's output. It goes through the capacitor C1 to OPAMP (U1) input with variable amplifying coefficient (from 7.5 to 82, changed by R4) for the sensitivity setting. After amplifying, this pulse will be detected as illustrated in Figure 2.

It is recommended to use diodes with small forward drop voltage (germanium or Schottky diodes), to minimize sensitivity loss. After detection, the pulse will be filtered and sent to PIN10 of GreenPAK4 IC.









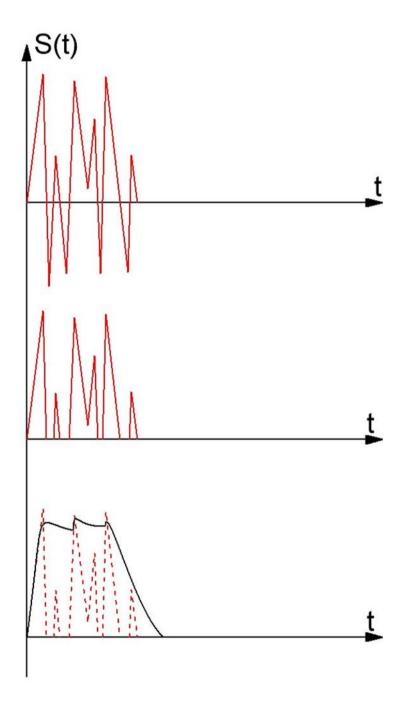


Figure 2. Detection and filtration process

Acoustic relay

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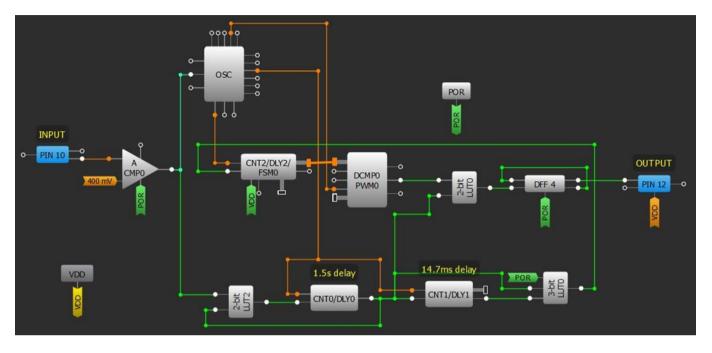


Figure 3. Design circuit

PIN 10 is configured as an analog input with 100K pull-down resistor for C3 capacitor discharge.

The pulse arrives at the ACMP0 input, where it will be compared with a 400mV reference voltage. ACMP0 hysteresis is enabled to prevent noise on the output.

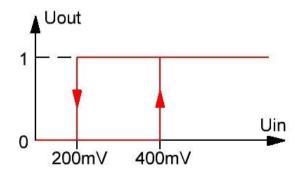


Figure 4. ACMP0 thresholds

Properties		(
	A CMP0	
Hysteresis:	200 mV	-
Low bandwidth:	Enable	*
Input 100uA current source:	Disable	•
IN+ gain:	Disable	•
Co	nnections	
IN+ source:	PIN 10	Ŧ
IN- source:	400 mV	*
In	formation	
Typical ACMP thres	holds	
V_IH (mV)	V_IL (r	nV)
400	200)
Powe	r ctrl. settings	
0 5	E App	ly

Figure 5. ACMP0 properties

Acoustic relay



If the input pulse exceeds ACMP0 threshold, an output pulse appears, which goes to the CNT2 input. CNT2 (up counting) data buss is connected to DCMP0, which compares CNT2 counter data with register 0 (DCMP EQ output goes High when data are equal). Changing register 0 values, it is possible to control the desired number of claps. DCMP0 out is connected to 2-bit LUT0. The ACMP0 output pulse also goes to the delay circuit based on 2-bit LUT2 and DLY0, which creates a 1.5 sec pulse (regardless of incoming pulses at the same time) and blocks 2-bit LUT0. DCMP0 EQ signal doesn't arrive at the 2-bit LUT0 during DLY0 operation. ACMP0 output pulse also goes to the delay circuit based on 2-bit LUT2 and DLY0, which creates a 1.5 sec pulse (regardless of incoming pulses at the same time) and blocks 2-bit LUT0. DCMP0 EQ signal doesn't arrive at the 2-bit LUT0 during DLY0 operation. If DCMP0 EQ is High, after DLY0 duration it will arrive at the 2-bit LUT0 and will change DFF4 state to inverse. If Low – nothing will be changed. DFF4 inverted output is connected to its D input, so DFF4 operates as a 1bit counter. DFF4 nReset is connected to POR, which provides the reset when VDD is switched.

roperties WS Ctrl/1	14-bit CNT0/DLY0	
Туре:	CNT/DLY	¥
Mode:	Delay	Ŧ
Counter data:	9360	\$
Delay time (typical):	(Range: 1 - 16383) 1.50 s Form	nula
Edge select:	Falling	٣
Counter value control:	Reset (counter valu	Ŧ
DFF bypass enable:	None	v
Co	nnections	
FSM data:	None	Ŧ
Clock:	CLK /4	٠
Clock source:	RC OSC Freq. /4	
Clock frequency:	6.25 kHz	
6 5	Apply	

Figure 6. DLY0 properties

Properties		
DCM	P0/PWM0	
DCMP/PWM power register:	Power on	Ŧ
Function selection:	DCMP	Ŧ
PD sync to clock:	Off	•
Clock source:	ADC CLK	Ŧ
Clock invert:	Disable	Ŧ
PWM & ADC clock source :	RC OSC	Ŧ
PWM data sync with SPI clock:	Disable	Ŧ
Duty cycle:	0% - 99.6%	Ŧ
PWM deadband time:	10 ns	Ŧ
Register 0: MTRX SEL: (0:0)	2	4
Register 1: MTRX SEL: (0:1)		4
Register 2: MTRX SEL: (1:0)		4
Register 3: MTRX SEL: (1:1)		4
Con	nections	
IN+ selector:	FSM0 [7:0]	Ŧ
IN- selector:	Register 0	¥
0 5	Apply	

Figure 7. DCMP0 properties

Acoustic relay



Properties	s			×
	2	-bit LUT	0	
IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0

Figure 8. 2-bit LUT0 and 2-bit LUT2 properties

3-bit LUT0					
IN3	IN2	IN1	INO	OUT	
0	0	0	0	1	
0	0	0	1	1	
0	0	1	0	1	
0	0	1	1	1	
0	1	0	0	0	
0	1	0	1	1	
0	1	1	0	0	
0	1	1	1	0	

Figure 9. 3-bit LUT0 properties

DLY1 and 3-bit LUT0 are used to make CNT2 reset on the falling edge of DLY0, or when VDD is taken off.

Conclusion

Using the SLG46140V allowed the following significant advantages:

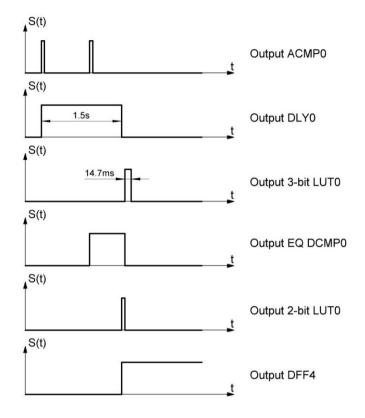


Figure 10. Design timing diagram

- Lower power consumption
- Smaller size (22 mm × 30 mm)
- Lower overall cost

Using the GreenPAK made the design of this acoustic relay easier and faster. Using this circuit one can create many other useful devices such as controllers for electric heaters, air coolers etc.

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