AC Phase Control Light Dimmer

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Introduction

This application note describes controlling power to AC circuits through AC phase control, or phase-cut circuitry. This is achieved by turning a TRIAC on/off after specific time intervals, synchronized with the AC signal. The TRIAC is on only during a part of the AC sine wave; this is called leading edge cutting. A GreenPAK4 IC provides a voltage controlled interface to set the level of dimming of an incandescent bulb.

The TRIAC triggering must be synchronized to the AC sine wave for predictable AC phase cutting. To achieve this, a reference point in the AC sine wave is required. For this purpose, a zero point crossing detection circuit is used which gives an input pulse of 5v at the digital input of the *GreenPAK4 SLG46140V.* After detecting zero point crossing, the TRIAC is turned on for a specific time but this time, it can be manipulated by the user via the GreenPAK code.

The Phase cutting of the AC load is determined by an analog input from the potentiometer to the GreenPAK4 SLG46140V. The user can use any customized waveform in the logic generator to obtain a customized waveform for the AC output signal.

Zero detection Circuit

The AC voltage passes through 2 resistors (33k, 1watt) and is rectified by the bridge rectifier (KBJ608G). This rectification results in a pulsating DC voltage that is fed to a phototransistor output optocoupler (4N25). The voltage lets the optocoupler stay on while keeping the zero-crossing signal (at the collector of the phototransistor) LOW until the voltage drops to 'zero'.

At the pertinent point, the optocoupler will not be conducting anymore and the zero-crossing signal will be pulled high until the pulsating DC voltage rises enough to send the optocoupler into conduction again, which eventually results in the zero-crossing pin going LOW.

The quality of that zero-crossing pulse is dependent on a number of factors, but the most important ones are: the speed of the optocoupler, the value of the collector resistor and the value of the two resistors in the main line.

If the collector resistor is too low then the optocoupler will burn out, but if it is too high, the voltage (at which there is still enough current going through the optocoupler to keep it conducting) will keep getting higher and higher.

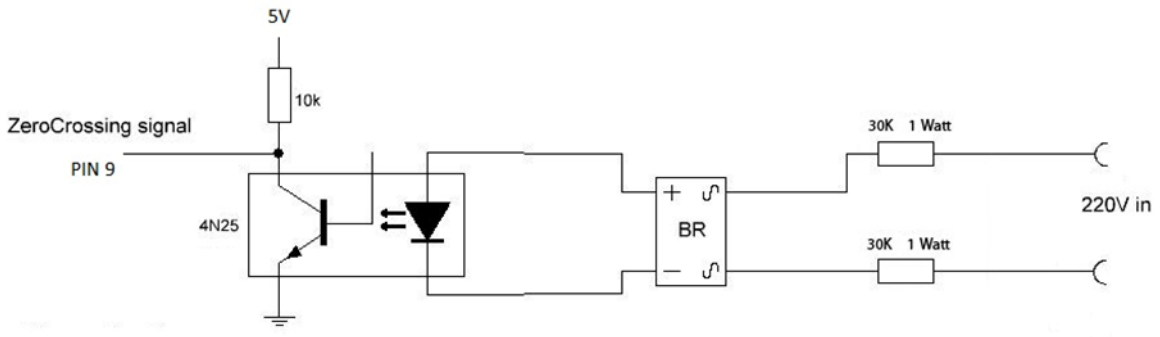

Figure 1. Zero-crossing circuit

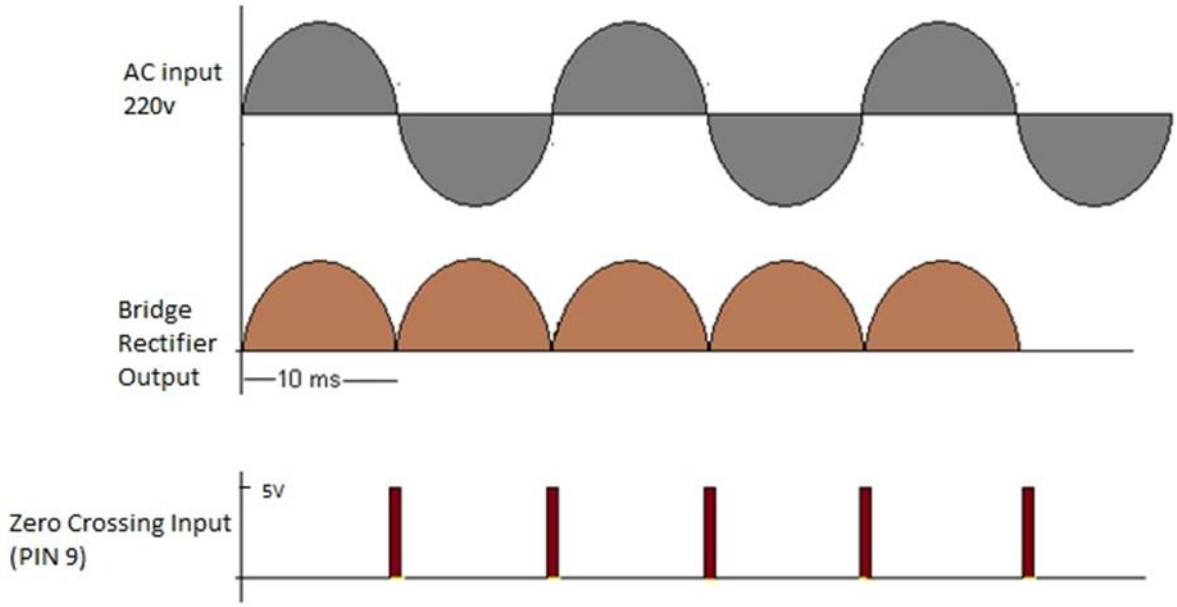

Figure 2. 220v ac, pulsating dc and optocoupler output waveforms

This means that if the resistor value is too high, the switching of the optocoupler will happen more frequently on the rising and falling flanks of the sine wave; resulting in a wide zero-crossing signal.

TRIAC Driver Circuit

After determining the zero detection, the SLG46140V circuit will turn on the TRIAC driver optocoupler (MOC3021). The time period for which the TRIAC driver optocoupler remains ON depends on a customized signal (between 0 to 1v) received by the SLG46140V ADC through a logic generator or some potentiometer.

Another important factor in determining the time for which the TRIAC driver operates is the frequency of the AC sine wave. For example, for a 50Hz frequency, each sine wave cycle takes 1000ms/50 = 20ms (milliseconds).

As there are two sine wave peaks in a wave, this means that after every zero detection, there is a 10ms period that can be regulated. So, the TRIAC driver (MOC3021) shall turn on/off the TRIAC (BT136) within 10ms.

The signal from the MOC3021 to the gate of the BT136 will turn the TRIAC ON. The TRIAC shall remain in the conduction state (irrespective of the input signal at its gate) until the half AC cycle. Therefore, the gate signal from the MOC3021 shall be turned off as soon as the BT136 starts conduction (so that it can turn the BT136 ON during the next AC cycle half and so on).

The customized signal from the logic generator or potentiometer at the analog input of SLG46140V will determine the time delay after which the TRIAC is set into conduction (turned ON and then OFF). This time shall start after the zero-crossing signal is detected.

If the TRIAC is turned ON in the beginning of the AC half cycle, the load will receive full power. Also, if the TRIAC is turned ON at the end of the 10ms period, the load will receive no power; at the halfway, the load will receive half power. If the logic generator or potentiometer signal is not constant the load will receive variable power.

GreenPAK design code

1. Zero Detection Signal

The zero detection signal from the zero detection circuit shall terminate at PIN 9 (Digital Input) of the GreenPAK4 SLG46140V. The zero-crossing signal has a frequency of 100Hz (since a 50 Hz AC waveform signal crosses zero 100 times).

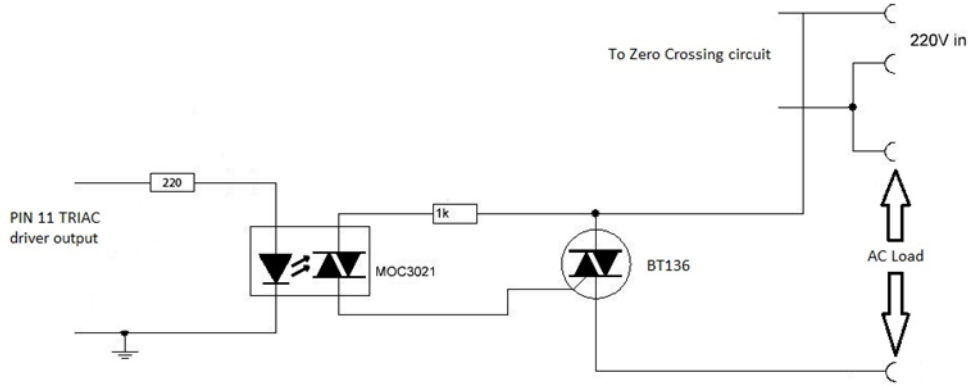

Figure 3. TRIAC operating circuit

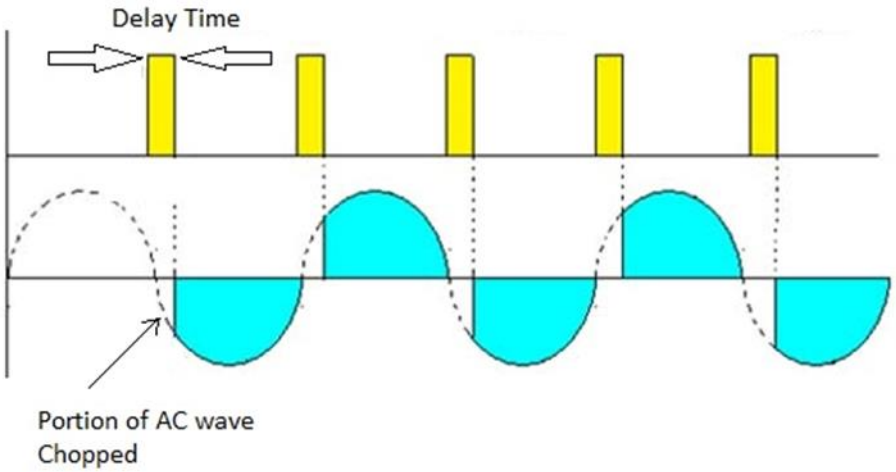

Figure 4. AC input and output waveform (after Phase cutting)

The PIN 9 signal is low but there is a high pulse whenever zero is crossed by AC sine wave.

The circuit with two NOR gates (2-L3 & 2-L4) will work as a RS latch. The latch is set to 'ONE' (logic High) whenever a pulse is detected at the input of 2-L3 NOR gate. So whenever the AC sine wave crosses zero, a high pulse is detected at the Digital input PIN 9 and it will eventually set the output of RS latch to 'ONE' (Logic High).

The RS Latch has two inputs for its reset circuit. One of them comes from the Digital input PIN 4 through the OR gate 2-L2; this input is optional and is for testing purposes only. The other one is from the TRIAC driver Digital output and will be explained later in the application note.

2. TRIAC ON Loop after Zero Detection

Once the zero-signal is detected by the RS Latch, its output is set to ONE. The next phase is to turn the TRIAC driver optocoupler MOC3021 ON and hence turn the TRIAC BT136 ON. The TRIAC needs to be turned ON after a specific period of time and this time is determined by the ADC input to the Counter CNT3/DLY3/FSM1.

In the properties of the Oscillator block OSC, the RC OSC tab is selected and the property RC OSC power mode is set to force the power on.

The property RC OSC frequency is set to 25 kHz. The cycle time for this frequency is 0.04 milliseconds.

It helps in the counter counting and delay signals since the application needs to deal with a total time of 10ms. For an 8-bit counter (which has a maximum of 255 counts), the clock with a cycle time of 0.04ms needs a total counts of 250 (250 x 0.04 = 10ms).

The property Clock selector is set to RC OSC; but if an external clock is to be used, it can be set to EXT CLK 0.

Once the RS Latch output signal is HIGH, it is sent to RESET the IN pin of the Counter CNT3/DLY3/FSM1 block.

The counter is actually a 3-bit LUT7/8-bit CNT3/DLY3/FSM1. Once selected, its Type property is changed to CNT/DLY, so that it will get converted into a 14-bit counter/delay block.

The Mode property is set to Delay, which converts the block to a Delay block. The Edge Select property is set to Rising which will delay the rising edge of the RESET IN signal.

In counter FSM data property choose ADC which will allow the counter to take the input from ADC block. Based on this input, the delay time to turn the TRIAC ON shall be determined.

The clock signal of the delay block is 25 KHz clock signal. It means that when the RS Latch output is high, the delay block gets reset and generates a single pulse signal (of 25 KHz clock) at the "OUT" output of the delay block. But, since this is a delay block, the OUT will go to high state after a delay.

The delay time of the block will determine how long the 'OUT' output shall take to go to a high state once the RESET IN is high.

3. Delay time from ADC

The PIN 6 is configured as an Analog input; this pin can take the input signal from a logic generator (emulation) or an external signal from a potentiometer. In this example, the logic generator is used to configure a signal which varies from 0 to 1v in small steps, as shown below.

Alternatively, the signal of 0 to 1v can be given from a potentiometer at Analog input PIN 6.

The input signal of 0 to 1v is then sent to the PGA block.

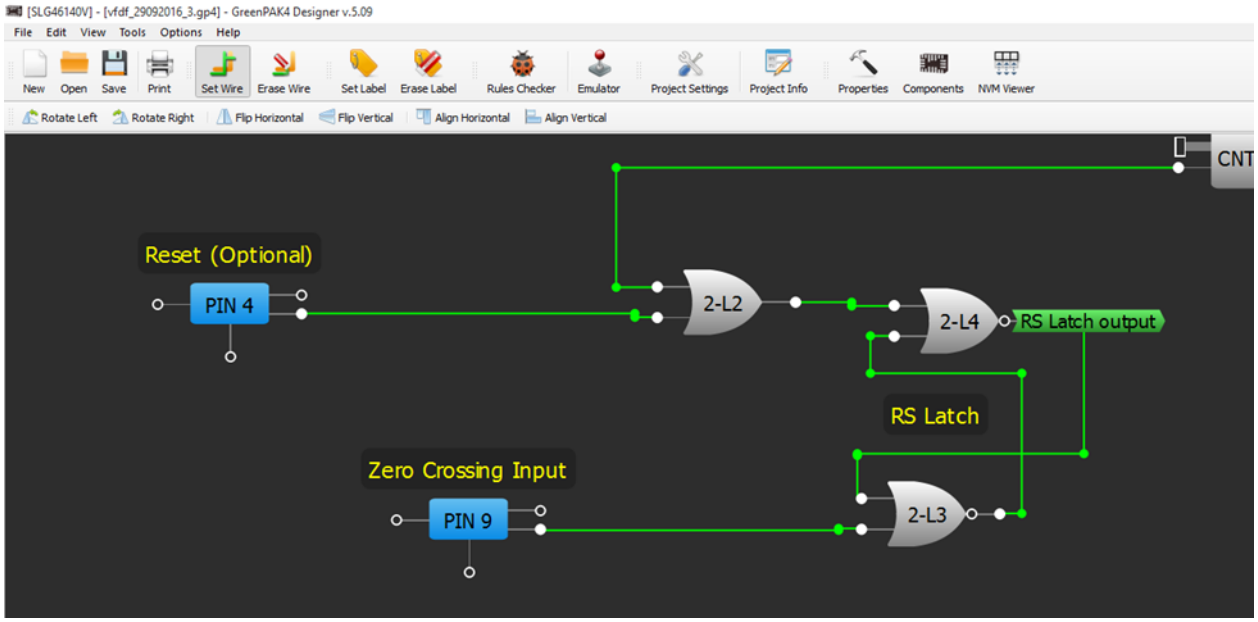

Figure 5. Zero-Cross Signal stored in the RS Latch

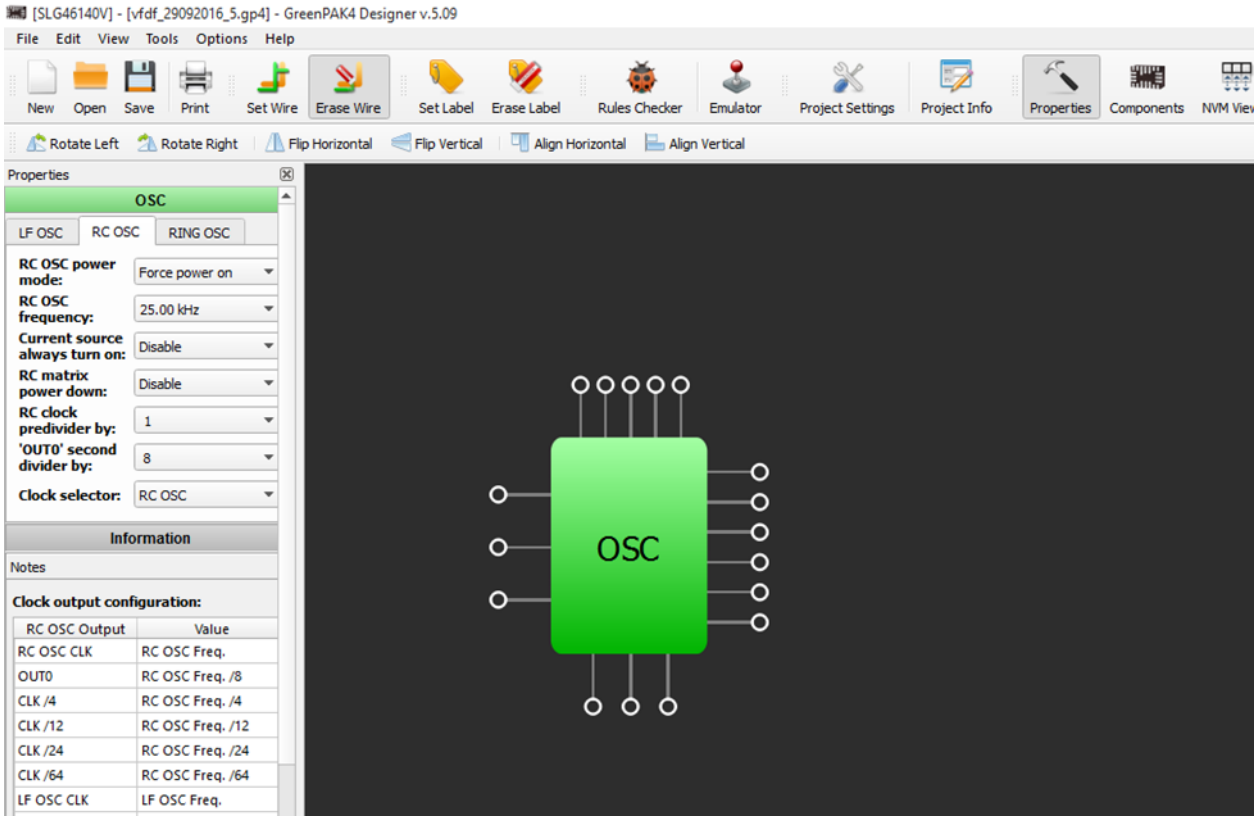

Figure 6. OSC block properties

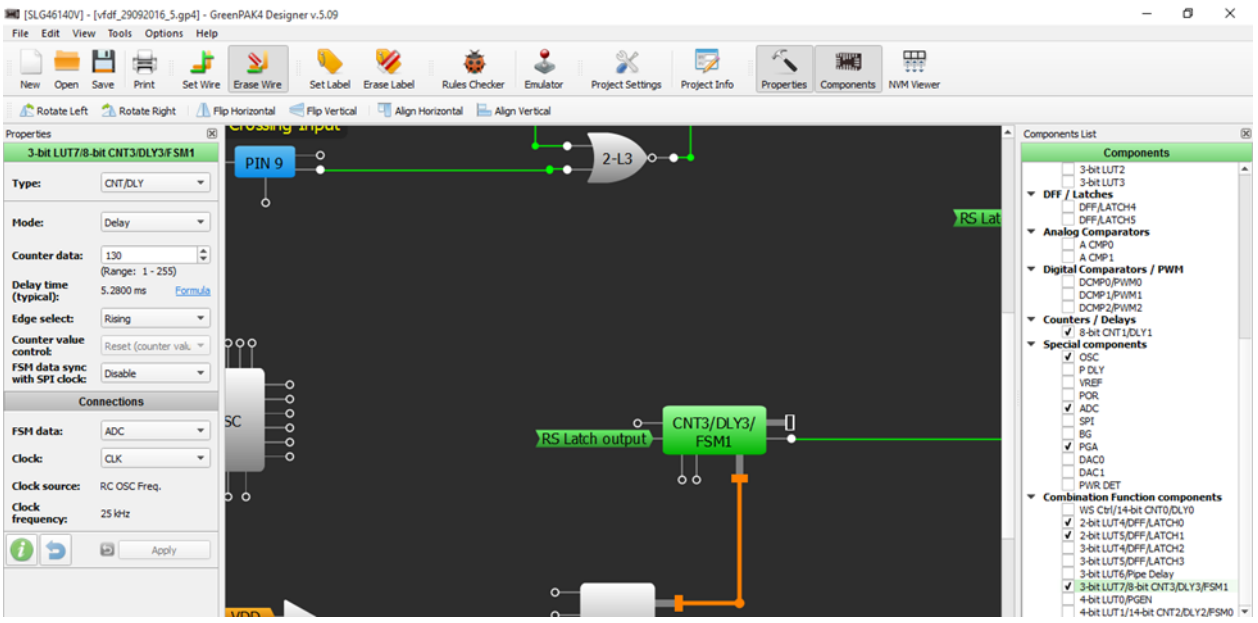

Figure 7. Delay block (CNT3/DLY3/FSM1) properties

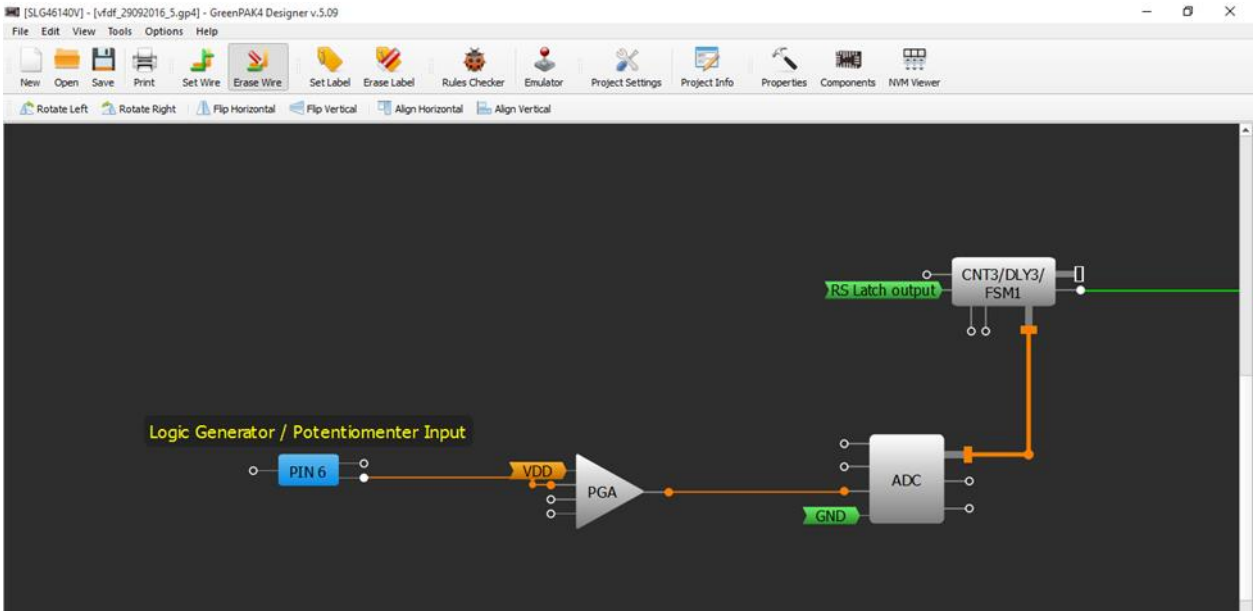

Figure 8. Delay time loop

In the properties of the PGA block, the **Power on** signal needs to be set to *Power on* and the **Gain** property has to be set to *x1*. The gain property can be used to amplify the input, up to 8 times. ADC mode property is set to *single ended.*

The output of the PGA is then sent to "*PGA in*" input of the ADC block; the *Vref* property of the ADC is set to internal 1.0v. The clock source is RC OSC.

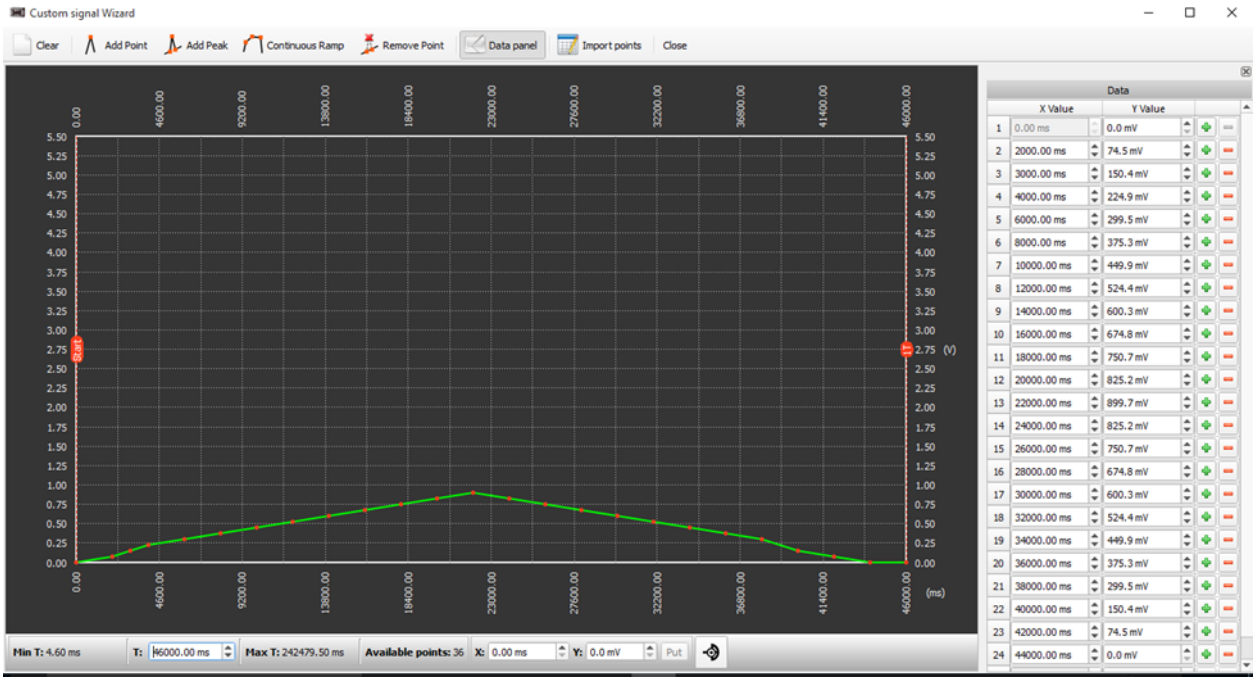

Figure 9. Logic generator signal configuration

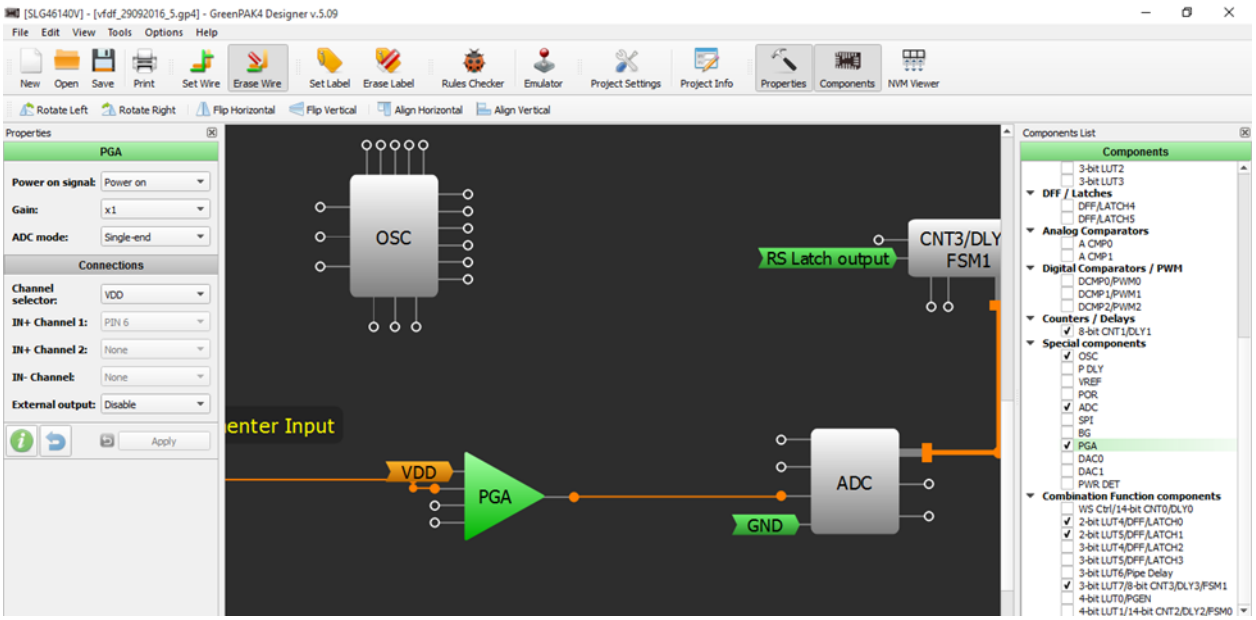

Figure 10. PGA block properties

The PAR DATA output of the ADC block is attached to the DATA IN input of the delay block CNT3/DLY3/FSM1.

Now, the input signal at the analog input PIN 6 (from logic generator or potentiometer) is passed through the PGA block, which does not amplify the input signal.

The signal is then sent to the ADC block which converts the signal into an 8 bit data stream.

This 8 bit data is sent to the PAR DATA, which in turn, sends it to the DATA IN pin of the delay block. The data from the ADC is the delay time in counts for the RS Latch output HIGH signal.

The RS Latch output signal gets turned to HIGH after this delay time.

The 0 to 1v analog input at the PIN 6 is mapped at 0 to 255 (8-bit data), which is then mapped on a time scale of 0 to 10ms. For example, an input signal of 0.5v at the input is mapped at 0 to 127 (8-bit data), which is equivalent to a delay time of 5ms. So the RS latch *High* output signal is delayed by a time of 5ms as it passes through the delay block.

4. Turning the TRIAC driver ON

The output signal of the delay block is then set to the 2-L5 AND gate. Since the RS Latch output is HIGH and it has already enabled the AND gate, therefore, the delayed signal from the delay block shall pass through the AND gate.

It then turns the TRIAC driver MOC3021 ON by setting the Digital output PIN 11 to HIGH.

The MOC3021 then turns the TRIAC BT136 on by setting a HIGH at its gate input. This lets a portion of the AC wave half cycle to pass through it.

The TRIAC turns off automatically once the AC wave *zero* is reached. Similarly, the TRIAC shall get turned ON in the next half cycle after a time delay followed by getting switched off automatically once the zero gets reached. For a 50HZ input frequency signal, the TRIAC is turned ON and OFF, 100 times in one second.

5. Turning the TRIAC driver OFF

We mentioned above that the TRIAC BT136 needs to be turned ON during every half cycle of the AC signal. So, the Digital output signal (PIN 11) needs to be reset as soon as the TRIAC gets turned ON (So that it can turn the TRIAC driver MOC3021 on during the next half cycle of AC sine wave).

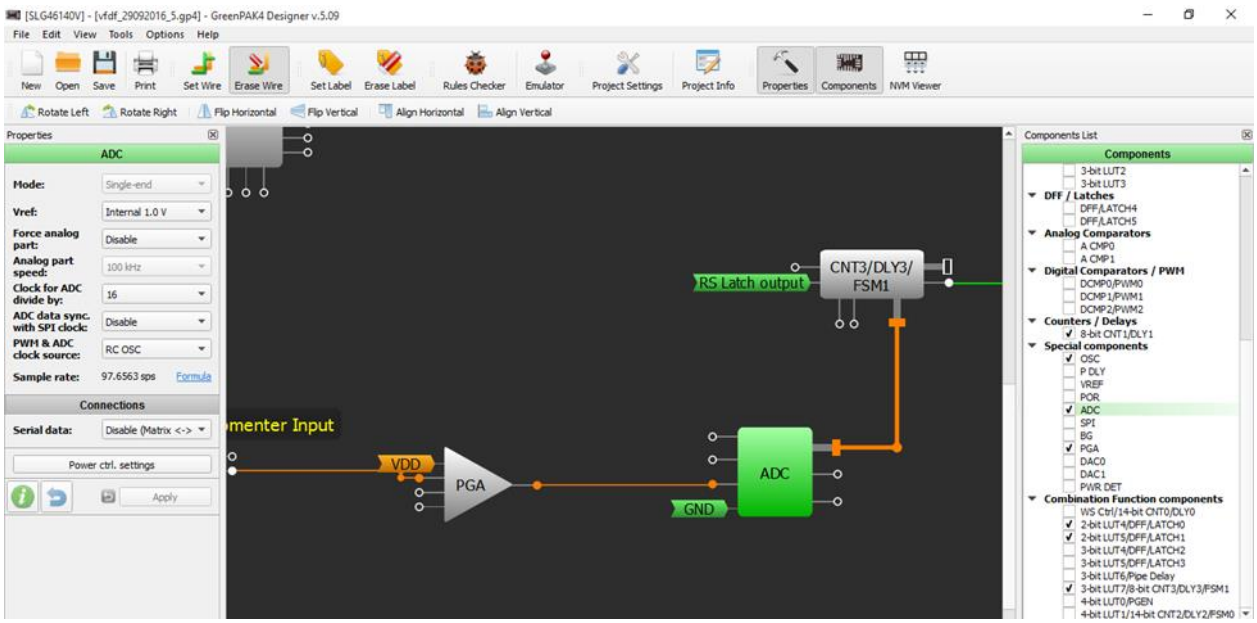

Figure 11. ADC block properties

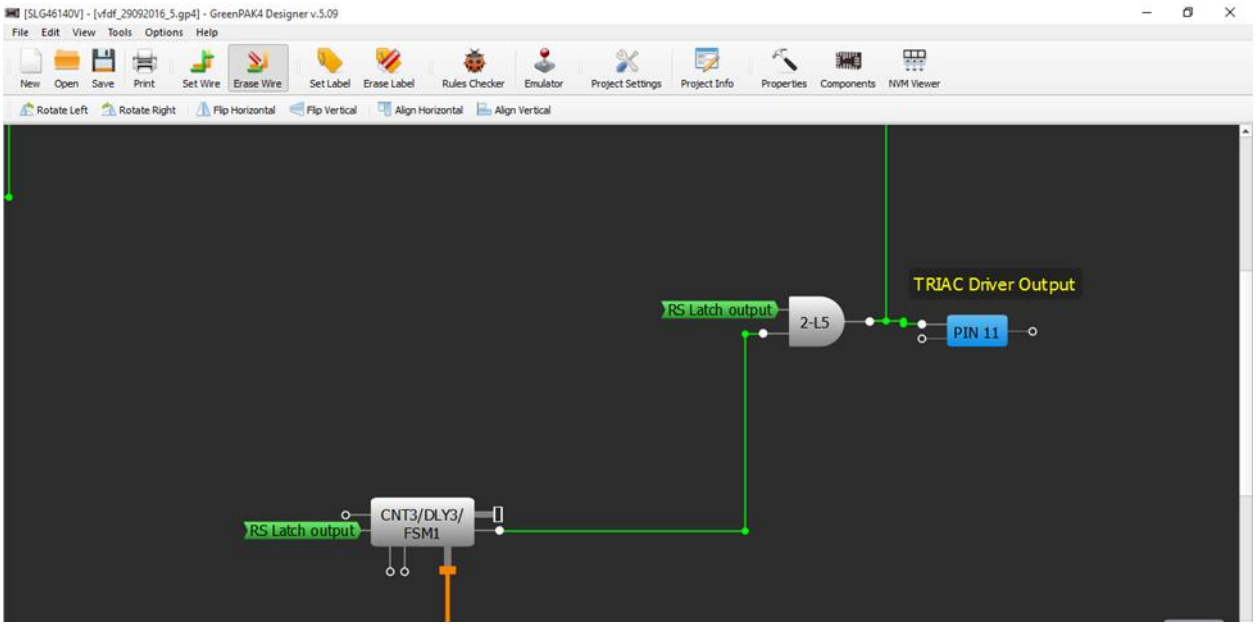

Figure 12. Turning ON TRIAC driver

Once turned ON, the TRIAC does not need a high signal at its gate during the half cycle of AC sine wave; this is because it continues to operate until the half cycle ends.

The output of the 2-L5 gate is fed back to the reset pin of the RS Latch after passing through a delay block CNT1/DLY1 and the 2-L2 OR gate.

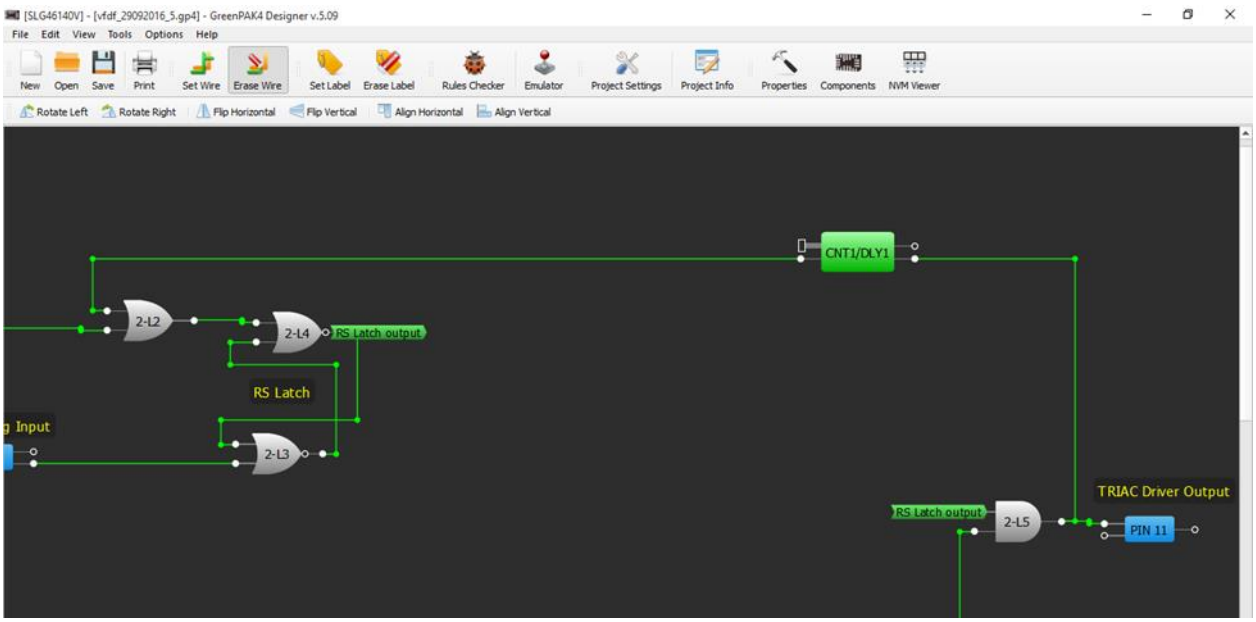

Figure 13. Reset TRIAC driver output

The delay block is used for those TRIACs that need some more time for their gate signal. The delay block CNT1/DLY1 can delay the high signal at its input by a time determined by the counter data property; this time can be configured by the user. Keeping this time less is significant in reliable cutting of the AC signal; so a TRIAC with less time (required for the gate signal) must be chosen.

The high output of the 2-L5 will reset the RS Latch output to LOW after a delay time determined by CNT1/DLY1 block. The low RS Latch output will turn the output of 2-L5 gate to LOW; which as a result, turns the TRIAC driver off.

Example Application

An example application of AC waveform cutting is a light dimmer. The intensity of a bulb can be varied by varying the cutting of the AC waveform signal. The code included with the application has a logic generator configured at its analog input PIN 6.

The logic generator slowly decreases the intensity of a bulb until it is completely off and then slowly increases the intensity to full brightness. The video of this example is also attached.

For inductive AC loads (like fans, AC motors etc.), the AC waveform cutting must be done with care because heavy motors behave unpredictably at low voltages. Brush type AC motors are easier.

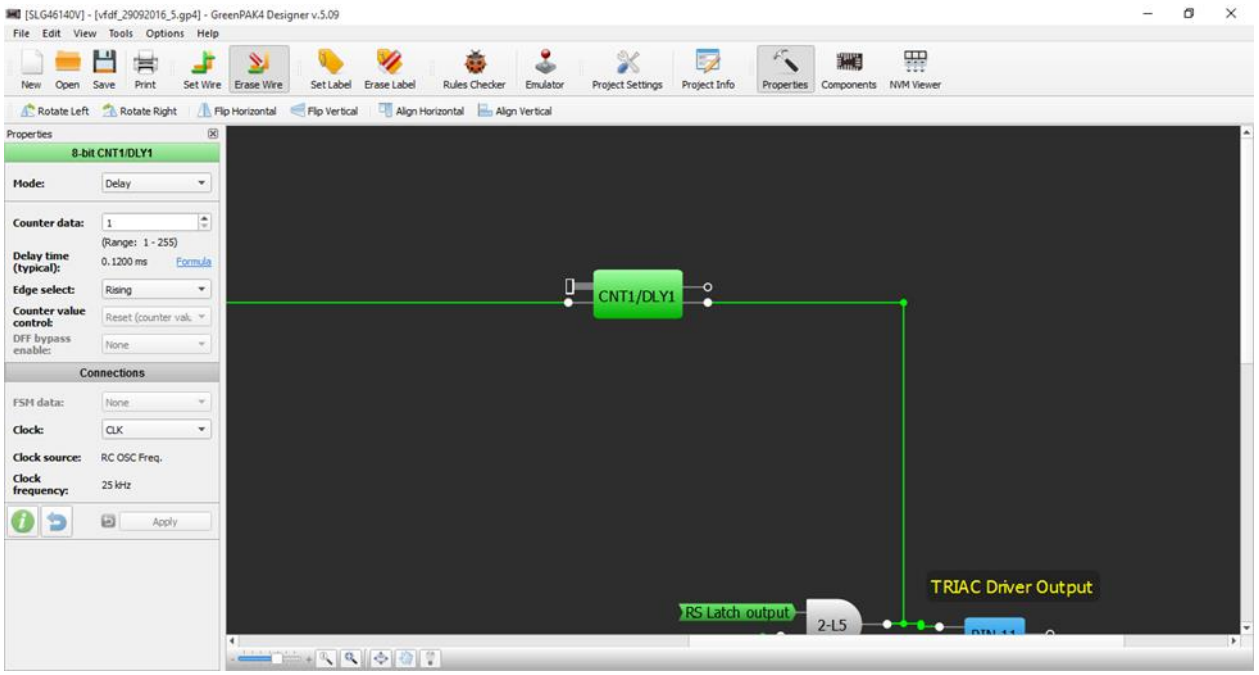

Figure 14. Delay block (CNT1/DLY1) properties

Conclusion

AC power can be varied quite precisely using this phase control circuit. We demonstrated proper TRIAC conduction by controlling its gate input from a fast switching optocoupler.

The GreenPAK SLG46140V IC provides the timing, and a voltage controlled input for many interface devices. This application example showed an incandescent lamp dimmer circuit, and other resistive loads are compatible such as heater elements, coffee makers. The voltage controlled input is suitable for some home automation device interfaces.

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