6-Channel Power Lines Sequencer

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Introduction

This application note describes the design of a 6 channel power lines sequencer. It can be used for switching supply rails on/off in a predetermined order with constant or variable delays.

Power Lines Sequencer circuit design

To design this sequencer it is necessary to construct a generator which sets the delay time, and DFFs and LUTs are used to shift the signal edges. Using blocks combinations “3-bit LUT + DFF” (cells) it is possible to sequence as many lines as the number of cells you have available. Cell configuration is shown in Figure 2, where N-1 = previous cell, N+1 = next cell.

The Generator block is made using 4-bit LUT0, CNT1/DLY1, 2-bit LUT1 and P DLY.

Blocks configurations are presented in figures 1-9.

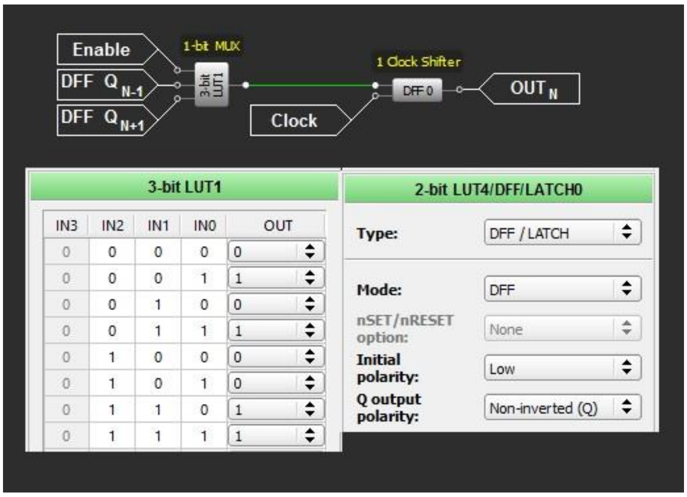

Figure 2. 3-bit LUT + DFF “cell” connections and configuration

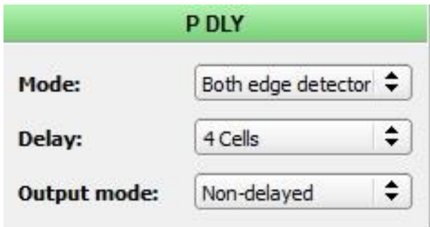

Figure 3. P DLY configuration

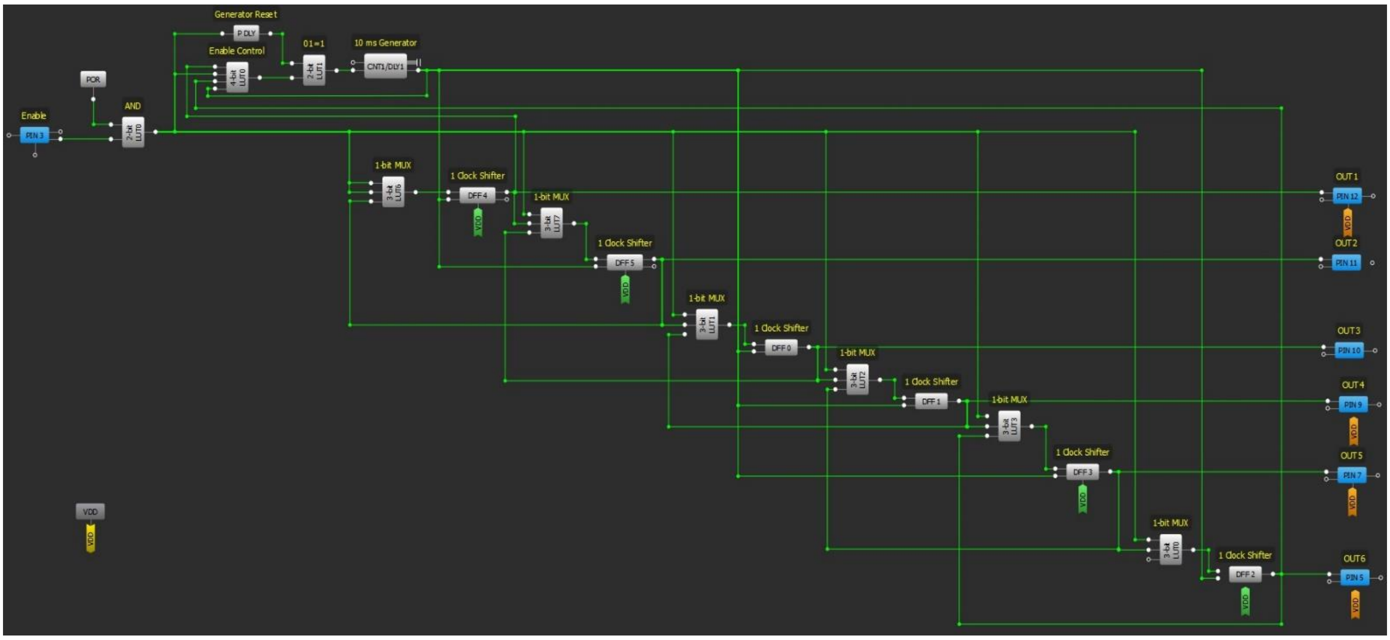

Figure 1. Power Lines Sequencer schematic

Figure 4. PINs configuration

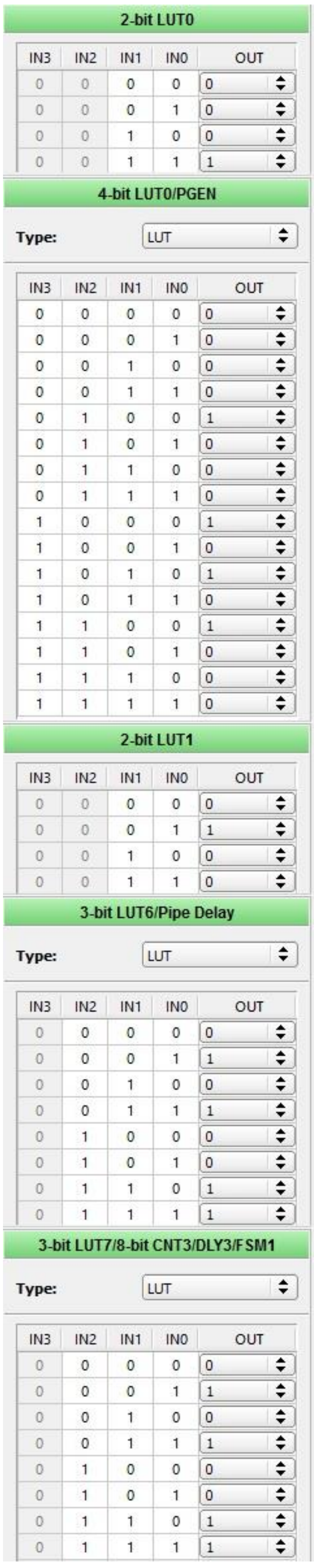

Figure 5. LUTs configuration

3-bit LUT1

IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1

3-bit LUT2

IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1

3-bit LUT3

IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1

3-bit LUT0

IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1

Figure 6. LUTs configuration

DFF/LATCH4

Mode:	DFF
nSET/nRESET option:	nRESET
Initial polarity:	Low
Q output polarity:	Non-inverted (Q)

DFF/LATCH5

Mode:	DFF
nSET/nRESET option:	nRESET
Initial polarity:	Low
Q output polarity:	Non-inverted (Q)

2-bit LUT4/DFF/LATCH0

Type:	DFF / LATCH
Mode:	DFF
nSET/nRESET option:	None
Initial polarity:	Low
Q output polarity:	Non-inverted (Q)

2-bit LUT5/DFF/LATCH1

Type:	DFF / LATCH
Mode:	DFF
nSET/nRESET option:	None
Initial polarity:	Low
Q output polarity:	Non-inverted (Q)

3-bit LUT5/DFF/LATCH3

Type:	DFF / LATCH
Mode:	DFF
nSET/nRESET option:	nRESET
Initial polarity:	Low
Q output polarity:	Non-inverted (Q)

3-bit LUT4/DFF/LATCH2

Type:	DFF / LATCH
Mode:	DFF
nSET/nRESET option:	nRESET
Initial polarity:	Low
Q output polarity:	Non-inverted (Q)

Figure 7. DFFs configuration

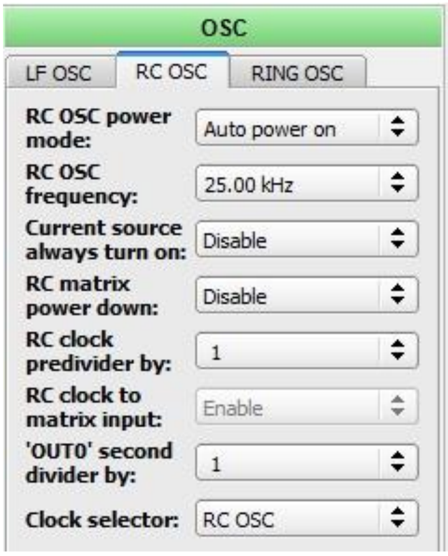

Figure 8. ADC properties

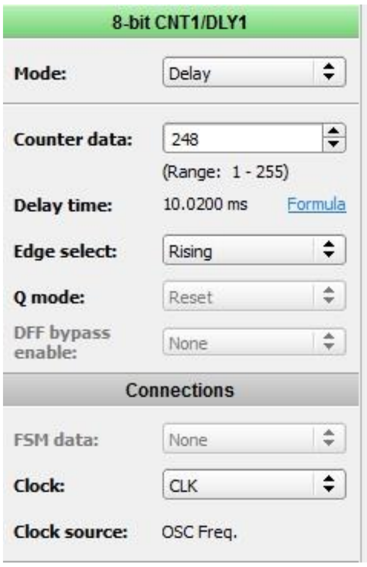

Figure 9. DLY1 configuration

Power Lines Sequencer circuit analysis

As we know, a DFF can shift an input signal (D input) by 1 clock. The point is to form this input signal using existing signals (Enable, Previous line, Next line), which are applied to 3-bit LUT.

This 3-bit LUT operates as a MUX and outputs N-1 signal when Enable is HIGH, and N+1 signal when Enable is LOW (see figure 10).

4-bit LUT0 is used to turn on/off the generator when it is necessary to decrease current consumption. Its output will invert the IN0 input signal until the lines are all HIGH or all LOW (see figure 10). 2-bit LUT1 repeats the 4-bit LUT0 value when P DLY output is LOW. When the pulse comes from PDLY block, 2-bit LUT1 output goes LOW. This will reset the generator on the rising or falling edge of Enable signal, and that provides proper delay for the last (6^{th}) line's falling edge (figure 11).

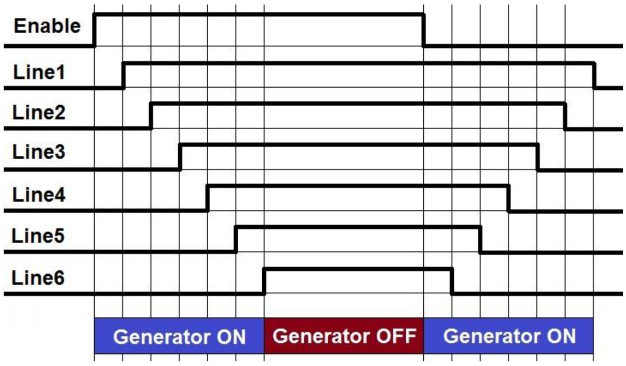

Figure 10. Power Lines Sequencer theoretical timing diagram

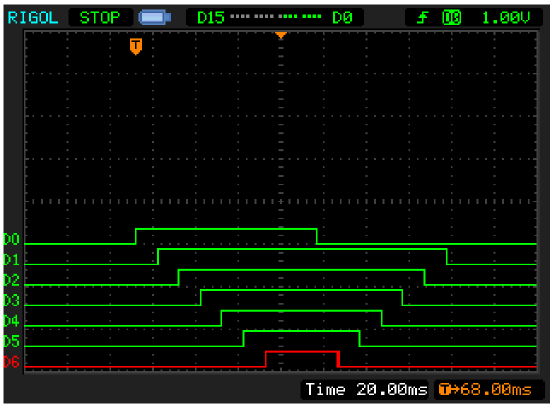

Figure 11. Power Lines Sequencer Scope Shot D0 – Enable; D1 – Line1; D2 – Line2; D3 – Line3; D4 – Line4; D5 – Line5; D6 – Line6.

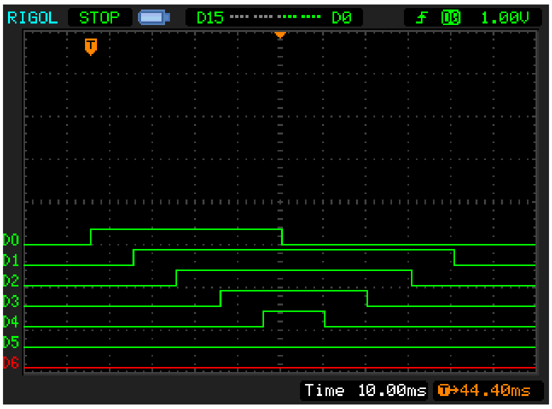

Figure 12. Power Lines Sequencer Scope Shot D0 – Enable; D1 – Line1; D2 – Line2; D3 – Line3; D4 – Line4; D5 – Line5; D6 – Line6.

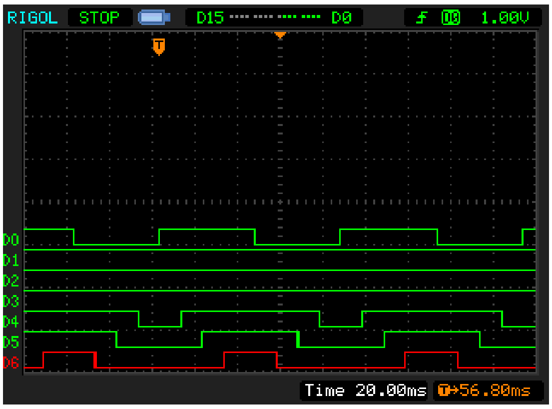

Figure 13. Power Lines Sequencer theoretical timing diagram D0 – Enable; D1 – Line1; D2 – Line2; D3 – Line3; D4 – Line4; D5 – Line5; D6 – Line6.

In the case when Enable goes low before some lines are driven high, these lines will stay LOW (see figure 12).

In the case Enable signal comes before some lines are driven LOW, these lines will stay HIGH (see figure 13).

No additional blocks are required to provide these functions. It is realized only with 3-bit LUTs and DFFs, described earlier.

Also it is possible to make a circuit simplification (Figure 14). That can be done for the first and last 3-bit LUT + DFF cells. In the first case, Enable signal and "Previous line" have the same timing. So 3-bit LUT can be replaced with a 2-bit LUT, configured as an OR gate (see figure 15).

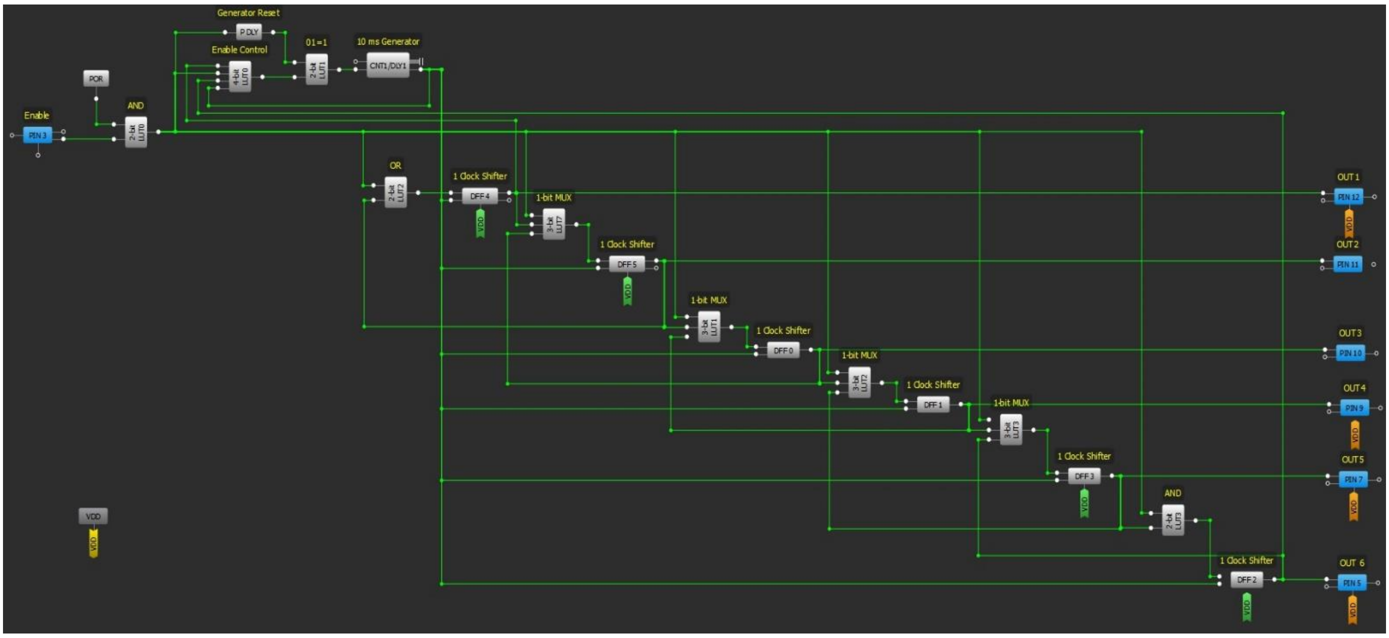

Figure 14. Simplified Power Lines Sequencer circuit design

As for the last line, there is no Next line and one of the 3-bit LUT's inputs stays LOW all the time. This LUT can be replaced with a 2-bit LUT (AND gate) as well (figure 15).

Power Lines Sequencer with variable delay time

Using a state machine instead of a simple Delay block makes it possible to change a delay time by loading counter data from the ADC. The Power lines sequencer with variable delay time circuit is presented in figure 17.

Configuration of the LUT + DFF cells remains the same, but there are some changes in the generator operation process and some blocks are added (see figure 17). The corresponding Blocks configuration is shown in figures 18-22.

2-bit LUT2

IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1

2-bit LUT3

IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1

Figure 15. 2-bit LUTs configuration

PIN 6

I/O selection:	Analog input/outpu
Input mode: OE = 0	Analog input
Output mode: OE = 1	Analog output
Resistor:	Floating
Resistor value:	Floating

Figure 16. PIN6 properties

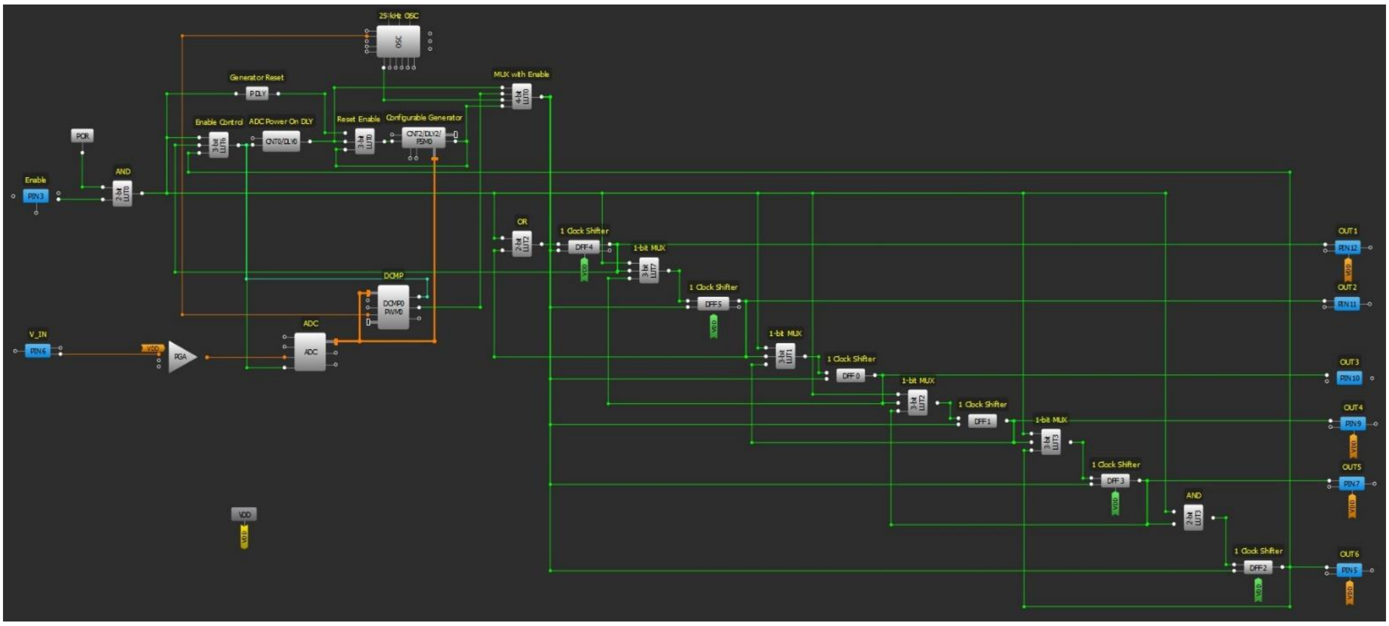

Figure 17. Schematic of Power Lines Sequencer with variable delay time

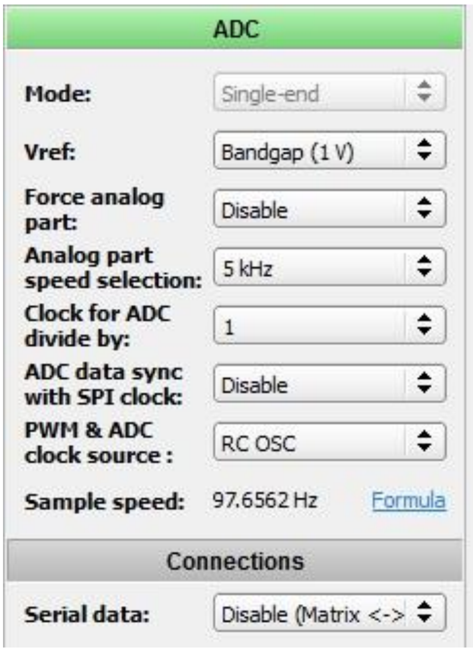

Figure 19. ADC properties

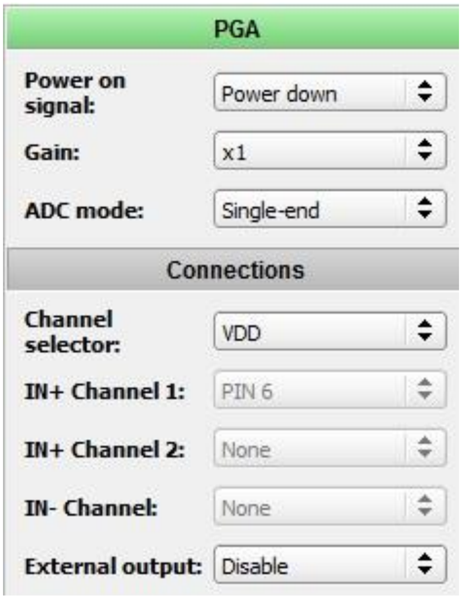

Figure 18. PGA properties

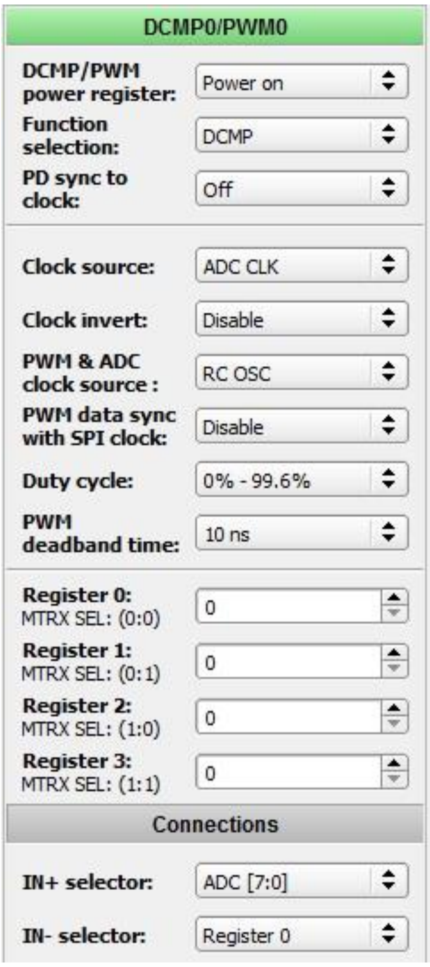

Figure 20. DCMP properties

Figure 21. DLYs properties

Figure 22. LUTs properties

An analog voltage comes from PIN6, configured as analog input, to the PGA and then – to ADC block, which converts it into 8-bit code. Then this code can be loaded into CNT2/DLY2/FSM0 block as counter data. So by the changing Pin6 analog input voltage, it is possible to change delay time between power lines switching. As in previous circuits, the generator operation time range is determined by LUT "Enable Control", but for generator reset (by P DLY in both edge detector mode) 3-bit LUT0 is used. CNT0/DLY0 block is needed to switch generator on after the ADC outputs its first proper parallel data. When the ADC input voltage is less that ADC offset (about 50mV), the ADC will output 8-bit logic 0, which will make the generator not operational. To remedy this situation, DCMP checks if ADC data is equal to 0. If it is, a 1-bit MUX with Enable (4-bit LUT0) will output its signal (after CNT0/DLY0 delay) from the OSC (minimum delay time). If it is not equal to 0 – then signaling is from CNT2/DLY2/FSM0 + 3-bit LUT0 generator.

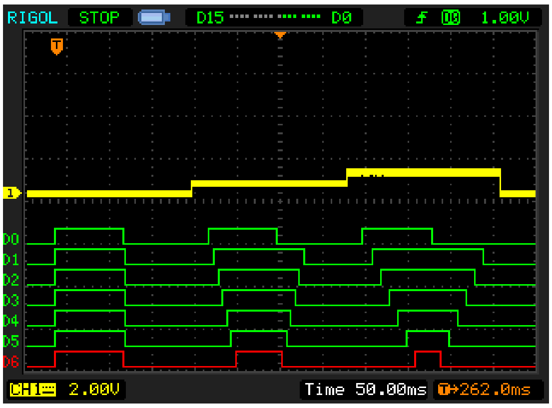

Figure 23. Timing diagram of Power Lines Sequencer with variable delay
CH1 – V-IN; D0 – Enable; D1 – Line1; D2 – Line2; D3 – Line3; D4 – Line4; D5 – Line5; D6 – Line6.

Conclusion

Using only one SLG46140 chip it is possible to create a power lines sequencer for six (or even more) lines with constant or variable delay between lines switching. Current consumption is also optimized (at 3.3V VDD): 150uA during lines switching on/off (dynamic), and 0uA when lines are are settled (static).

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