4 Channel Power Up/Down Sequencer Using GPAK

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Introduction

Modern day electronics often have multi-core and multi-rail processors that require regulated power up sequencing for each rail in order to maintain proper operation. Some processors also require regulated power down sequencing for each rail in order to maximize processor life cycle.

The GreenPAKs consist of various analog and digital building blocks called “macro cells”; the delay and look-up-table cells can be used to build highly intelligent sequencers with reconfigurable turn on and turn off sequence. This app note goes over 3 example designs.

Design 1: Power Up Only Sequencing

GreenPAK’s delay macro cells “CNTx/DLYx” can be used to generate daisy-chained delays starting from an enable signal as shown in figure 1. Sequencing begins at the rising edge of the “EN” pin. A 2-bit Look-Up-Table (LUT) is used to make sure the GreenPAK’s power-on-reset (POR) is met when the sequence begins. The “CNT0/DLY0” cell introduces a delay from EN high to OUT0 high. The “CNT1/DLY1” cell then introduces a delay from OUT0 high to OUT1 high and so on. The 3-bit LUTs between the delay cells and output pins realize an AND function. When “Enabled” is high, these LUTs make sure an output turns high with some delay after the previous rail turns high. When “Enable” is low, these LUTs make sure all outputs are pulled low instantaneously and simultaneously as show in Figure 2.

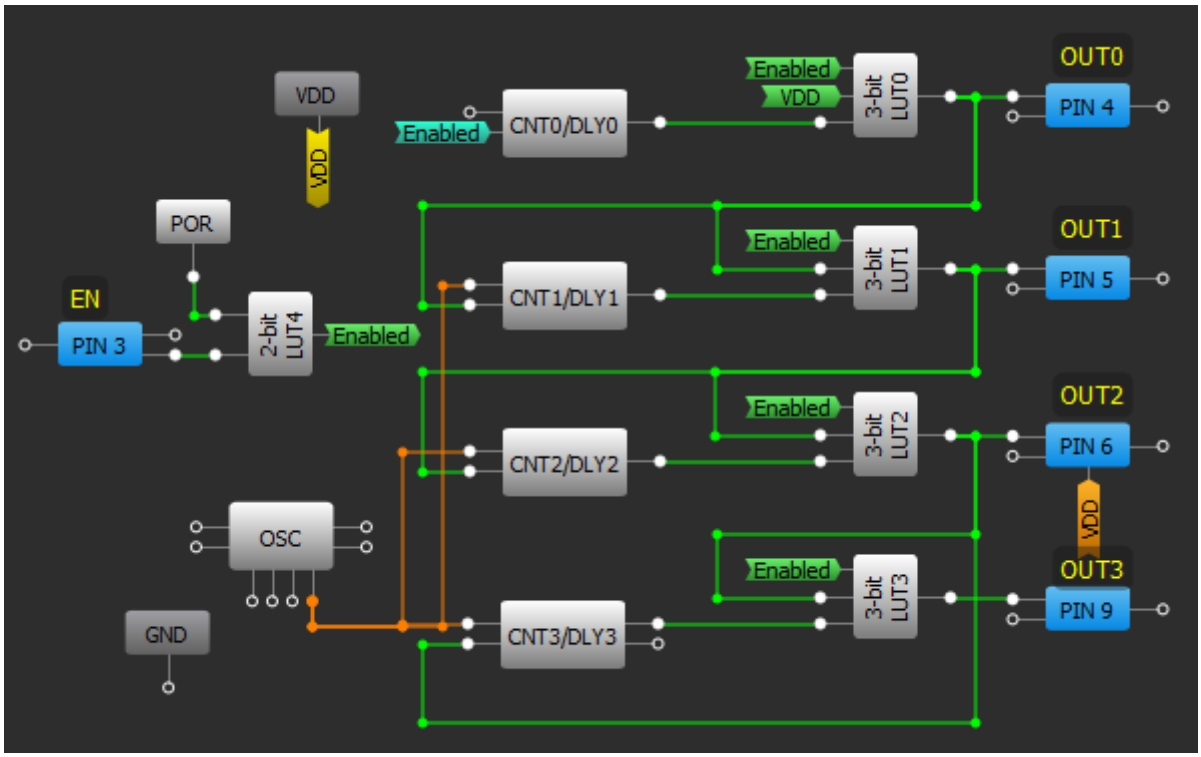

Figure 1. Power up sequencer block diagram

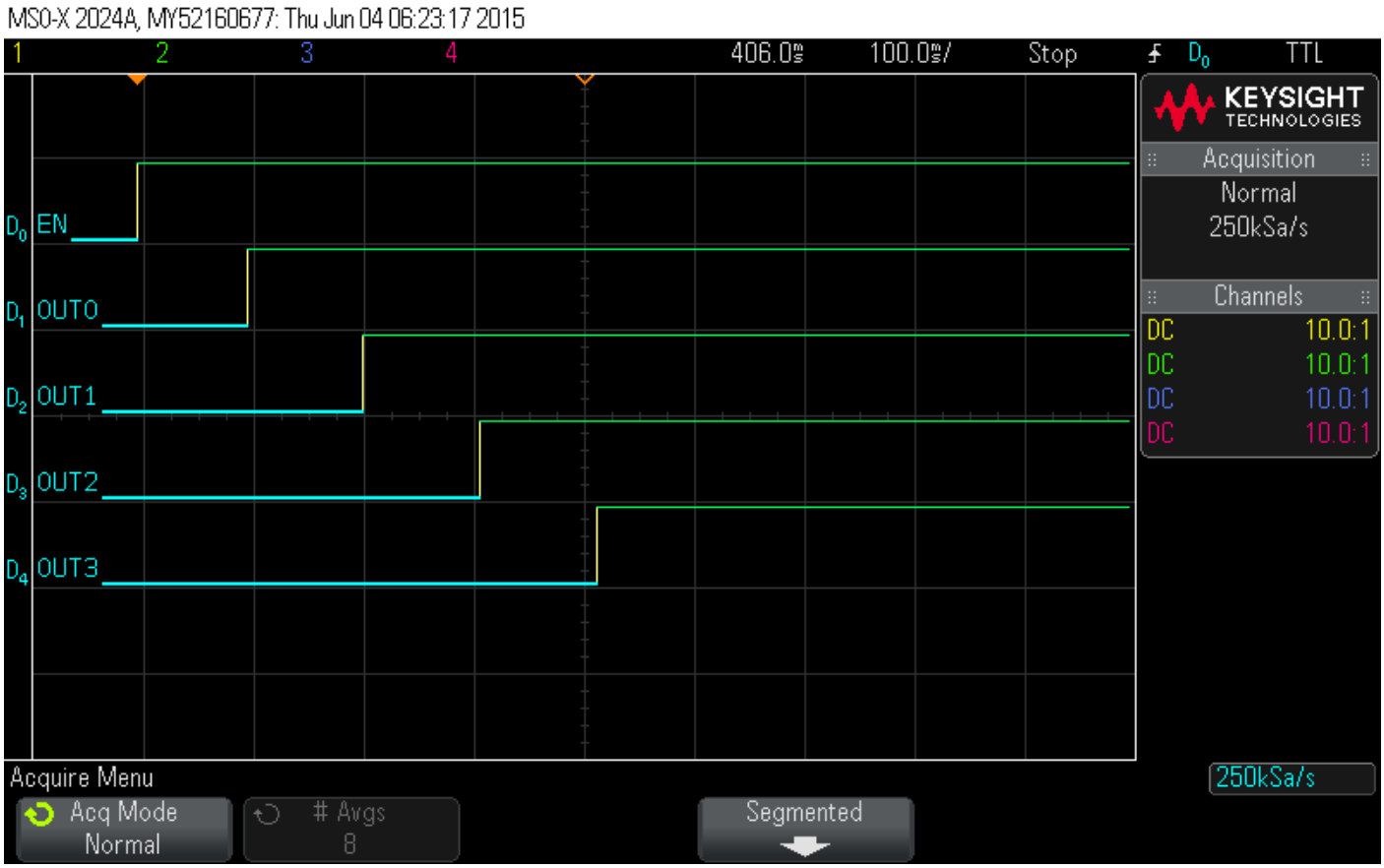

Figure 2. Power up sequencing waveform

Design 2: Power Up and Power Down Sequencing

In addition to power up sequence, power down sequence can also be realized as shown in figure 3. Comparing with figure 1, notice how the wirings have changed slightly in figure 3. When EN is high, the LUTs make sure an output turns high with some delay only after the previous rail turns high. When EN is low, these LUTs make sure an output turns low with some delay only after the previous rail turns low. The timing waveform is shown in figure 4. The logic states of the LUTs used are shown in the appendix.

Design 3: Sequencing with PG indicator

Often times the outputs of a sequencer are used to enable individual DCDC converters, which turn on different cores inside a processor at different times. Sometimes these DCDC converters have an unknown amount of turn on time, so the sequencer needs a PG signal from the converters before enabling the next converter. Figure 5 shows a modified power up and down sequencer with PG input. Now an output needs to wait for a PG signal from a previous rail's converter before going high.

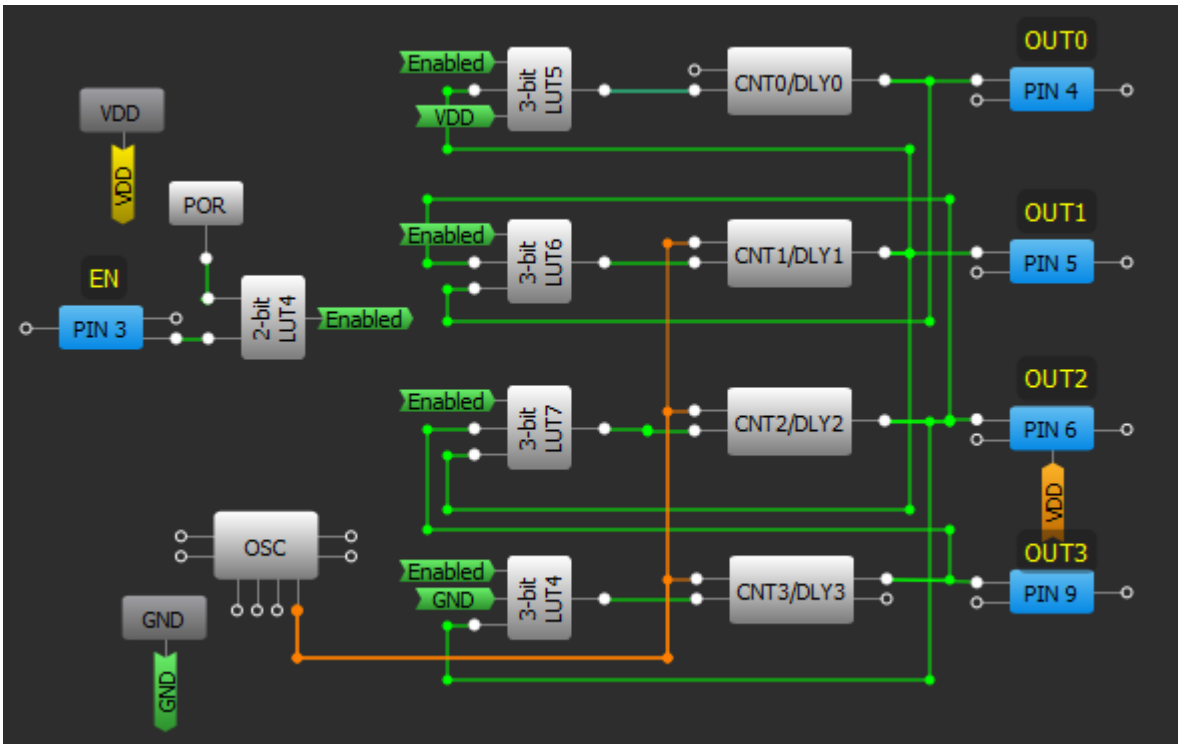

Figure 3. Power up and down sequencer block diagram

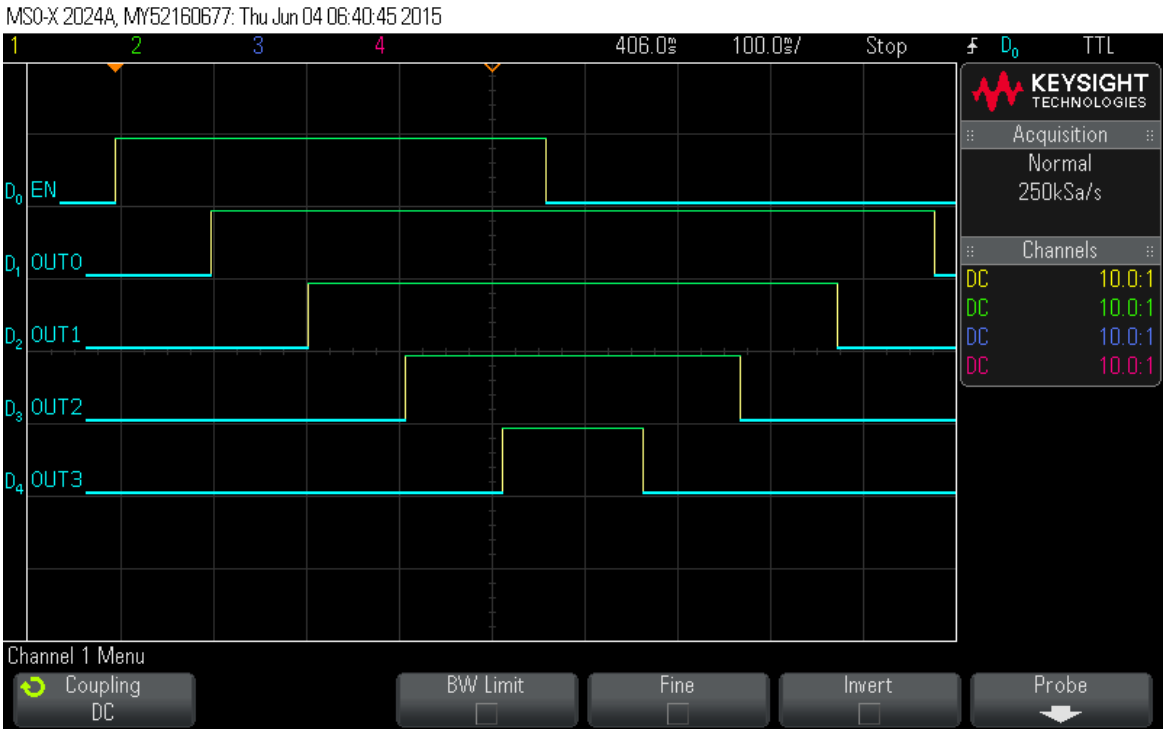

Figure 4. Power sequence up and down waveform

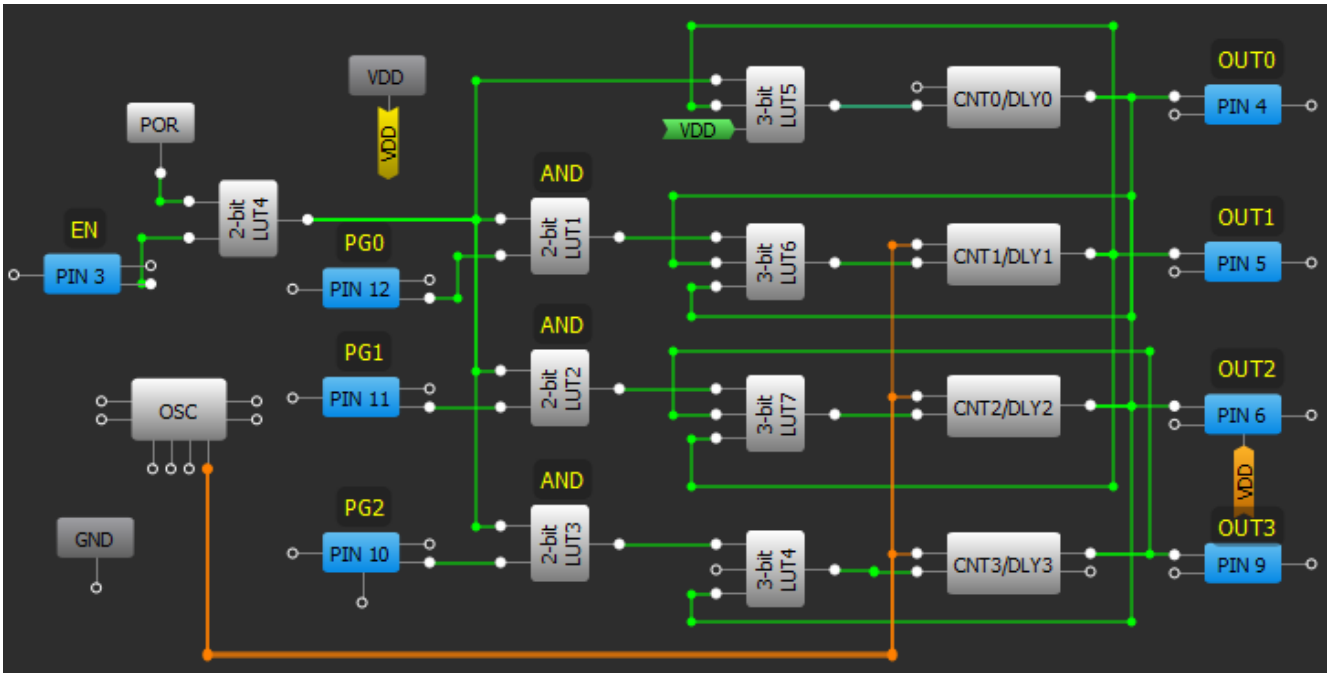

Figure 5. Power up and down sequencer with PG input block diagram

Conclusion

With programmable mixed-signal ASICs technologies, programming a 4-channel sequencer is only the beginning. GreenPAK4 based programmable mixed-signal ASICs have the ability to not only sequence, monitor, and supervise rails but also daisy chain to each other to multiply the number of rails controlled.

Appendix

Table one shows the look up table used in the power up and down sequencer. IN2 is from the sequencer enable, IN1 is from the output of the next rail, IN0 is from the output of the previous rail.

3-bit LUT6			
IN2	IN1	IN0	OUT
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Table 1. Power up and down sequencer LUT

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