Linear to Exponential Converter
SLG46140

This application note shows the implementation of a linear to exponential converter circuit using the SLG46140 GreenPAK device. The circuit uses the SLG46140 ADC to read a linear input voltage and, the device PWM generators with a low-pass filter to generate an approximation of an exponential output function. This application note comes complete with design files which can be found in the References section

Contents

1. Reference

For related documents and software, please visit:

https://www.renesas.com/eu/en/products/programmable-mixed-signal-asic-ip-products/greenpak-programmable-mixed-signal-products

Download our free GreenPAK Designer software [1] to open the .gp files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Find out more in a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the GreenPAK IC.

[1] GreenPAK Designer Software, Software Download and User Guide

[2] Linear to Exponential Converter.gp, GreenPAK Design File

[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage

[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage

2. GreenPAK Circuit Design

The GreenPAK design using the SLG46140 device, and the low-pass filter circuit is shown in Figure 1. The low-pass filter is a second-order RC ladder and is used to convert a PWM output signal through PIN 9 into an analog voltage. The linear input voltage is connected to PIN 6.

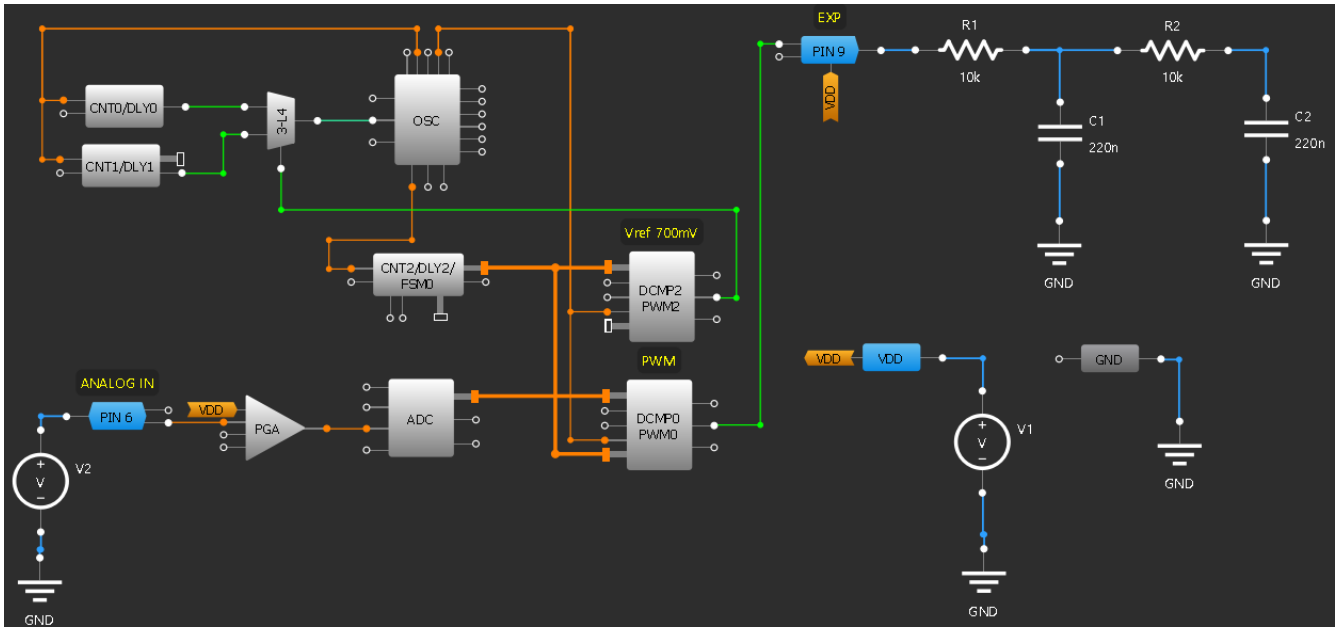

Figure 1. GreenPAK internal design with external circuit connections

The circuit idea is to generate an output voltage as an exponential function of the input voltage. The exponential function is approximated by a dual slope approximation, where the input voltage ranging from 0 to V_{ref} = *700mV* have an output slope much lower than the input voltages ranging from *700mV to 1V*. This relationship between the input and output voltages can be seen in the measurements shown in Figure 2.

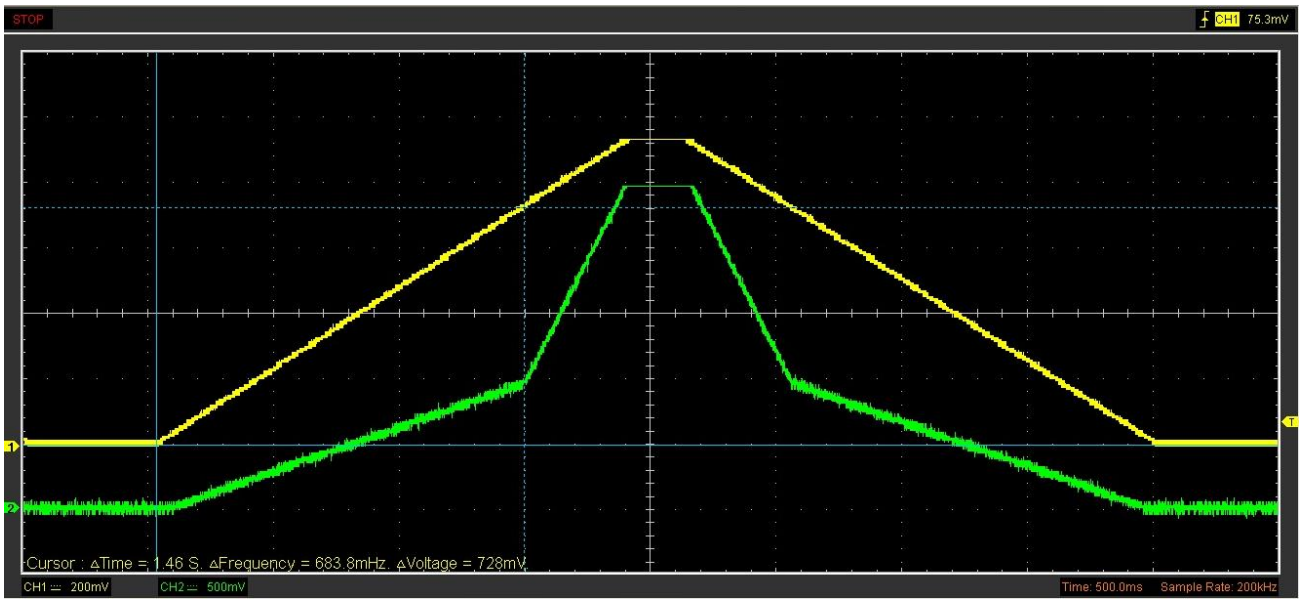

Figure 2. Linear input voltage trace (Channel 1 in yellow) versus exponential output trace (Channel 2 in green)

Figure 3 shows circuit operation timing diagrams. The following description of the circuit operation will explain the timing diagrams.

To create a function with two different slopes in the output, the generated PWM period was split into two timing windows. The 1st time window corresponds to 70% of the entire PWM period. This window is used to generate PWM output for input voltages between *700mV to 1V*. The 2nd time window is used to generate PWM output for input voltages between *0V to 700mV*. This window represents 30% of the entire PWM period.

The split in the PWM period makes the input voltages up to *700mV* generate an output voltage up to 30% of the full-scale power supply (the output analog voltage will be the PWM width, in percentage, multiplied by the digital output high-level voltage). In contrast, the input voltages between *700mV* and *1V* (a smaller range of *300mV*) can generate an output voltage from 30% to 100%. This different PWM behavior can be seen in the difference between the curves of **PWM_EXP** (exponential PWM) and **PWM_LIN** (linear PWM) in Figure 3. The PWM width is defined by analog input voltage shown in blue in Figure 3.

The PWM output is generated by the digital comparator (PWM generator) DCMP0/PWM0 with the CNT2/DLY2/FSM0. The CNT2/DLY2/FSM0 is configured as a down counter with a reset value of 255. When the counter reaches zero, it resets to 255. The DCMP0/PWM0 compares the 8-bit ADC digital output with the CNT2 counter value. While the ADC output is lower than the CNT2 counter value, the output is at a low level. When the counter value goes below the ADC value, the output raises to a high level. When the counter CTN2 resets the PWM, the output returns to the low level. This operation makes the CNT2 counter count from 255 till 0 and the time taken to count is the PWM period output. The PWM width is then defined by the ADC output reading.

If the clock supplied to the counter CNT2 was fixed, the function relationship between the analog input, the ADC reading, and the PWM width would be linear. This behavior can be seen in Figure 3 by observing the green curve (Current counter with constant clock) and in the **PWM_LIN** curve. When the green curve crosses the blue curve (the ADC reading output) the PWM signal raises.

However, to create the exponential function output, the circuit does not apply a constant clock frequency to the CNT2 counter. The applied clock frequency to CNT2 is defined by the digital comparator DCMP2/PWM2. This comparator compares the CNT2 counter output with a value fixed in a register, in this case, 179. While the CNT2 counter value is higher than 179, the DCMP2/PWM2 output is high, and the MUX created with LUT 3-L4 outputs the clock frequency from CNT1/DLY1 counter. The CNT1/DLY1 counter divides the oscillator (OSC) clock frequency by 55 (counter data + 1). When the CNT2 counter value is lower than 179, the DCMP2/PWM2 output falls to a low level and the MUX outputs the clock frequency from CNT0/DLY0 counter. The counter CNT0/DLY0 then divides the oscillator (OSC) clock frequency by 10 (counter data + 1). This difference in clock supply for the CNT2 counter makes the period for input voltages between *700mV* to *1V*, higher than the period for the input voltages below *700mV*. The total PWM period is given by the sum of these two periods. The operation of these different clock supplies and, the PWM behavior are seen in Figure 3 with the red curve (current counter with change clock) and the PWM_EXP.

The lower clock frequency for CTN2 counter values higher than 179 allows wider PWM signals, generating an analog input/output function with a higher slope. The higher clock frequency applied to the CNT2 counter for values lower than 179 generates narrow PWM signals, and then input/output functions with a lower slope. The value 179 corresponds to the ADC reading for the 700mV voltage, working as the reference input point where the output curve should change its slope. This change in the slope for input voltages higher than 700mV is visible in Figure 2

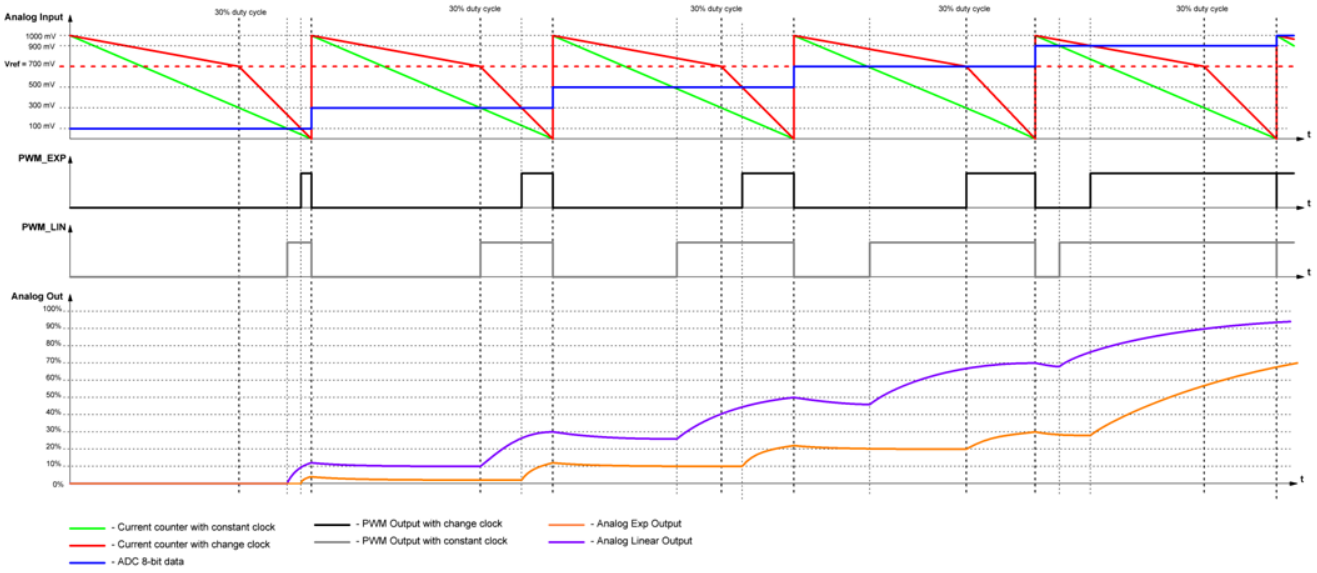

Figure 3. Linear to exponential converter timing diagram

3. Test Results

A prototype of the circuit in Figure 1 was implemented and tested with the support of the GreenPAK Advanced Development Board. A circuit simulation using a staircase input voltage was executed too. The circuit simulation with the staircase input voltage and the respective output voltage is shown in Figure 4. A similar staircase input (the simulated staircase has a narrow width, to reduce the simulation time) was applied in the prototype circuit. The prototype input voltage and the filtered exponential output voltage are shown in Figure 5.

In Table 1 shows voltage comparison between the simulated circuit and the prototype circuits for each input voltage. The power supply voltage is 3.3 V for both.

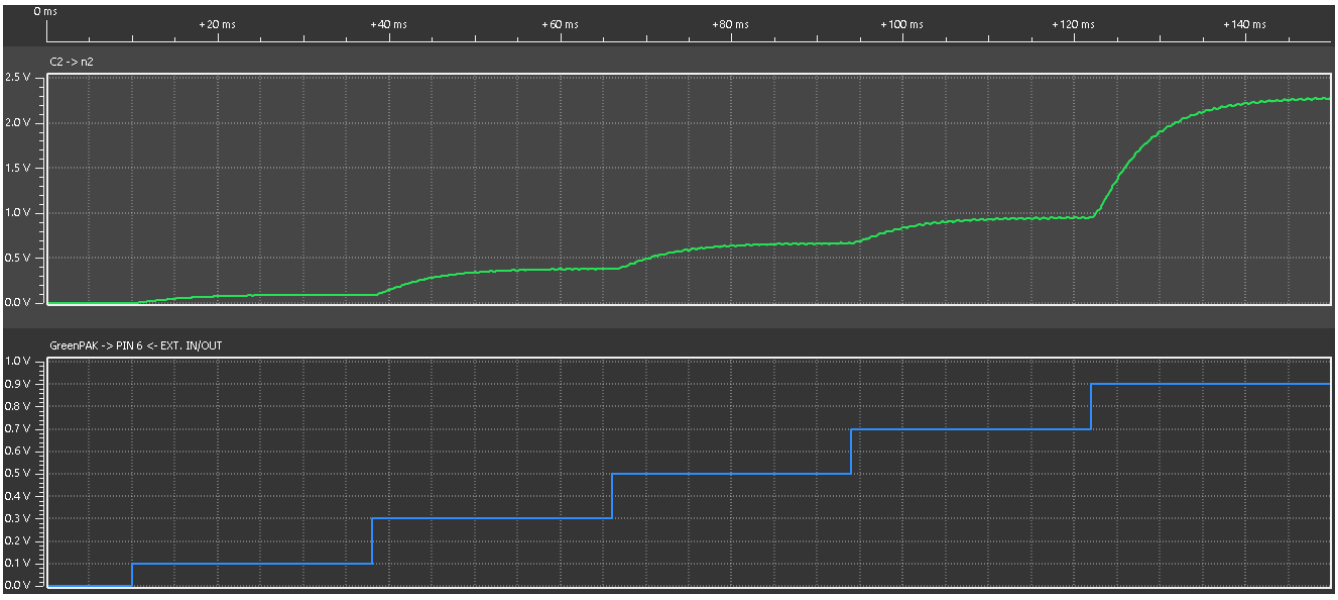

Figure 4. Input staircase voltage in blue (bottom) and filtered exponential output in green (top)

Table 1: Output voltage comparison between simulated circuit and prototype

Input (mV)	Simulation (mV)	Simulation (% output)	Prototype (mV)	Prototype (% output)	Simulation – Prototype (mV)	Simulation – Prototype (%)
100	93	2.82	105	3.18	+14	-0.36
300	382	11.57	375	11.36	+7	+0.21
500	666	20.18	645	19.54	+21	+0.64
700	930	28.18	951	28.81	-21	-0.63
900	2227	67.48	2275	68.94	-48	-1.46

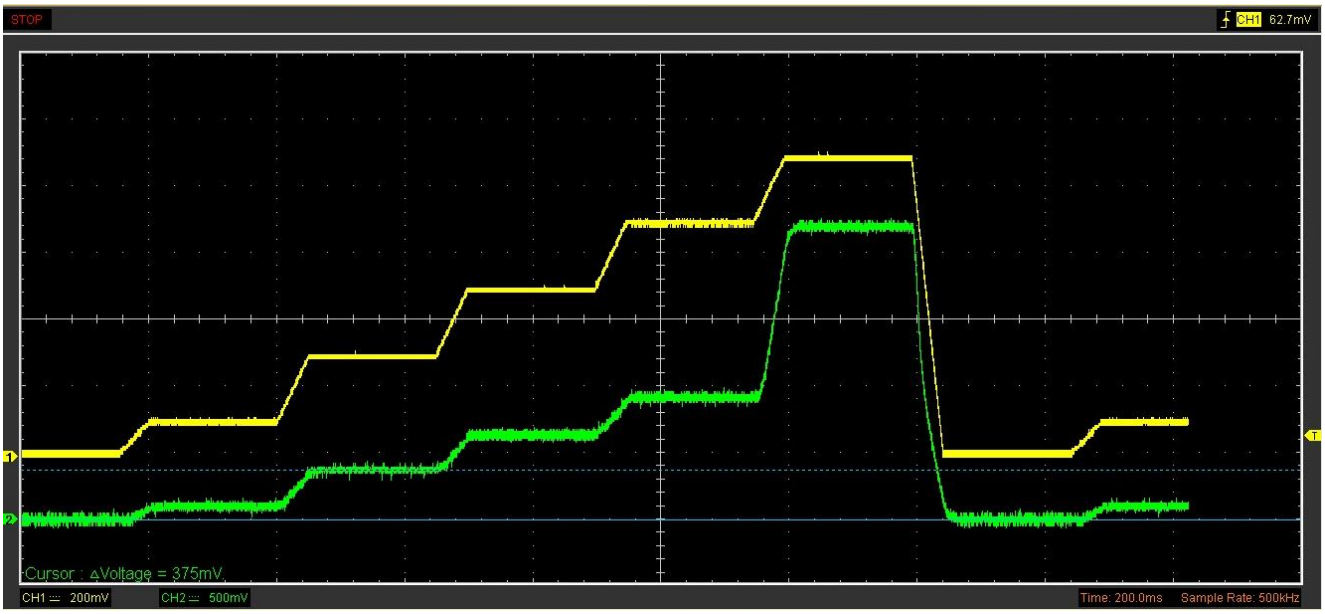

Figure 5. Input staircase voltage in yellow (Channel 1) and filtered exponential output in green (Channel 2)

Figure 6 shows the output of the circuit simulation using an input voltage curve like the input voltage curve used in Figure 2. The input curve in Figure 6 has a narrow waveform period just to reduce the software simulation time. The two different slopes are clearly observed in Figure 6 as well.

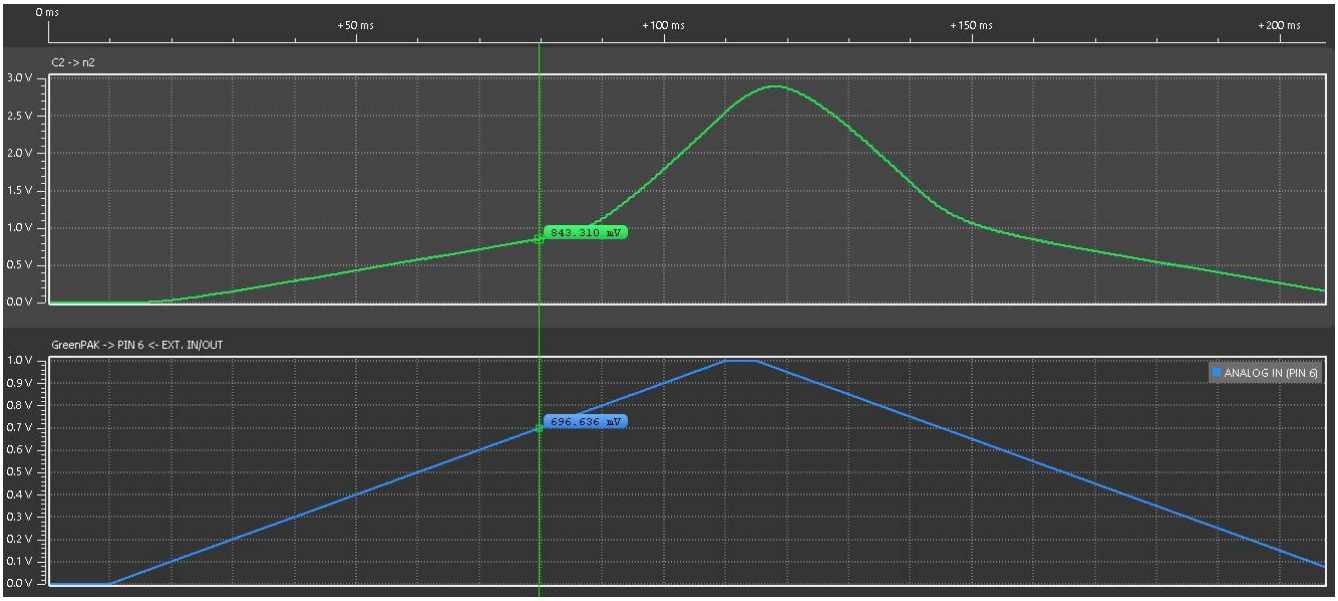

Figure 6. Circuit simulation showing the exponential output (top curve in green) as response to the trapezoidal input voltage (bottom curve in blue)

4. Conclusion

This application note showed the implementation of a linear to exponential converter using the SLG46140 device. The linear input voltage was read by the internal ADC and then converted into an unusual PWM output. This unusual PWM behavior (changing the input clock frequency in all periods) is a good example of the GreenPAK flexibility.

5. Revision History

Revision	Date	Description
1.00	June 02,2015	Initial release (SLG46400)
2.00	Sep 22, 2022	Application note review for a new device (SLG46140).

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