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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SY*-A026A/E	Rev.	1.00
Title	Unexpected GLCDC interrupt generated in S7G2 and S5D9 after the GLCDC starts		Information Category	Technical Notification		
Applicable Product	Renesas Synergy™ S7 Series S7G2, S5 Series S5D9	Lot No. All lots	Reference Document	S7G2 User's Manual: Microcontrollers, Rev.1.20 S5D9 User's Manual: Microcontrollers, Rev.1.00		

Renesas added a restriction to the GLCDC module of the S7G2 and S5D9 because of an unexpected GLCDC interrupt that is generated after the GLCDC is started.

1. Revised information about the System Control Block State Detection Control Register (SYSCNT_DTCEN) of the GLCDC in S7G2 and S5D9.

[Before]

Bit	Symbol	Bit name	Description	R/W
b0	VPOSDTC	Specified Line Detection Control	0: Disable detection of specified line 1: Enable detection of specified line.	R/W
b1	L1UNDFDTC	Graphics 1 Underflow Detection Control	0: Disable detection of graphics 1 underflow 1: Enable detection of graphics 1 underflow.	R/W
b2	L2UNDFDTC	Graphics 2 Underflow Detection Control	0: Disable detection of graphics 2 underflow 1: Enable detection of graphics 2 underflow.	R/W
b31 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

[After]

Bit	Symbol	Bit name	Description	R/W
b0	VPOSDTC	Specified Line Detection Control	0: Disable detection of specified line 1: Enable detection of specified line.*1	R/W
b1	L1UNDFDTC	Graphics 1 Underflow Detection Control	0: Disable detection of graphics 1 underflow 1: Enable detection of graphics 1 underflow.*2	R/W
b2	L2UNDFDTC	Graphics 2 Underflow Detection Control	0: Disable detection of graphics 2 underflow 1: Enable detection of graphics 2 underflow.*2	R/W
b31 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1: Set the VPOSDTC bit to 1 after setting the BG_EN.EN bit to 1.

Note 2: When the LnUNDFDTC (n = 1, 2) bit is set to 1 and when the BG_SYNC.VP[3:0] bits are set to a value greater than 5h, an unexpected GLCDC_LnUNDF (n = 1, 2) interrupt is generated after the GLCDC starts. Therefore, set the SYSCNT_STCLR.LnUNDFCLR (n = 1, 2) bit to 1, then set the SYSCNT_STMON.LnUNDF (n = 1, 2) bit to 0 to clear the unexpected GLCDC_LnUNDF (n = 1, 2) interrupt.