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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SY*-A003A/E	Rev.	1.00
Title	Restriction and revised information of S3 Series from the previous Rev.0.85		Information Category	Technical Notification		
Applicable Product	Synergy S3 Series S3A7	Lot No. All lots	Reference Document	S3A7 User's Manual: Microcontrollers, Rev.1.00		

1. Restriction about CTSU

• Corrected CTSU channel in Table 1.14, Function comparison as follows:

[Before]

Parts number	R7FS3A77C2A 01CLK	R7FS3A77C3A 01CFB	R7FS3A77C2A 01CBJ	R7FS3A77C3A 01CFP	R7FS3A77C2A 01CLJ	R7FS3A77C3A 01CFM/ R7FS3A77C3A 01CNB
CTSU	35		30		17	

[After]

Parts number	R7FS3A77C2A 01CLK	R7FS3A77C3A 01CFB	R7FS3A77C2A 01CBJ	R7FS3A77C3A 01CFP	R7FS3A77C2A 01CLJ	R7FS3A77C3A 01CFM/ R7FS3A77C3A 01CNB
CTSU	31		26		14	

• Corrected CTSU pins in section 1.5, Pin Functions as follows:

[Before]

Function	Signal	I/O	Description
CTSU	TS00, TS01, TS03 to TS35	Input	Capacitive touch detection pins (touch pins).

[After]

Function	Signal	I/O	Description
CTSU	TS00, TS01, TS03 to TS22, TS26 to TS27, TS29 to TS35	Input	Capacitive touch detection pins (touch pins).

• Corrected CTSU pins in section 1.7, Pin Lists as follows:

[Before]

Pin number							I/O ports	Analogs			HMI	
LGA145	LQFP144	BGA121	LQFP100	LGA100	LQFP64	QFN64		ADC14	DAC12, OPAMP	ACMPHS, ACMPLP	CTSU	Interrupt
K7	133	H7	93	H7			P007	AN007	AMP3O	IVCMP4/ IVCMP1	TS28	
K9	136	J8	96	J8	60	60	P004	AN004	AMP2O	IVREF0	TS25	IRQ9
K10	137	K8	97	H8	61	61	P003	AN003	AMP1O	IVCMP0	TS24	
M10	138	J9	98	K8	62	62	P002	AN002	AMP0O	IVREF2/ IVCMP2	TS23	IRQ8

[After]

Pin number							I/O ports	Analogs			HMI	
LGA145	LQFP144	BGA121	LQFP100	LGA100	LQFP64	QFN64		ADC14	DAC12, OPAMP	ACMPHS, ACMPLP	CTSU	Interrupt
K7	133	H7	93	H7			P007	AN007	AMP3O	IVCMP4/ IVCMP1	—	
K9	136	J8	96	J8	60	60	P004	AN004	AMP2O	IVREF0	—	IRQ9
K10	137	K8	97	H8	61	61	P003	AN003	AMP1O	IVCMP0	—	
M10	138	J9	98	K8	62	62	P002	AN002	AMP0O	IVREF2/ IVCMP2	—	IRQ8

• Corrected Table 20.4, Register settings for input/output pin function (PORT0) as follows:

[Before]

PSEL[4:0] bits settings	Function	Pin							
		P000	P001	P002	P003	P004	P005	P006	P007
01100b	CTSU	TS21	TS22	TS23	TS24	TS25	TS26	TS27	TS28

[After]

PSEL[4:0] bits settings	Function	Pin							
		P000	P001	P002	P003	P004	P005	P006	P007
01100b	CTSU	TS21	TS22	—	—	—	TS26	TS27	—

• Corrected Table 45.1, CTSU specifications as follows:

[Before]

Parameter		Description
Pins	Electrostatic capacitance measurement	35 channels (TS00, TS01, TS03 to TS35)

[After]

Parameter		Description
Pins	Electrostatic capacitance measurement	31 channels (TS00, TS01, TS03 to TS22, TS26 to TS27, TS29 to TS35)

• Corrected Table 45.2, CTSU pin configuration as follows:

[Before]

Pin name	I/O	Function
TS00, TS01, TS03 to TS35	Input	Electrostatic capacitive measurement pins (touch pins)

[After]

Pin name	I/O	Function
TS00, TS01, TS03 to TS22, TS26 to TS27, TS29 to TS35	Input	Electrostatic capacitive measurement pins (touch pins)

2. Restriction about PLL output frequency division ratio

• Modified Table 9.1, Clock Generation Circuit specifications (clock source).

[Before]

Clock source	Item	Specification
PLL circuit	input clock source	MOSC
	Input frequency	4 MHz to 12.5 MHz
	Frequency multiplication ratio	Selectable from 8 to 31 (1 step) (multiplication frequency is up to 64 MHz)
	Output pulse frequency division ratio	Selectable from 1, 2, and 4
	PLL output frequency	24MHz to 64MHz(Minimum PLL output frequency is 48 MHz when output frequency division ratio is 1)

[After]

Clock source	Item	Specification
PLL circuit	input clock source	MOSC
	Input frequency	4 MHz to 12.5 MHz
	Frequency multiplication ratio	Selectable from 8 to 31 (1 step) (multiplication frequency is up to 64 MHz)
	Output pulse frequency division ratio	Selectable from 1, 2, and 4
	PLL output frequency	48MHz to 64MHz (output frequency division ratio:1) 24MHz to 64MHz (output frequency division ratio:2) 24MHz to 32MHz (output frequency division ratio:4)

3. Restriction about ELCON bit setting timing

• Modified section 19.4.3, Module Stop Function Setting.

[Before]

ELC operation can be disabled or enabled using Module Stop Control Register C (MSTPCRC). The ELC is initially stopped after reset. Releasing the module-stop state enables access to the registers. For more information, see Table 19.3 and section 11, Low-Power Modes.

[After]

The Module Stop Control Register C (MSTPCRC) can enable or disable ELC operation. After a reset, the ELC is disabled. Releasing the module-stop state enables access to the registers. For more information, see Table 19.3 and section 11, Low-Power Modes. The ELCON bit must be set to 0 before ELC operation is disabled using the Module Stop Control Register.

Information: Event Link Controller Register (ELCR)

Bit	Symbol	Bit name	Description	R/W
b7	ELCON	All Event Link Enable	0: Disable ELC function 1: Enable ELC function.	R/W

4. Restriction about cancelling Software Standby mode to use A/D conversion

• Added section 39.8.14, Notes on Canceling Software Standby Mode to section 39.8, Usage Notes.

[Before]

No description.

[After]

39.8.14 Notes on Canceling Software Standby Mode

After the transition from Software Standby mode to normal mode, wait 1 µs before starting A/D conversion.

5. Restriction about the FSPR bit in the AWSC Register.

• Updated FSPR bit in section 7.2.4, Access Window Setting Control Register (AWSC).

[Before]

Bit	Symbol	Bit name	Description	R/W
b14	FSPR	Protection of Access Window and Startup Area Select Function	Write/Erase Protection of Access Window, Start-Up Area Select Flag (BTFLG) and Temporary Boot Swap Control. 0: It is invalid to execute the configuration setting command for programming the access window (FAWE10-00, FAWS10-00) and the start-up area select flag (BTFLG). It is invalid to execute the configuration clear command. It is invalid to write the start-up area select bits (TMSPMD, TMBTSEL) in the FSSET register. 1: It is valid to execute the configuration setting command for programming the access window (FAWE10-00, FAWS10-00) and the start-up area select flag (BTFLG). It is valid to execute the configuration clear command. It is valid to write the start-up area select bits (SAS[1:0] in the FISR register.	R

[After]

Bit	Symbol	Bit name	Description	R/W
b14	FSPR	Protection of Access Window and Startup Area Select Function	Write/Erase Protection of Access Window, Start-Up Area Select Flag (BTFLG) and Temporary Boot Swap Control. After this bit is set to 0, it cannot be changed to 1. 0: It is invalid to execute the configuration setting command for programming the access window (FAWE[10:0], FAWS[10:0]) and the start-up area select flag (BTFLG). It is invalid to write the start-up area select bits (TMSPMD, TMBTSEL) in the FSSET register. 1: It is valid to execute the configuration setting command for programming the access window (FAWE[10:0], FAWS[10:0]) and the start-up area select flag (BTFLG). It is valid to write the start-up area select bits (SAS[1:0] in the FISR register.	R

6. Updated section 51, Electrical Characteristics

• Corrected Table 51.22, Clock timing as follows:

[Before]

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
HOCO clock oscillation frequency	f_{HOCO24}	23.64	24	24.36	MHz	Ta = –40 to –20℃ 1.8 ≤ VCC ≤ 5.5
		22.68	24	25.32		Ta = –40 to –20℃ 1.6 ≤ VCC < 1.8
		23.76	24	24.24		Ta = –20 to 85℃ 1.8 ≤ VCC ≤ 5.5
		22.80	24	25.20		Ta = –20 to 85℃ 1.6 ≤ VCC < 1.8
		23.52	24	24.48		Ta = 85 to 105℃ 2.4 ≤ VCC ≤ 5.5
	f_{HOCO64}	63.04	64	64.96		Ta = –40 to –20℃ 2.4 ≤ VCC ≤ 5.5
		63.36	64	64.64		Ta = –40 to –20℃ 2.4 ≤ VCC ≤ 5.5
		62.72	64	65.28		Ta = –40 to –20℃ 2.4 ≤ VCC ≤ 5.5

[After]

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
HOCO clock oscillation frequency	f_{HOCO24}	23.64	24	24.36	MHz	Ta = –40 to –20℃ 1.8 ≤ VCC ≤ 5.5
		22.68	24	25.32		Ta = –40 to 85℃ 1.6 ≤ VCC < 1.8
		23.76	24	24.24		Ta = –20 to 85℃ 1.8 ≤ VCC ≤ 5.5
		23.52	24	24.48		Ta = 85 to 105℃ 2.4 ≤ VCC ≤ 5.5
	f_{HOCO64}	63.04	64	64.96		Ta = –40 to –20℃ 2.4 ≤ VCC ≤ 5.5
		63.36	64	64.64		Ta = –20 to 85℃ 2.4 ≤ VCC ≤ 5.5
		62.72	64	65.28		Ta = 85 to 105℃ 2.4 ≤ VCC ≤ 5.5

• Corrected Table 51.35, I/O Ports, POEG, GPT, AGT, KINT, and ADC14 trigger timing as follows:

[Before]

Item		Symbol	Min	Max	Unit
I/O Ports	Input data pulse width	t_{PRW}	1.5	—	t_{PCYC}

[After]

Item		Symbol	Min	Max	Unit
I/O Ports	Input data pulse width	t_{PRW}	1.5	—	t_{PCYC}
	Input/output data cycle (P002,P003,P004,P007)	t_{POcyc}	10	—	μs

• Corrected Table 51.72, ACMPHS characteristics as follows:

[Before]

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input voltage range	V_{ICMP}	0	—	AVCC0	V	—

[After]

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input voltage range	V_{ICMP}	0	—	AVCC0	V	—
Input signal cycle	t_{PCMP}	10	—	—	μs	—

• Corrected Table 51.55, 14-Bit A/D converter channel classification as follows:

[Before]

Classification	Channel	Conditions	Remarks
High-precision channel	AN000 to AN015	AVCC0 = 1.6 to 5.5 V	AN010 to AN015 are multiplied with VREFH, VREFL, VREFH0, VREFL0, or DAC12 outputs since they are grouped in Normal-precision channel.
Normal-precision channel	AN016 to AN027		

[After]

Classification	Channel	Conditions	Remarks
High-precision channel	AN000 to AN015	AVCC0 = 1.6 to 5.5 V	Pins AN000 to AN015 cannot be used as general I/O, IRQ8, IRQ9 inputs, and TS transmission, when the A/D converter is in use.
Normal-precision channel	AN016 to AN027		

7. Other revised items (from Rev.0.85 to Rev.1.00)

• Revised items are shown in the table below. See Rev.1.0 of the User Manual for detail.

Chapter	Points in Rev.1.0
2. CPU	Updated the component name for address E00F F000h and E00F F004h in Table 2.7, ROM entries of CoreSight ROM Table
7. Option-Setting Memory	Updated the Note in section 7.2.2, Option Function Select Register (OFS1)
11. Low Power Mode	Added Note 12. to Table 11.2, Operating conditions of each low power mode
	Added Note 3. to Table 11.3, Available interrupt sources to transition to Normal mode from Snooze mode and Software Standby mode
	Updated description in section 11.2.9, Snooze End Control Register (SNZEDCR)
	Added section 11.9.12, Conditions of CTSU in Snooze Mode
12. Battery Backup Function	Updated the access permission for bit VBTRVLD in section 12.2.3, VBATT Status Register (VBTSR)
	Updated bit [0] VWEN in section 12.2.7, VBATT Wakeup Control Register (VBTWCTLR)
	Updated description in section 12.2.12, VBATT Output Control Register (VBTOCTLR)
	Updated bit names for bits [0], [1], and [2] in section 12.2.15, VBATT Wakeup Trigger Source Flag Register (VBTWFR)
14. Interrupt Controller Unit (ICU)	Added Note 3. and updated Table 14.4, Event table
15. Buses	Changed address output pins from A23 to A16 in Table 15.4, External pin configurations, and throughout the document
	Updated section 15.3.6, CSn Wait Control Register 2 (CSnWCR2) (n = 0 to 3)
	Updated section 15.7, Notice to use Flash Cache
18. Data Transfer Controller (DTC)	Updated address range in section 18.2.8, DTC Vector Base Register (DTCVBR)
20. I/O Ports	Added explanation for P402, P403, and P404 and modified description for VBTICTLR in section 20.5.5 I/O Buffer Specification
	Updated Table 20.4, Register settings for input/output pin function (PORT0) for CTSU in P002 to P004 and P007
	Updated Table 20.4, Register settings for input/output pin function (PORT0) for the ASEL bit in P014 and P015
	Updated Table 20.5, Register settings for input/output pin function (PORT1) (1) for AGT in P100 and P101
	Updated Table 20.7, Register settings for input/output pin function (PORT2) (1) for AGT/CTSU in P204
	Updated Table 20.8, Register settings for input/output pin function (PORT2) (2) for AGT in P212
	Updated Table 20.10, Register settings for input/output pin function (PORT4) (1) for 64-pin product in P406
	Updated Table 20.10, Register settings for input/output pin function (PORT4) (1) for DSCR bit in P400
21. Key Interrupt Function (KINT)	Updated section 21.4, Usage Note
25. Realtime Clock (RTC)	Updated section 25.2.20, Frequency Register (RFRH/RFRL)
28. USB 2.0 Full-Speed Module (USBFS)	Added Table 28.6, Endian operation in 8-bit access in section 28.2.4, CFIFO Port Register (CFIFO/CFIFOL), D0FIFO Port Register (D0FIFO/D0FIFOL), D1FIFO Port Register (D1FIFO/D1FIFOL)
	Updated Figure 28.3, Example of power supply connection when the USB LDO regulator is used (BC used) and Figure 28.4, Example of power supply connection when the USB LDO regulator is used (BC not used)

Chapter	Points in Rev.1.0
29. Serial Communication Interface (SCI)	Updated the initial value and access permission for bit [1] in section 29.2.14, Serial Status Register for Non-Smart Card Interface and FIFO Mode (SSR_FIFO) (SCMR.SMIF = 0 and FCR.FM = 1)
	Updated the initial value and access permission for bit [6] in section 29.2.31, Serial Port Register (SPTR)
34. Quad Serial Peripheral Interface (QSPI)	Updated Table 34.3, Relationship among SFMDV[4:0] bits, cycle multiplier, and serial clock frequencies
35. Cyclic Redundancy Check (CRC) Calculator	Updated description for CRCSA [13:0] in section 35.2.5, Snoop Address Register (CRCSAR)
41. Temperature Sensor (TSN)	Deleted the TBD from section 41.3.1, Preparation for Using Temperature Sensor
45. Capacitive Touch Sensing Unit (CTSU)	Updated descriptions in section 45.2.5, CTSU Measurement Channel Register 0 (CTSUMCH0)
	Updated descriptions in section 45.2.6, CTSU Measurement Channel Register 1 (CTSUMCH1)
	Updated descriptions and added Note 1.in section 45.2.9, CTSU Channel Enable Control Register 2 (CTSUCHAC2)
	Updated descriptions and added Note 1.in section 45.2.10, CTSU Channel Enable Control Register 3 (CTSUCHAC3)
	Updated descriptions and added Note 1.in section 45.2.14, CTSU Channel Transmit/Receive Control Register 2 (CTSUCHTRC2)
	Updated descriptions and added Note 1.in section 45.2.15, CTSU Channel Transmit/Receive Control Register 3 (CTSUCHTRC3)
	Updated bit [15] CTSUICOMP in section 45.2.24, CTSU Error Status Register (CTSUERRS)
	Updated section 45.4.5, TSCAP Pin
51. Electrical Characteristics	Added section 51.17, Joint European Test Action Group (JTAG) and section 51.17.1, Serial Wire Debug (SWD) in section 51, Electrical Characteristics
	Updated input voltage in Table 51.1, Absolute maximum ratings
	Added section 51.2.5, I/O Pin Output Characteristics of Low Drive Capacity
	Updated Table 51.6, I/O I_{OH}, I_{OL} in section 51.2.3, I/O I_{OH}, I_{OL} to change from normal drive to low drive
	Changed Note 6 to Note 5. in Table 51.11, Operating and standby current (1)
	Updated the conditions in Table 51.13, Operating and standby current (3)
	Updated Note 2. in Table 51.17, Operation frequency value in high-speed operating mode.
	Updated Note 2. in Table 51.18, Operation frequency value in middle-speed mode
	Removed the 2nd note from Table 51.19, Operation frequency value in low-speed Mode
	Updated Note 2. in Table 51.20, Operation frequency value in low-voltage mode
	Updated Table 51.22, Clock timing
	Removed the 2nd note from Table 51.37, SCI timing (1)
	Updated the conditions in Table 51.38, SCI timing (2)
	Updated Figure 51.59, SPI timing (master, CPHA = 0) (bit rate: PCLKA division ratio is set to 1/2)
	Added the conditions in Table 51.42, IIC timing
	Updated Figure 51.68, SSI data transmit/receive timing (SSICR.SCKP = 0)
	Updated the Quantization error in the following tables: - Table 51.48, A/D conversion characteristics (1) in high-speed mode - Table 51.49, A/D conversion characteristics (2) in high-speed mode - Table 51.50, A/D conversion characteristics (3) in high-speed mode - Table 51.51, A/D conversion characteristics (4) in low power mode - Table 51.52, A/D conversion characteristics (5) in low power mode
	Updated Table 51.64, Battery Backup Function Characteristics
	Deleted VLCD = 0Dh to 13h in Table 51.70, Internal voltage boosting method LCD characteristics
	Updated the response time in Table 51.72, ACMPHS characteristics
	Added the temperature in Table 51.77, Code flash characteristics (3)
	Added the temperature in Table 51.80, Data flash characteristics (3)
All	Deleted # from pin names