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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A118A/E	Rev.	1.00
Title	Usage Notes on A/D Conversion Delaying Function of MTU2		Information Category	Technical Notification		
Applicable Product	RX62N/621 Group RX63N/631 Group, RX630 Group RX210 Group, RX220 Group RX21A Group, RX111 Group RX113 Group	Lot No. All lots	Reference Document	See below.		

Usage notes on the multi-function timer pulse unit 2 (MTU2, MTU2a) for the products listed below are as follows.

According to this update, relevant manuals are revised. The details of the corrections are described as follows based on the user's manual: hardware of the RX62N group and RX621 group.

See the section of Applicable Products and Relevant Documents in the last section for the corrections of the manuals in other groups.

[Notes]

1. A/D Converter Start Request Enabled Interval in A/D Conversion Delaying Function

- If the UT4AE or UT4BE bit in MTUn.TADCR is set to 1 in complementary PWM mode, A/D converter start requests are enabled during the MTUn.TCNT up-counting period. The A/D converter start request enabled interval is: 0 ≤ MTUn.TCNT ≤ TCDR - 1.
- If the DT4AE or DT4BE bit in MTUn.TADCR is set to 1 in complementary PWM mode, A/D converter start requests are enabled during the MTUn.TCNT down-counting period. The A/D converter start request enabled interval is: TCDR ≥ MTUn.TCNT ≥ 1.
- Clear the DT4AE and DT4BE bits in MTUn.TADCR to 0 when not in complementary PWM mode. Setting the UT4AE or UT4BE bit in MTUn.TADCR to 1 causes an A/D converter start request to be generated at a compare match between MTUn.TCNT and MTUn.TADCORA/MTUn.TADCORB, regardless of whether MTUn.TCNT is counting up or down (n = 4, 10).

2. Notes on A/D Converter Start Request Delaying Function in Complementary PWM Mode

- When MTUn.TADCOBRA/MTUn.TADCOBRB is set to 0 and the UT4AE or UT4BE bit in MTUn.TADCR is set to 1, and the result is transferred to the buffer when counting by MTUn.TCNT reaches its trough, an A/D converter start request is not generated during the up-counting period immediately following the transfer (Figure 2.1).
- When the same value as that of TCDR is set to MTUn.TADCOBRA/MTUn.TADCOBRB and the DT4AE or DT4BE bit in MTUn.TADCR is set to 1, and the result is transferred to the buffer when counting by MTUn.TCNT reaches its crest, an A/D converter start request is not generated during the down-counting period immediately following the transfer (Figure 2.2).

- When A/D converter start requests are linked to the interrupt skipping function, set MTUn.TADCORA or MTUn.TADCORB to meet the condition 2 ≤ MTUn.TADCORA or MTUn.TADCORB ≤ TCDR - 2 (n = 4, 10).

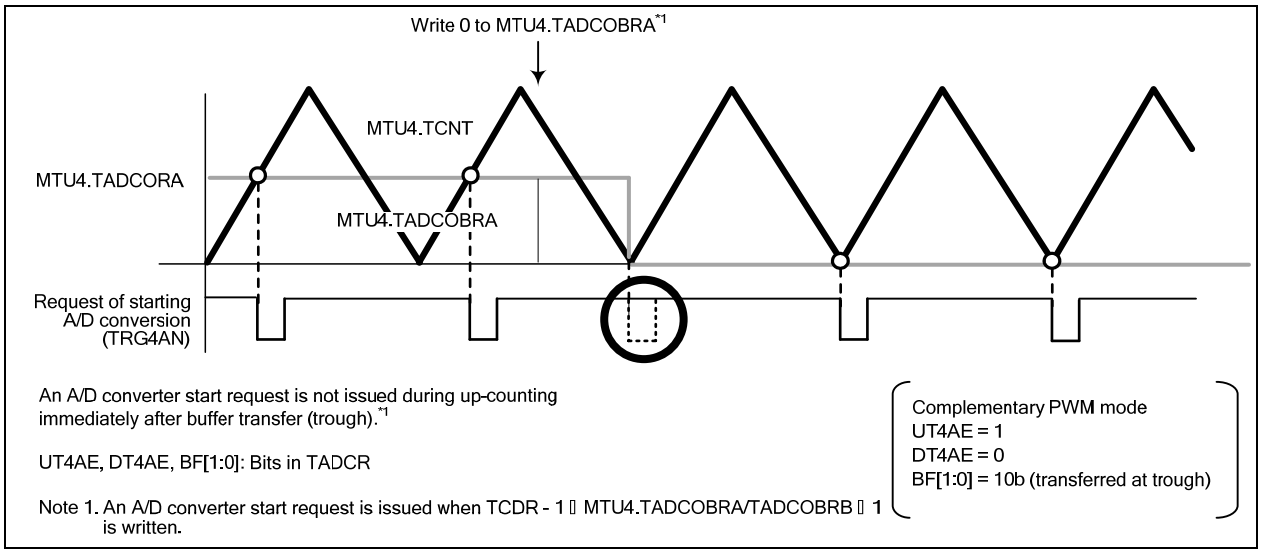

Figure 2.1 A/D Converter Start Request When 0 is Written to MTU4.TADCOBRA

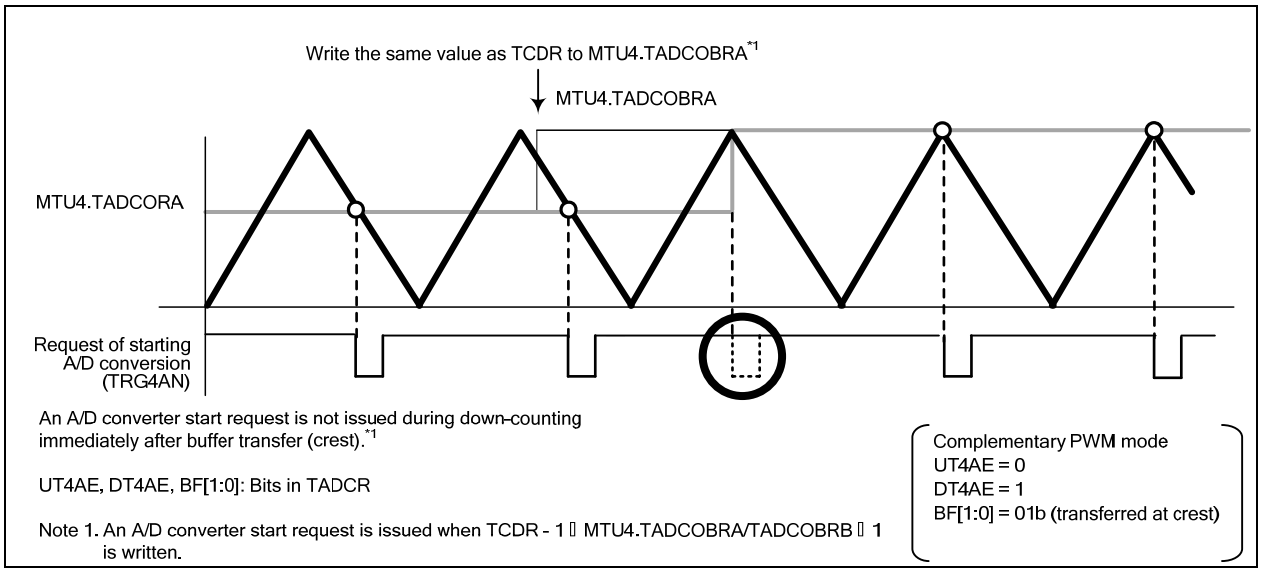

Figure 2.2 A/D Converter Start Request When the Same Value as TCDR is Written to MTU4.TADCOBRA

[Corrections in the Manual]

18.2.9 Timer A/D Converter Start Request Control Register (TADCR)

<Before correction (p. 909)>

Address: MTU4.TADCR 0008 8640h, MTU10.TADCR 0008 8A40h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BF[1:0]		—	—	—	—	—	—	UT4AE	DT4AE	UT4BE	DT4BE	ITA3AE	ITA4VE	ITB3AE	ITB4VE
Value after reset	0	0	0	0	0	0	0	0	0	0*	0	0*	0*	0*	0*	0*

Note: * Do not set bits 6, and 4 to 0 to 1 when complementary PWM mode is not selected.

Bit	Symbol	Bit Name	Description	R/W
b0	ITB4VE	TCIV4 Interrupt Skipping Link Enable	0: TCI4V interrupt skipping is not linked 1: TCI4V interrupt skipping is linked	R/W
b1	ITB3AE	TGIA3 Interrupt Skipping Link Enable	0: TGI3A interrupt skipping is not linked 1: TGI3A interrupt skipping is linked	R/W
b2	ITA4VE	TCIV4 Interrupt Skipping Link Enable	0: TCI4V interrupt skipping is not linked 1: TCI4V interrupt skipping is linked	R/W
b3	ITA3AE	TGIA3 Interrupt Skipping Link Enable	0: TGI3A interrupt skipping is not linked 1: TGI3A interrupt skipping is linked	R/W
b4	DT4BE	Down-Count TRG4BN Enable	0: A/D converter start requests (TRG4BN) disabled during MTU4.TCNT down-count operation 1: A/D converter start requests (TRG4BN) enabled during MTU4.TCNT down-count operation	R/W
b5	UT4BE	Up-Count TRG4BN Enable	0: A/D converter start requests (TRG4BN) disabled during MTU4.TCNT up-count operation 1: A/D converter start requests (TRG4BN) enabled during MTU4.TCNT up-count operation	R/W
b6	DT4AE	Down-Count TRG4AN Enable	0: A/D converter start requests (TRG4AN) disabled during MTU4.TCNT down-count operation 1: A/D converter start requests (TRG4AN) enabled during MTU4.TCNT down-count operation	R/W
b7	UT4AE	Up-Count TRG4AN Enable	0: A/D converter start requests (TRG4AN) disabled during MTU4.TCNT up-count operation 1: A/D converter up requests (TRG4AN) enabled during MTU4.TCNT down-count operation	R/W
b13 to b8	—	Reserved	These bits are always read as 0. The write value should be 0.	R/W
b15, b14	BF[1:0]	MTU4.TADCOBRA/B Transfer Timing Select	See Table 18.31 for details.	R/W

Note 1. Since channels 4 and 10 have the same functionality, the explanation here is only for unit 0.

Note 2. Access to TADCR in eight-bit units is prohibited. Always access this register in 16-bit units.

Note 3. While interrupt skipping is prohibited, i.e. while the T3AEN and T4VEN bits and the skipping count setting bits (T3ACOR and T4VCOR) in the timer interrupt skipping set register (TITCR) are set to "0", do not set up interlocking with interrupt skipping, i.e. set the ITA3AE, ITA4VE, ITB3AE, or ITB4VE bits in the timer A/D converter start request register (TADCR) to "0".

Note 4. Requests to start A/D converter are not issued if the setting for interlocking with interrupt skipping is made while interrupt skipping is prohibited.

<After correction>

Address: MTU4.TADCR 0008 8640h, MTU10.TADCR 0008 8A40h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b1
	BF[1:0]		—	—	—	—	—	—	UT4AE	DT4AE	UT4BE	DT4BE	ITA3AE	ITA4VE	ITB3AE	ITB4VE
Value after reset	0	0	0	0	0	0	0	0	0	0*	0	0*	0*	0*	0*	0*

Note: * Set bits 6, and 4 to 0 to 0 when not in complementary PWM mode.

Bit	Symbol	Bit Name	Description	R/W
b0	ITB4VE*1, *2	TCIV4 Interrupt Skipping Link Enable	0: TCI4V interrupt skipping is not linked 1: TCI4V interrupt skipping is linked	R/W
b1	ITB3AE*1, *2	TGIA3 Interrupt Skipping Link Enable	0: TGI3A interrupt skipping is not linked 1: TGI3A interrupt skipping is linked	R/W
b2	ITA4VE*1, *2	TCIV4 Interrupt Skipping Link Enable	0: TCI4V interrupt skipping is not linked 1: TCI4V interrupt skipping is linked	R/W
b3	ITA3AE*1, *2	TGIA3 Interrupt Skipping Link Enable	0: TGI3A interrupt skipping is not linked 1: TGI3A interrupt skipping is linked	R/W
b4	DT4BE	Down-Count TRG4BN Enable	0: A/D converter start requests (TRG4BN) disabled during MTU4.TCNT down-count operation 1: A/D converter start requests (TRG4BN) enabled during MTU4.TCNT down-count operation	R/W
b5	UT4BE	Up-Count TRG4BN Enable	0: A/D converter start requests (TRG4BN) disabled during MTU4.TCNT up-count operation 1: A/D converter start requests (TRG4BN) enabled during MTU4.TCNT up-count operation	R/W
b6	DT4AE	Down-Count TRG4AN Enable	0: A/D converter start requests (TRG4AN) disabled during MTU4.TCNT down-count operation 1: A/D converter start requests (TRG4AN) enabled during MTU4.TCNT down-count operation	R/W
b7	UT4AE	Up-Count TRG4AN Enable	0: A/D converter start requests (TRG4AN) disabled during MTU4.TCNT up-count operation 1: A/D converter up requests (TRG4AN) enabled during MTU4.TCNT down-count operation	R/W
b13 to b8	—	Reserved	These bits are always read as 0. The write value should be 0.	R/W
b15, b14	BF[1:0]	MTU4.TADCOBRA/B Transfer Timing Select	See Table 18.31 for details.	R/W

Note Since channels 4 and 10 have the same functionality, the explanation here is only for unit 0.

Note Access to TADCR in 8-bit units is prohibited. Always access this register in 16-bit units.

Note 1. While interrupt skipping is prohibited (i.e. while the T3AEN and T4VEN bits and the skipping count setting bits (T3ACOR and T4VCOR) in the timer interrupt skipping set register (TITCR) are set to 0), set this bit to 0.

Note 2. Requests to start A/D converter are not issued if the setting for interlocking with interrupt skipping is made while interrupt skipping is prohibited.

<Before correction (p.910)>

Table 18.31 Setting of Transfer Timing by BF[1:0] Bits

Bit 15	Bit 14	
BF[1]	**BF[0]**	**Description**
0	0	Does not transfer data from the cycle set buffer register to the cycle set register.
0	1	Transfers data from the cycle set buffer register to the cycle set register at the crest of the MTUn.TCNT count.*1
1	0	Transfers data from the cycle set buffer register to the cycle set register at the trough of the MTUn.TCNT count.*2
1	1	Transfers data from the cycle set buffer register to the cycle set register at the crest and trough of the MTUn.TCNT count.*2

[Legend] n = 4 or 10, m = 3 or 9

Note 1. Data is transferred from the cycle set buffer register to the cycle set register when the crest of the MTUn.TCNT count is reached in complementary PWM mode, when a compare match occurs between MTUm.TCNT and MTUm.TGRA in reset-synchronized PWM mode, or when a compare match occurs between MTUn.TCNT and

MTUn.TGRA in PWM mode 1 or normal mode.

Note 2. These settings are prohibited when complementary PWM mode is not selected.

<After correction>

Table 18.31 Setting of Transfer Timing by BF[1:0] Bits

Bit 15	Bit 14	Description	
BF1	BF0	Complementary PWM Mode	Reset Synchronous PWM Mode
0	0	Does not transfer data from the cycle set buffer register (MTUn.TADCOBRA/MTUn.TADCOBRB) to the cycle set register (MTUn.TADCORA/MTUn.TADCORB)	Does not transfer data from the cycle set buffer register (MTUn.TADCOBRA/MTUn.TADCOBRB) to the cycle set register (MTUn.TADCORA/MTUn.TADCORB)
0	1	Transfers data from the cycle set buffer register (MTUn.TADCOBRA/MTUn.TADCOBRB) to the cycle set register (MTUn.TADCORA/MTUn.TADCORB) at the crest of MTUn.TCNT	Transfers data from the cycle set buffer register (MTUn.TADCOBRA/MTUn.TADCOBRB) to the cycle set register (MTUn.TADCORA/MTUn.TADCORB) at a compare match between MTUm.TCNT and MTUm.TGRA
1	0	Transfers data from the cycle set buffer register (MTUn.TADCOBRA/MTUn.TADCOBRB) to the cycle set register (MTUn.TADCORA/MTUn.TADCORB) at the trough of MTUn.TCNT	Setting prohibited
1	1	Transfers data from the cycle set buffer register (MTUn.TADCOBRA/MTUn.TADCOBRB) to the cycle set register (MTUn.TADCORA/MTUn.TADCORB) at the crest and trough of MTUn.TCNT	Setting prohibited

Bit 15	Bit 14	Description	
BF1	BF0	PWM Mode 1	Normal Mode
0	0	Does not transfer data from the cycle set buffer register (MTUn.TADCOBRA/MTUn.TADCOBRB) to the cycle set register (MTUn.TADCORA/MTUn.TADCORB)	Does not transfer data from the cycle set buffer register (MTUn.TADCOBRA/MTUn.TADCOBRB) to the cycle set register (MTUn.TADCORA/MTUn.TADCORB)
0	1	Transfers data from the cycle set buffer register (MTUn.TADCOBRA/MTUn.TADCOBRB) to the cycle set register (MTUn.TADCORA/MTUn.TADCORB) at a compare match between MTUn.TCNT and MTUn.TGRA	Transfers data from the cycle set buffer register (MTUn.TADCOBRA/MTUn.TADCOBRB) to the cycle set register (MTUn.TADCORA/MTUn.TADCORB) at a compare match between MTUn.TCNT and MTUn.TGRA
1	0	Setting prohibited	Setting prohibited
1	1	Setting prohibited	Setting prohibited

[Legend] n = 4, 10, m = 3, 9

18.3.9 A/D Converter Start Request Delaying Function

(1) Example of Procedure for Specifying A/D Converter Start Request Delaying Function

<Before correction (p.1000)>

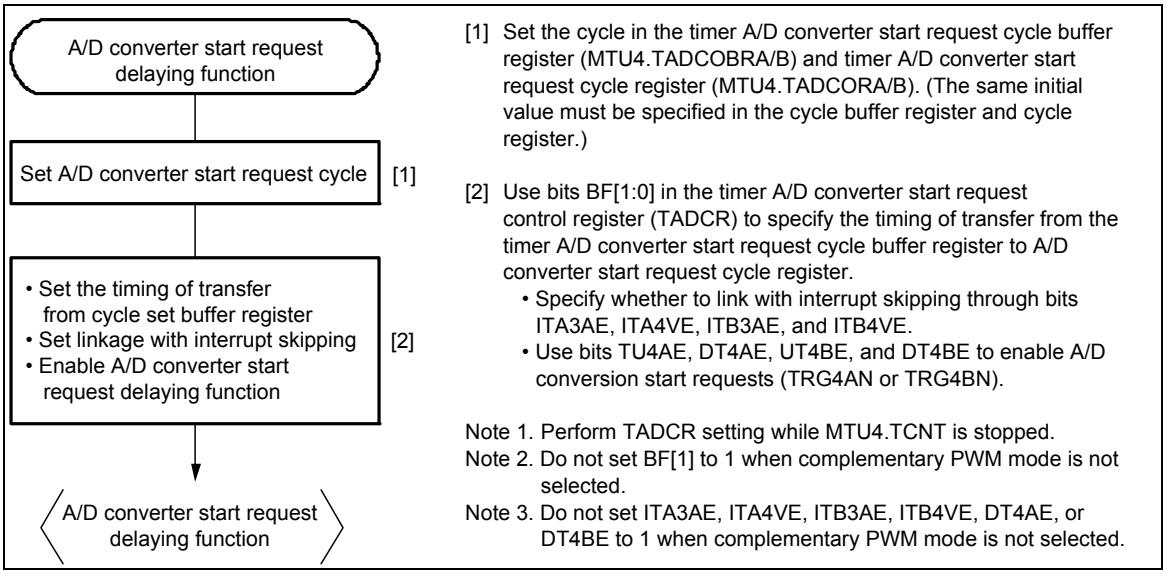

Figure 18.74 Example of Procedure for Specifying A/D Converter Start Request Delaying Function

<After correction>

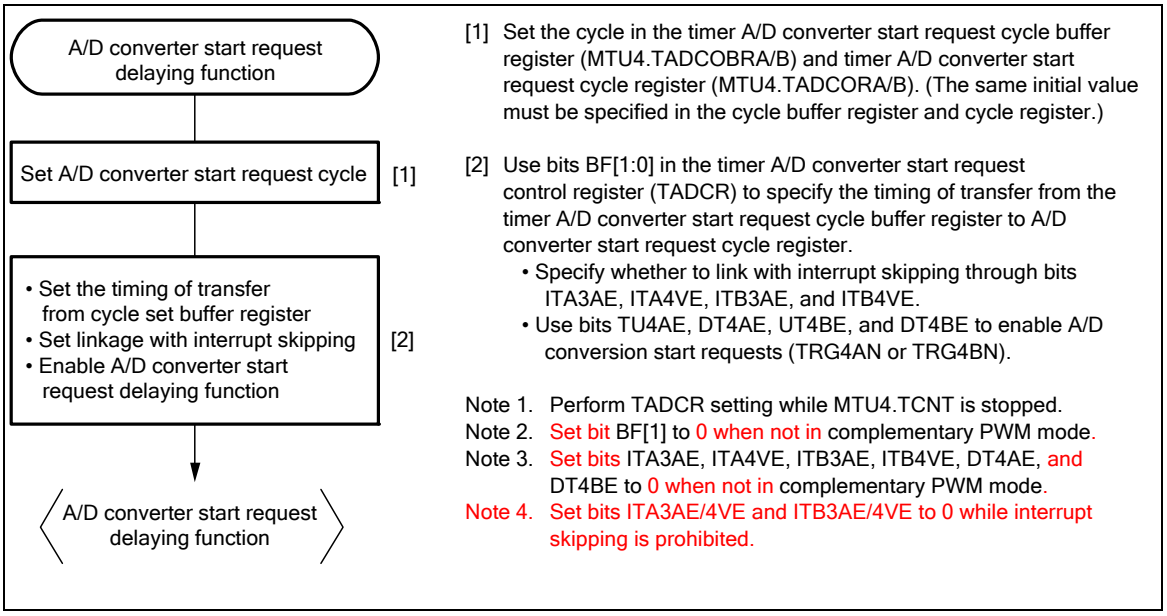

Figure 18.74 Example of Procedure for Specifying A/D Converter Start Request Delaying Function

(2) Basic Example of A/D Converter Start Request Delaying Function Operation

<Before correction (p.1001)>

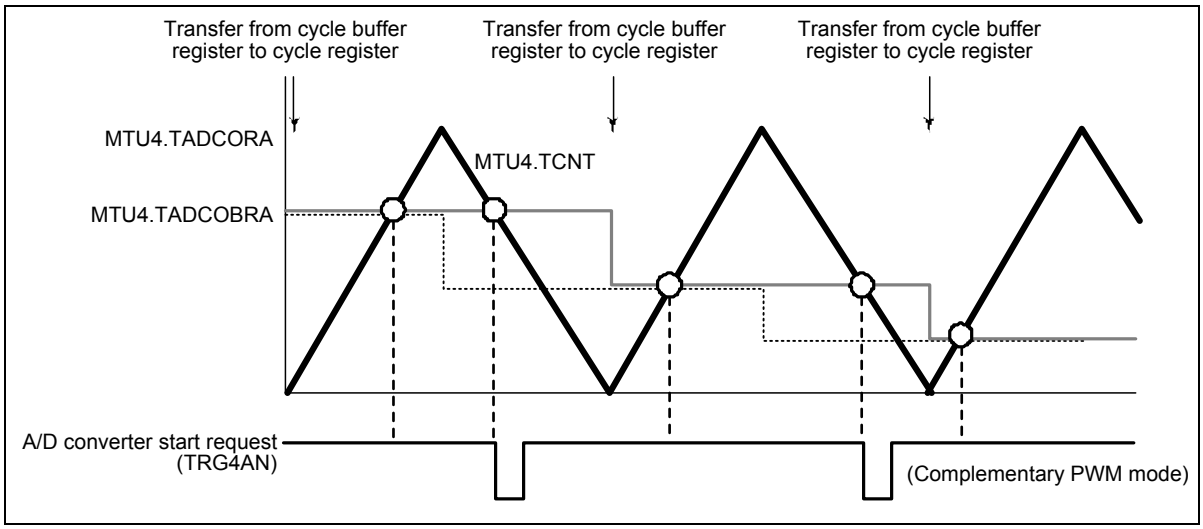

Figure 18.75 Basic Example of A/D Converter Start Request Signal (TRG4AN) Operation (Unit 0)

<After correction>

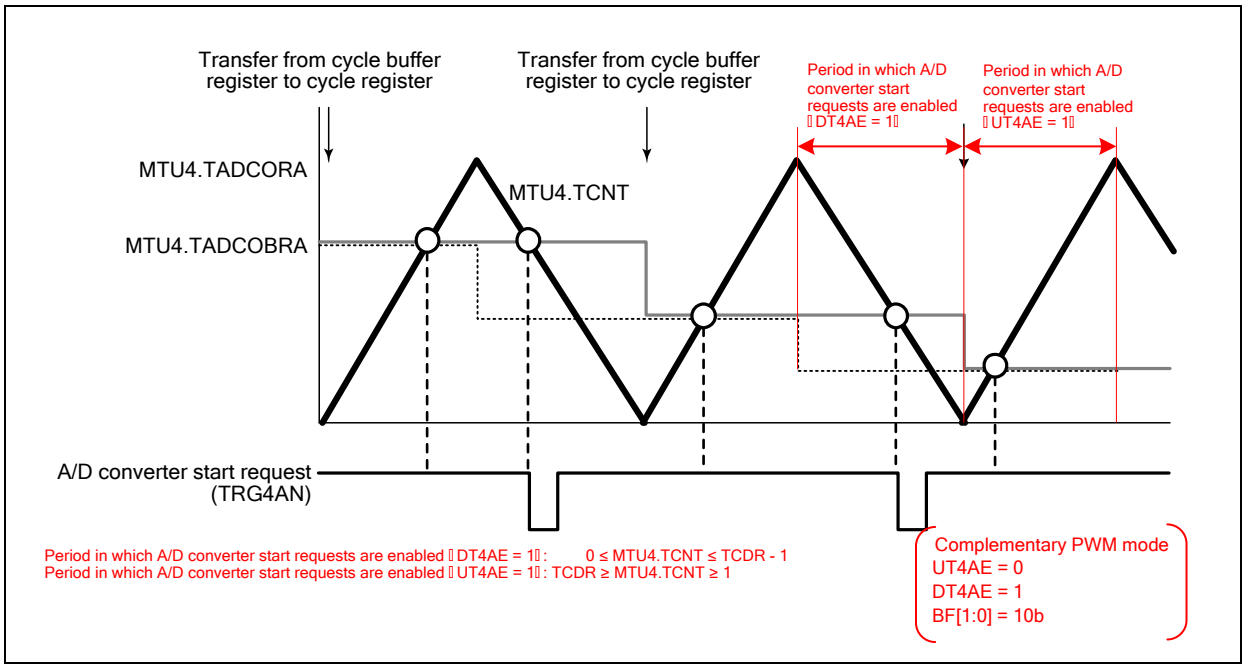

Figure 18.75 Basic Example of A/D Converter Start Request Signal (TRG4AN) Operation (Unit 0)

<Addition>

(3) Period in Which A/D Converter Start Requests are Enabled

When MTUn.TCNT and MTUn.TADCORA/MTUn.TADCORB match during the period enabled by the UT4AE, DT4AE, UT4BE, or DT4BE bit in MTUn.TADCR, the corresponding A/D converter start request (TRG4AN or TRG4BN) is generated.

If the UT4AE or UT4BE bit is set to 1 in complementary PWM mode, A/D converter start requests are enabled during the MTUn.TCNT up-counting period (0 ≤ MTUn.TCNT ≤ TCDR - 1). A/D converter start requests are enabled during the MTUnTCNT down-counting period (TCDR ≥ MTUn.TCNT ≥ 1) if the DT4AE or DT4BE bit is set to 1 (Figure 18.75).

Clear the DT4AE and DT4BE bits to 0 when not in complementary PWM mode. Setting the UT4AE or UT4BE bit to 1 causes an A/D converter start request to be generated at a compare match between MTUn.TCNT and MTUn.TADCORA/MTUn.TADCORB, regardless of whether MTUn.TCNT is counting up or down (n = 4, 10).

(3) Buffer Transfer

The title is changed to “(4) Buffer Transfer”.

<Before correction (p.1001)>

The data in the timer A/D converter start request cycle set registers (MTUn.TADCORA and MTUn.TADCORB) is updated by writing data to the timer A/D converter start request cycle set buffer registers (MTUn.TADCOBRA and MTUn.TADCOBRB). Data is transferred from the buffer registers to the respective cycle set registers at the timing selected with the BF[1:0] bits in the timer A/D converter start request control register (MTUn.TADCR). (n = 4 or 10)

<After correction>

The data in the timer A/D converter start request cycle set registers (MTUn.TADCORA and MTUn.TADCORB) is updated by writing data to the timer A/D converter start request cycle set buffer registers (MTUn.TADCOBRA and MTUn.TADCORB). Data is transferred from the buffer registers to the respective cycle set registers at the timing selected with the BF[1:0] bits in the timer A/D converter start request control register (MTUn.TADCR). (n = 4 or 10)

There are notes on the timing for transferring data when using buffer transfer in complementary PWM mode.

For details, see section 18.6.25, Notes on A/D converter Delaying Function in Complementary PWM Mode.

In modes other than complementary PWM mode, set the BF1 bit in the MTU4.TADCR register to 0.

(4) A/D Converter Start Request Delaying Function Linked with Interrupt Skipping

The title is changed to (5) A/D Converter Start Request Delaying Function Linked with Interrupt Skipping.

<Before correction (p.1001)>

A/D converter start requests (TRG4AN and TRG4BN) can be issued in coordination with interrupt skipping by the ITA3AE, ITA4VE, ITB3AE, and ITB4VE bits in the timer A/D converter start request control register (TADCR).

Figure 18.76 shows an example of A/D converter start request signal (TRG4AN) operation when TRG4AN output is enabled during MTUn.TCNT up-counting and down-counting and A/D converter start requests are linked with interrupt skipping.

Figure 18.77 shows another example of A/D converter start request signal (TRG4AN) operation when TRG4AN output is enabled during MTUn.TCNT up-counting and A/D converter start requests are linked with interrupt skipping. (n = 4 or 10)

Note: This function should be used in combination with interrupt skipping.

When interrupt skipping is disabled (the T3AEN and T4VEN bits in the timer interrupt skipping set register (TITCR) are cleared to 0 or the skipping count set bits (T3ACOR and T4VCOR) in TITCR are cleared to 0), make sure that A/D converter start requests are not linked with interrupt skipping (clear the ITA3AE, ITA4VE, ITB3AE, and ITB4VE bits in the timer A/D converter start request control register (TADCR) to 0).

Note that TRG4ABN (TRG4AN or TRG4BN) is output as the A/D converter start request signal in this case.

<After correction>

In complementary PWM mode, A/D converter start requests (TRG4AN and TRG4BN) can be issued in coordination with interrupt skipping by making settings the ITA3AE, ITA4VE, ITB3AE, and ITB4VE bits in the timer A/D converter start request control register (TADCR).

Figure 18.76 shows an example of A/D converter start request signal (TRG4AN) operation when TRG4AN output is enabled during MTUn.TCNT up-counting and down-counting and A/D converter start requests are linked with interrupt skipping.

Figure 18.77 shows another example of A/D converter start request signal (TRG4AN) operation when TRG4AN output is enabled during MTUn.TCNT up-counting and A/D converter start requests are linked with interrupt skipping. (n = 4 or 10)

In modes other than complementary PWM mode, do not use the A/D converter start request delaying function linked with the interrupt skipping function.

Set the ITA3AE, ITA4VE, ITB3AE, and ITB4VE bits in the MTU4.TADCR register to 0.

Note: This function should be used in combination with interrupt skipping.

When interrupt skipping is disabled (the T3AEN and T4VEN bits in the timer interrupt skipping set register (TITCR) are cleared to 0 or the skipping count set bits (T3ACOR and T4VCOR) in TITCR are cleared to 0), make sure that A/D converter start requests are not linked with interrupt skipping (clear the ITA3AE, ITA4VE, ITB3AE, and ITB4VE bits in the timer A/D converter start request control register (TADCR) to 0).

Note that TRG4ABN (TRG4AN or TRG4BN) is output as the A/D converter start request signal in this case.

When this function is used, MTUn.TADCORA and MTUn.TADCORB should be set with the value ranging 0002h to the value set in TCDRA minus 2 (n = 4, 10).

<Addition>

18.6.25 Usage Notes on A/D Converter Delaying Function in Complementary PWM Mode

- When MTUn.TADCOBRA/MTUn.TADCOBRB is set to 0 and the UT4AE or UT4BE bit in MTUn.TADCR is set to 1, and the result is transfer to the buffer when counting by MTUn.TCNT reaches its trough, an A/D converter start request is not generated during the up-counting period immediately following the transfer (Figure 18.125).
- When the same value as that of TCDR is set to MTUn.TADCOBRA/MTUn.TADCOBRB and the DT4AE or DT4BE bit in TADCR is set to 1, and the result is transferred to the buffer when counting by MTUn.TCNT reaches its crest, an A/D converter start request is not generated during the down-counting period immediately following the transfer (Figure 18.126).
- When A/D converter start requests are linked to the interrupt skipping function, set TADCORA/TADCORB to meet the condition 2 ≤ MTUn.TADCORA/MTUn.TADCORB ≤ TCDR - 2. (n = 4, 10)

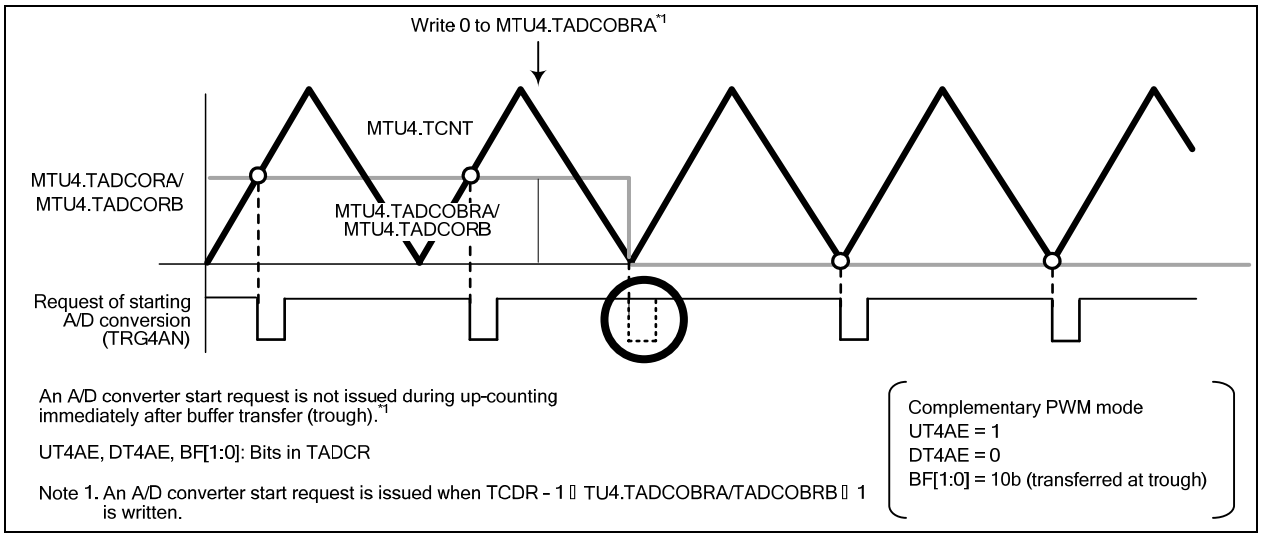

Figure 18.125 A/D Converter Start Request When 0 is Written to MTU4.TADCOBRA

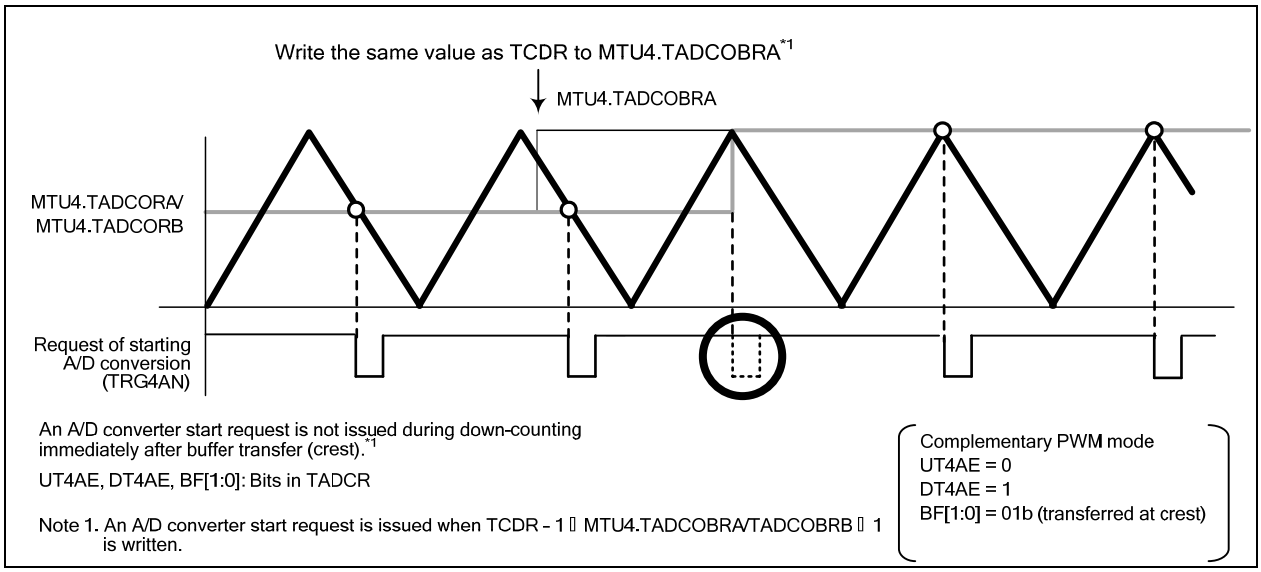

Figure 18.126 A/D Converter Start Request When the Same Value as TCDR is Written to MTU4.TADCOBRA

[Applicable Products and Reference Documents]

Series	Group	Reference Document	Rev.	Ref. No.	Section No. of MTU2
RX600	RX62N/621	RX62N/RX621 Group User's Manual: Hardware	1.40	R01UH0033EJ0140	18
	RX63N/631	RX63N/RX631 Group User's Manual: Hardware	1.80	R01UH0041EJ0180	23
	RX630	RX630 Group User's Manual: Hardware	1.60	R01UH0040EJ0160	22
RX200	RX210	RX210 Group User's Manual: Hardware	1.50	R01UH0037EJ0150	21
	RX220	RX220 Group User's Manual: Hardware	1.10	R01UH0292EJ0110	21
	RX21A	RX21A Group User's Manual: Hardware	1.10	R01UH0251EJ0110	22
RX100	RX111	RX111 Group User's Manual: Hardware	1.10	R01UH0365EJ0110	20
	RX113	RX113 Group User's Manual: Hardware	1.02	R01UH0448EJ0102	20