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RENESAS TECHNICAL UPDATE

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Product Category	MPU & MCU		Document No.	TN-16C-A201A/E	Rev.	1.00
Title	Specification Modifications in M16C/65, M16C/64A, M16C/63, and M16C/6C Groups		Information Category	Technical Notification		
Applicable Product	M16C/65, M16C/64A, M16C/63, and M16C/6C Groups	Lot No. —	Reference Document	Supplement for Serial Interface UARTi		

Specifications of the M16C/65, M16C/64A, M16C/63, and M16C/6C Groups have changed. MCU usage and setting procedures have also been added or changed. The items and targeted groups are listed below.

1. Specification Changes

Item			Targeted Group			
			65	64A	63	6C
1.1 Voltage Detector			✓	✓	✓	✓
1.2 Clock Generator			✓	✓	–	✓
1.3 External Bus			✓	✓	✓	✓
1.4 Remote Control Signal Receiver			✓	✓	✓	–
1.5 Serial Interface UARTi			✓	✓	✓	✓
1.6 Flash Memory			✓	✓	✓	✓
1.7 Electrical Characteristics	1.7.1 Power-On Reset Circuit	1.7.1.1 V_{por1}	–	–	✓	✓
		1.7.1.2 $t_{w(por)}$	✓	✓	✓	✓
	1.7.2 External Bus		✓	✓	✓	✓
	1.7.3 Timer S Input		–	–	–	✓

✓ : Targeted, – : Not targeted

2. Additions and Changes on Usage and Setting Procedures

Item		Targeted Group			
		65	64A	63	6C
2.1 Voltage Detector		✓	✓	✓	✓
2.2 Timer S		–	–	–	✓
2.3 Serial Interface UARTi		✓	✓	✓	✓
2.4 Flash Memory	2.4.1 FMSTP Bit 2.4.2 User Boot Mode	✓	✓	✓	✓
	2.4.3 Procedure for Enabling Suspend Function	–	–	✓	–
2.5 Electrical Characteristics	2.5.1 Multi-master I^2C-bus	✓	✓	✓	✓
	2.5.2 CEC Function	✓	✓	✓	–

✓ : Targeted, – : Not targeted

1. Specification Changes

1.1 Voltage Detector (for the M16C/65, M16C/64A, M16C/63, and M16C/6C Groups)

Do not use the voltage monitor 0 digital filter. Set b1 in the VW0C register to 1, and b4 and b5 to 0. Diagrams for the VW0C register are shown below.

Post modification

Voltage Monitor 0 Control Register

b7	b6	b5	b4	b3	b2	b1	b0
1	1	0	0		0	1	

Symbol	Address	Reset Value
VW0C	002Ah	1000 XX10b (1) 1100 XX11b (2)

Bit Symbol	Bit Name	Function	RW
VW0C0	Voltage monitor 0 reset enable bit	0 : Disabled 1 : Enabled	RW
— (b1)	Reserved bit	Set to 1.	RW
— (b2)	Reserved bit	Set to 0. When read, the read value is undefined.	RW
— (b3)	Reserved bit	When read, the read value is undefined.	RO
— (b5-b4)	Reserved bits	Set to 0	RW
— (b7-b6)	Reserved bits	Set to 1	RW

Notes:
1. This is the reset value when the LVDAS bit of address OFS1 is 1 during hardware reset.
2. This is the reset value after voltage monitor 0 reset, power-on reset, and when the LVDAS bit of address OFS1 is 0 during hardware reset.

Premodification

Voltage Monitor 0 Control Register

b7	b6	b5	b4	b3	b2	b1	b0
1	1				0		

Symbol	Address	After Reset
VW0C	002Ah	1100 XX10b (1) 1100 XX11b (2)

Bit Symbol	Bit Name	Function	RW
VW0C0	Voltage monitor 0 reset enable bit	0 : Disabled 1 : Enabled	RW
VW0C1	Voltage monitor 0 digital filter disable mode select bit	0 : Digital filter enabled 1 : Digital filter disabled	RW
— (b2)	Reserved bit	Set to 0. When read, the read value is undefined.	RW
— (b3)	Reserved bit	When read, the read value is undefined.	RO
VW0F0	Sampling clock select bit	b5 b4 0 0 : fOCO-S divided by 1 0 1 : fOCO-S divided by 2 1 0 : fOCO-S divided by 4 1 1 : fOCO-S divided by 8	RW
VW0F1			
— (b7-b6)	Reserved bits	Set to 1	RW

Notes:
1. This is the reset value when the LVDAS bit of address OFS1 is 1 during hardware reset.
2. This is the reset value after voltage monitor 0 reset, power-on reset, and when the LVDAS bit of address OFS1 is 0 during hardware reset.

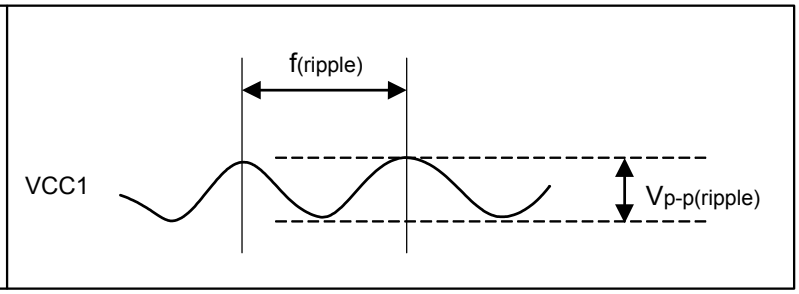
1.2 Clock Generator (for the M16C/65, M16C/64A, and M16C/6C Groups)

To use the PLL frequency synthesizer, stabilize the supply voltage within the acceptable range of the power supply ripple. The table below lists the acceptable range of power supply ripple, and the figure below shows the voltage fluctuation timing.

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
$f_{(ripple)}$	Power supply ripple allowable frequency (VCC1)				10	kHz
$V_{P-P(ripple)}$	Power supply ripple allowable amplitude voltage	(VCC1 = 5 V)			0.5	V
		(VCC1 = 3 V)			0.3	V
$V_{CC(\lvert\Delta V/\Delta T\rvert)}$	Power supply ripple rising/falling gradient	(VCC1 = 5 V)			0.3	V/ms
		(VCC1 = 3 V)			0.3	V/ms

f(ripple)
Power supply ripple allowable frequency (VCC1)

Vp-p(ripple)
Power supply ripple allowable amplitude voltage



1.3 External Bus (for the M16C/65, M16C/64A, M16C/63, and M16C/6C Groups)

When the $\overline{HOLD}$ function is used, ROM or RAM may be misread and the program may not be executed as expected. Therefore, the $\overline{HOLD}$ function is unavailable.

In memory expansion mode or microprocessor mode, connect the P5_5 pin ($\overline{HOLD}$) to VCC2 via a resistor and leave the P5_4 pin ($\overline{HLDA}$) open.

1.4 Remote Control Signal Receiver (for the M16C/65, M16C/64A, and M16C/63 Groups)

When reading registers PMC0BC (addresses D08Bh to D08Ah) and PMC1BC (addresses D09Fh to D09Eh), the read value may be undefined. Do not use these registers.

1.5 Serial Interface UARTi (for the M16C/65, M16C/64A, M16C/63, and M16C/6C Groups)

While in special mode 2, when the CKPH bit in the UiSMR3 register is 1 (with clock delay), slave mode is unavailable. Therefore, slave mode has been deleted from the next version of the user's manual.

1.6 Flash Memory (for the M16C/65, M16C/64A, M16C/63, and M16C/6C Groups)

Note the following when using the block blank check command:

- The block blank check command is designated for use with a programmer.
- When an instantaneous power failure occurs while the block erase command is executed, execute the block erase command again. The block blank check command cannot be used to check whether the erase operation is successfully completed or not.
- Do not execute the block blank check command during suspend. (for M16C/63 Group)

1.7 Electrical Characteristics

1.7.1 Power-On Reset Circuit

1.7.1.1 V_{por1} (for the M16C/63 and M16C/6C Groups)

The maximum value of V_{por1} (voltage at which power-on reset enabled) has been improved from 0.1 to 0.5 V.

1.7.1.2 $t_{w(por)}$ (for the M16C/65, M16C/64A, M16C/63, and M16C/6C Groups)

The minimum value of $t_{w(por)}$ (time necessary to enable power-on reset) has been improved to 300 ms (when $-40°C \leq T_{opr} \leq 85°C$). Premodification, the value was 30 s or more when $-20°C \leq T_{opr} \leq 85°C$, and 3000 s or more when $-40°C \leq T_{opr} < -20°C$.

1.7.2 External Bus (for the M16C/65, M16C/64A, M16C/63, and M16C/6C Groups)

The standard values of the $\overline{RDY}$ signal have been modified to the values shown below.

VCC1 = VCC2 = 5 V

Symbol	Parameter	Standard (Min.)		Unit
		Premodification	Post modification	
$t_{su(RDY-BCLK)}$	$\overline{RDY}$ input setup time	30	80	ns

VCC1 = VCC2 = 3 V

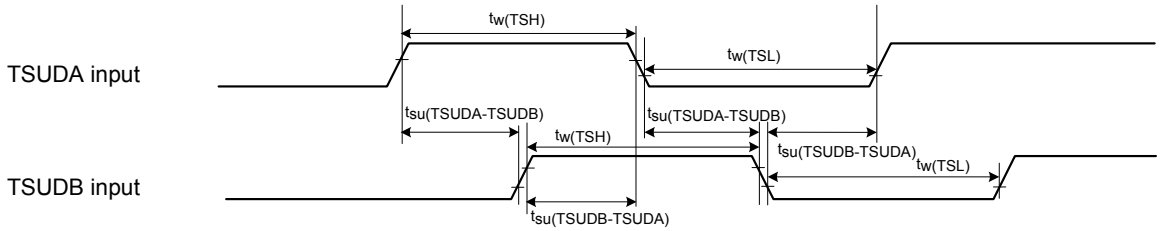
Symbol	Parameter	Standard (Min.)		Unit
		Premodification	Post modification	
$t_{su(RDY-BCLK)}$	$\overline{RDY}$ input setup time	40	85	ns

1.7.3 Timer S Input (for the M16C/6C Group)

The specification for two-phase pulse input in two-phase pulse signal processing mode has been added.
Pin names have also been added: P8_0 is TSUDA and P8_1 is TSUDB.

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TSH)}$	TSUDA, TSUDB input high pulse width	2		µs
$t_{w(TSL)}$	TSUDA, TSUDB input low pulse width	2		µs
$t_{su(TSUDA-TSUDB)}$	TSUDB input setup time	1		µs
$t_{su(TSUDB-TSUDA)}$	TSUDA input setup time	1		µs

Two-phase pulse input in two-phase pulse signal processing mode



Note:
1. When the TSUDA and TSUDB phases are interchanged, $t_{su(TSUDA-TSUDB)}$ and $t_{su(TSUDB-TSUDA)}$ are also interchanged.

2. Additions and Changes on Usage and Setting Procedures

2.1 Voltage Detector (for the M16C/65, M16C/64A, M16C/63, and M16C/6C Groups)

2.1.1 Voltage Detector 0

2.1.1.1 b6 in the VW0C register

When the LVDAS bit in the OFS1 address is 1, b6 in the VW0C register becomes 0 after a hardware reset. When using the voltage monitor 0 reset, set this bit to 1.

2.1.1.2 Procedure for setting voltage monitor 0 reset related bits

When the LVDAS bit in the OFS1 address is 1 (voltage monitor 0 reset disabled after hardware reset), set the related bits according to the following procedure:

(1) Set the VC25 bit in the VCR2 register to 1 (voltage detector 0 enabled).
(2) Wait for td(E-A).
(3) Set the VW0C0 bit in the VW0C register to 1 (voltage monitor 0 reset enabled).

When the LVDAS bit in the OFS1 address is 0 (voltage monitor 0 reset enabled after hardware reset), the above procedure is unnecessary.

2.1.2 Voltage Detector 1 and Voltage Detector 2

2.1.2.1 Voltage monitor 1 interrupt and voltage monitor 1 reset

Even if the voltage monitor 1 interrupt/reset is disabled, a low voltage is detected and the VW1C2 bit in the VW1C register becomes 1 (Vdet1 passage detected) when voltage detector 1 is enabled.

During the setting procedure of the voltage monitor 1 interrupt/reset related bits, after enabling voltage detector 1, a low voltage may be detected until the VW1C0 bit in the VW1C register is set to 1 (voltage monitor 1 interrupt/reset enabled). In this case, neither an interrupt request nor reset is generated.

When using this detection result, read the VW1C2 bit after setting the VW1C0 bit to 1. If the bit is 1, execute the process to be performed when low voltage is detected.

When ignoring this detection result, set the VW1C2 bit to 0 after setting the VW1C0 bit to 1.

This also applies to the voltage monitor 2 interrupt/reset.

2.1.2.2 Procedures for setting voltage monitor 1 or 2 interrupt/reset related bits

Set the voltage monitor 1 interrupt/reset related bits as shown below. The procedure for setting the voltage monitor 2 interrupt/reset related bits is the same.

Post modification

Turning the 125 kHz on-chip oscillator on and the oscillation stabilize wait time have been moved from the beginning of the procedure to steps 9 and 10.

Step	When Using the Digital Filter		When Not Using the Digital Filter	
	Voltage monitor 1 interrupt	Voltage monitor 1 reset	Voltage monitor 1 interrupt	Voltage monitor 1 reset
1	Set the VW12E bit in the VWCE register to 1 (voltage monitors 1 and 2 enabled).			
2	Set bits VD1LS3 to VD1LS0 in the VD1LS register to select Vdet1.			
3	Set the VC26 bit in the VCR2 register to 1 (voltage detector 1 enabled).			
4	Wait for td(E-A).			
5	Use bits VW1F1 and VW1F0 in the VW1C register to select the digital filter sampling clock.		Use the VW1C7 bit in the VW1C register to select the timing of the interrupt and reset request. (1)	
6 (2)	Set the VW1C1 bit in the VW1C register to 0 (digital filter enabled).		Set the VW1C1 bit in the VW1C register to 1 (digital filter disabled).	
7 (2)	Set the VW1C6 bit in the VW1C register to 0 (voltage monitor 1 interrupt).	Set the VW1C6 bit in the VW1C register to 1 (voltage monitor 1 reset).	Set the VW1C6 bit in the VW1C register to 0 (voltage monitor 1 interrupt).	Set the VW1C6 bit in the VW1C register to 1 (voltage monitor 1 reset).
8	Set the VW1C2 bit in the VW1C register to 0 (Vdet1 passage not detected).			
9	Set the CM14 bit in the CM1 register to 0 (125 kHz on-chip oscillator on)		-	
10	Wait for digital filter sampling clock x 3 cycles.		- (no wait time)	
11	Set the VW1C0 bit in the VW1C register to 1 (voltage monitor 1 interrupt/reset enabled).			

Notes:

1. Set the VW1C7 bit to 1 (when VCC1 reaches Vdet1 or below) for the voltage monitor 1 reset.
2. When the VW1C0 bit is 0, steps 5, 6, and 7 can be executed simultaneously (with one instruction).
3. If above setting is performed while voltage monitor 1 interrupt/reset is disabled (VW1C0 bit in the VW1C register is 0, VC26 bit in the VCR2 register is 0) and VCC1 < Vdet1 (or VCC1 > Vdet1) is detected before enabling voltage monitor 1 interrupt/reset (step 11), an interrupt does not occur. When VCC1 < Vdet1 (or VCC1 > Vdet1) is detected while executing steps 9 to 11, the VW1C2 bit becomes 1.
   When using this result detected between steps 9 and 11, read the VW2C2 bit after step 11. If the bit is 1, execute the process to be performed after detecting the VCC1 < Vdet1 (or VCC1 > Vdet1).
   When ignoring the result detected between step 9 and step 11, set the VW1C2 bit to 0 after step 11.

Premodification

Step	When Using the Digital Filter		When Not Using the Digital Filter	
	Voltage Monitor 1 Interrupt	Voltage Monitor 1 Reset	Voltage Monitor 1 Interrupt	Voltage Monitor 1 Reset
1	Set the CM14 bit in the CM1 register to 0 (125 kHz on-chip oscillator on)		-	
2	Wait for digital filter sampling clock x 3 cycles.		- (no wait time)	
3	Set the VW12E bit in the VWCE register to 1 (voltage detectors 1 and 2 enabled).			
4	Set bits VD1LS3 to VD1LS0 in the VD1LS register to select Vdet1.			
5	Set the VC26 bit in the VCR2 register to 1 (voltage detector 1 enabled).			
6	Wait for td(E(E-A).			
7	Use bits VW1F1 and VW1F0 in the VW1C register to select the digital filter sampling clock.		Use the VW1C7 bit in the VW1C register to select the timing of the interrupt and reset request. (1)	
8 (2)	Set the VW1C1 bit in the VW1C register to 0 (digital filter enabled).		Set the VW1C1 bit in the VW1C register to 1 (digital filter disabled).	
9 (2)	Set the VW1C6 bit in the VW1C register to 0 (voltage monitor 1 interrupt).	Set the VW1C6 bit in the VW1C register to 1 (voltage monitor 1 reset).	Set the VW1C6 bit in the VW1C register to 0 (voltage monitor 1 interrupt).	Set the VW1C6 bit in the VW1C register to 1 (voltage monitor 1 reset).
10	Set the VW1C2 bit in the VW1C register to 0 (Vdet1 passage not detected).			
11	Set the VW1C0 bit in the VW1C register to 1 (voltage monitor 1 interrupt/reset enabled).			

Notes:

1. Set the VW1C7 bit to 1 (when VCC reaches Vdet1 or below) for the voltage monitor 1 reset.
2. When the VW1C0 bit is 0, steps 7, 8, and 9 can be executed simultaneously (with one instruction).

2.2 Timer S (for the M16C/6C Group)

When SR waveform output mode is selected, the setting for the corresponding odd channels (the channel next to the even channel) is ignored. In SR waveform output mode, set odd channels in the G1OER register to 1 (output disabled).

2.3 Serial Interface UARTi (for the M16C/65, M16C/64A, M16C/63, and M16C/6C Groups)

Detail explanations on special mode 1 (I^2C mode) have been added to the user's manual and the application notes describe differences in the serial interface UARTi between the current user's manual and the next version have been prepared.

M16C/65 Group Supplement for Serial Interface UARTi (R01AN0418EJ0100)
M16C/64A Group Supplement for Serial Interface UARTi (R01AN0419EJ0100)
M16C/63 Group Supplement for Serial Interface UARTi (R01AN0420EJ0100)
M16C/6C Group Supplement for Serial Interface UARTi (R01AN0421EJ0100)

When developing a program using I^2C mode, refer to the following application notes:

I^2C-bus Interface Using UARTi Special Mode 1 (REJ05B1349)
I^2C-bus Interface Using UARTi Special Mode 1 (Master Transmit/Receive) (REJ05B1422)
I^2C-bus Interface Using UARTi Special Mode 1 (Slave Transmit/Receive) (REJ05B1423)

2.4 Flash Memory

2.4.1 FMSTP Bit (for the M16C/65, M16C/64A, M16C/63, and M16C/6C Groups)

When the FMR22 bit is 1 (slow read mode enabled), do not set the FMSTP bit in the FMR0 register to 1 (flash memory operation stopped). Also, when the FMSTP bit is 1, do not set the FMR22 bit to 1.

2.4.2 User Boot Mode (for the M16C/65, M16C/64A, M16C/63, and M16C/6C Groups)

Following notes have been added to the user boot mode description:

- When restarting the MCU in user boot mode after starting it in user boot mode, RAM becomes undefined.
- As the reset sequence differs, the time necessary for starting the program is longer than in single-chip mode.
- Functions in user boot mode cannot be debugged by the on-chip debugging emulator or full spec emulator.
- While using user boot mode, do not change the input level of the pin used for user boot entry (the pin selected by addresses 13FF8h to 13FFAh).
- If values at addresses 13FF0h to 13FF7h are "UserBoot" in ASCII code, and values at addresses 13FF8h to 13FFBh are all 00h, the MCU does not enter standard serial I/O mode. Therefore, the programmer or on-chip debugger cannot be connected.

2.4.3 Procedure for Enabling Suspend Function (for the M16C/63 Group)

The procedure for enabling the suspend function has been modified. The modified figures and modifications are shown below. Post modification and premodification examples of the program flowcharts in EW0 mode are shown on the next page.

Modified figures

- Program Flowchart in EW0 Mode (Suspend Function Enabled)
- Block Erase Flowchart in EW0 Mode (Suspend Function Enabled)
- Lock Bit Program Flowchart in EW0 Mode (Suspend Function Enabled)

Modifications

- The timing to set the I flag to 1 (interrupt enabled) has been changed.
- The determination flag used in maskable interrupt routine has been changed from bits FMR32 or FMR33 to the FMR00 bit.

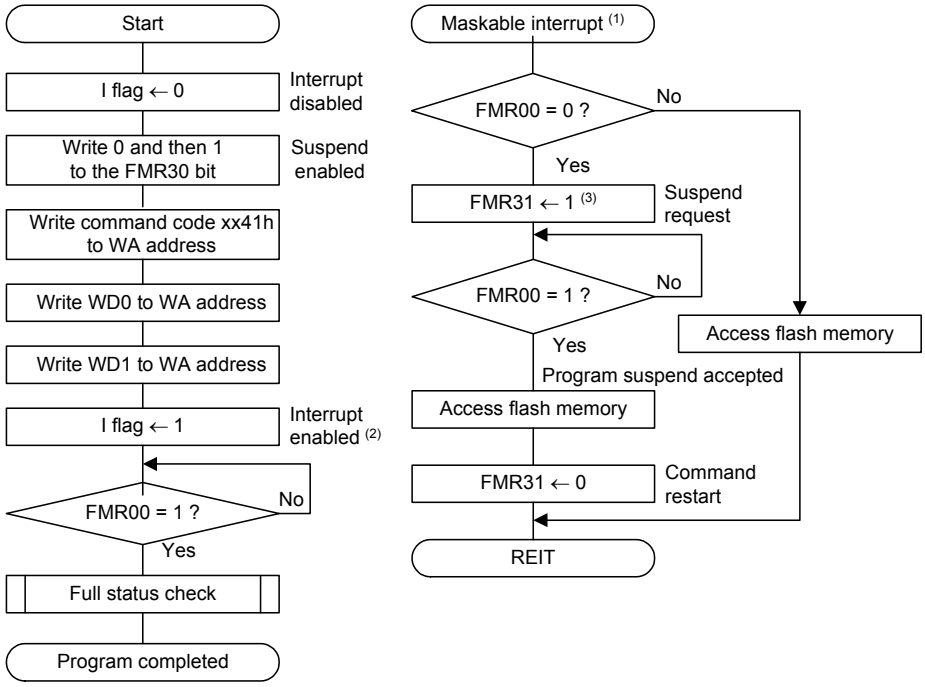
Modified figures

- Program Flowchart in EW1 Mode (Suspend Function Enabled)
- Block Erase Flowchart in EW1 Mode (Suspend Function Enabled)
- Lock Bit Program Flowchart in EW1 Mode (Suspend Function Enabled)

Modification

- The timing to set the I flag to 1 (interrupt enabled) has been changed.

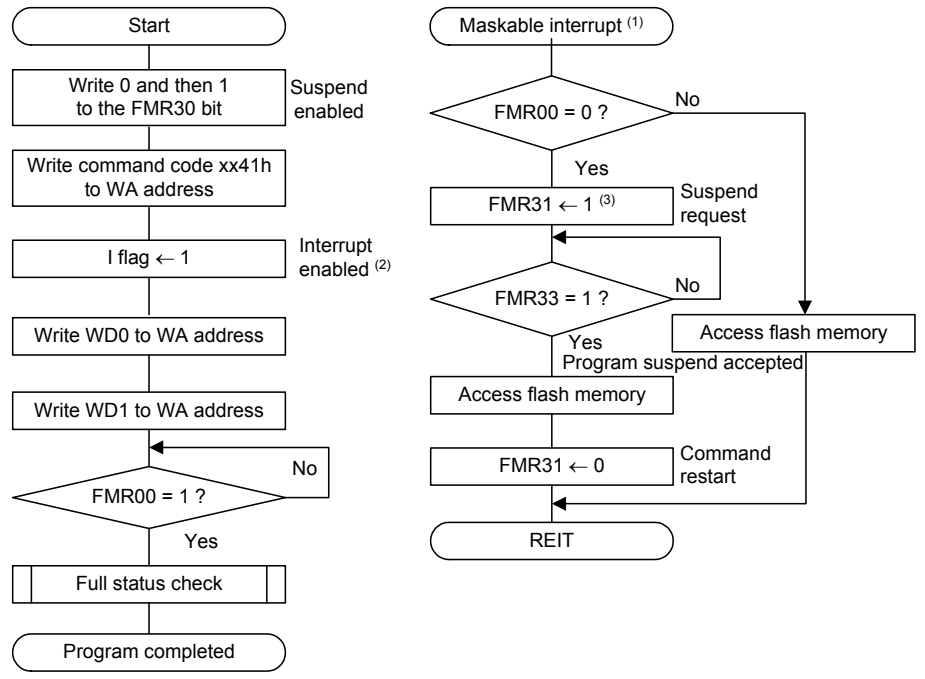
Post modification



Notes:
1. In EW0 mode, set the interrupt vector table for interrupts to be used and the interrupt routine in areas other than flash memory.
2. When interrupts are not used, an instruction to enable interrupts is not necessary.
3. Program is not suspended until td(SR-SUS) elapses after the FMR31 bit is set to 1.

Program Flowchart in EW0 Mode (Suspend Function Enabled)

Premodification



Notes:
1. In EW0 mode, set the interrupt vector table for interrupts to be used and the interrupt routine in areas other than flash memory.
2. When interrupts are not used, an instruction to enable interrupts are not necessary.
3. Program is not suspended until td(SR-SUS) elapses after the FMR31 bit is set to 1.

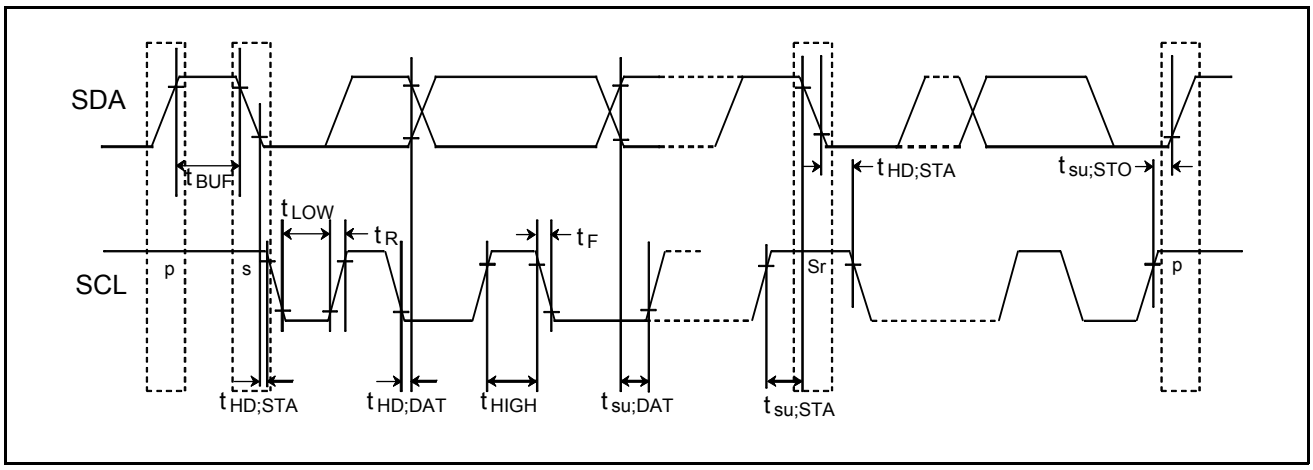
Program Flowchart in EW0 Mode (Suspend Function Enabled)

2.5 Electrical Characteristics

2.5.1 Multi-master I²C-bus (for the M16C/65, M16C/64A, M16C/63, and M16C/6C Groups)

Specifications for multi-master I²C-bus have been added.

Symbol	Parameter	Standard Clock Mode		Fast-mode		Unit
		Min.	Max.	Min.	Max.	
t_{BUF}	Bus free time	4.7		1.3		µs
$t_{HD;STA}$	Hold time in start condition	4.0		0.6		µs
t_{LOW}	Hold time in SCL clock 0 status	4.7		1.3		µs
t_R	SCL, SDA signals' rising time		1000	20 + 0.1 Cb	300	ns
$t_{HD;DAT}$	Data hold time	0		0	0.9	µs
t_{HIGH}	Hold time in SCL clock 1 status	4.0		0.6		µs
f_F	SCL, SDA signals' falling time		300	20 + 0.1 Cb	300	ns
$t_{su;DAT}$	Data setup time	250		100		ns
$t_{su;STA}$	Setup time in restart condition	4.7		0.6		µs
$t_{su;STO}$	Stop condition setup time	4.0		0.6		µs



2.5.2 CEC Function (for the M16C/65, M16C/64A, and M16C/63 Groups)

The specifications below have been added.

Recommended Operating Conditions

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
V_{CC1}, V_{CC2}	Supply voltage ($V_{CC1} \geq V_{CC2}$)	CEC function is used	2.7		3.63	V
V_{IH}	High input voltage	CEC	0.7 V_{CC1}			V
V_{IL}	Low input voltage	CEC			0.26 V_{CC1}	V

Electrical Characteristics (VCC1 = VCC2 = 3 V)

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OL}	Low output voltage	CEC	I_{OL} = 1 mA		0	0.5	V
V_{T+}-V_{T-}	Hysteresis	CEC		0.2	0.5	1.0	V
–	Leakage current in powered-off state	CEC	V_{CC1} = 0 V			1.8	µA