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RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RZ*-A0084A/E	Rev.	1.00
Title	RZ/G2E Document Collection for Pin Function Controller (PFC)		Information Category	Technical Notification		
Applicable Product	RZ/G Series, 2nd Generation RZ/G2E	Lot No. All lots	Reference Document	RZ/G Series, 2nd Generation User's Manual: Hardware Rev.1.10 (R01UH0808EJ0110)		

This technical update describes document correction of RZ/G Series, 2nd Generation product.

[Summary]

Document Collection for 9. Pin Function Controller (PFC) [RZ/G2E] in initial bit.

[Priority level]

Importance: “Normal”

Urgency: “Normal”

[Products]

RZ/G2E

[Section number and title]

Section 9. Pin Function Controller (PFC) [RZ/G2E]

“This is empty adjustment page to compare next Current (from) and Correction (to) on facing page. “

(By using two pages view of PDF readers this enables previously and prospectively view on odd and even pages.)

[Correction]

1. Section 9. PFC, Page 9-4 and 9-5, 9.1.4 Register Configuration, Table 9.1 Configuration of Registers in PFC. Correction of Initial value for PUEN0 and PUD0 register.

Current (from):

9.1.4 Register Configuration

Table 9.1 Configuration of Registers in PFC

Name	Abbr.	R/W	Initial Value	Address	Access Size	Condition
DRV control register 8	DRVCTRL8	R/W	H'9244_9249	H'E606_0320	32	—
DRV control register 9	DRVCTRL9	R/W	H'2492_4924	H'E606_0324	32	—
DRV control register 10	DRVCTRL10	R/W	H'2492_5258	H'E606_0328	32	—
POC control register 0	POCCTRL0	R/W	H'3FFF_FFFF	H'E606_0380	32	—
POC control register 2	POCCTRL2	R/W	H'FFFF_FFFF	H'E606_0388	32	—
TDSEL control register 0	TDSELCTRL0	R/W	H'0000_0000	H'E606_03C0	32	—
LSI pin pull-enable register 0	PUEN0	R/W	H'000F_FFE4	H'E606_0400	32	—
LSI pin pull-enable register 1	PUEN1	R/W	H'CE29_8464	H'E606_0404	32	—
LSI pin pull-enable register 2	PUEN2	R/W	H'A4C3_80F4	H'E606_0408	32	—
LSI pin pull-enable register 3	PUEN3	R/W	H'0000_079F	H'E606_040C	32	—
LSI pin pull-enable register 4	PUEN4	R/W	H'FFF0_FFFF	H'E606_0410	32	—
LSI pin pull-enable register 5	PUEN5	R/W	H'4000_0000	H'E606_0414	32	—
LSI pin pull-up/down control register 0	PUD0	R/W	H'0008_0000	H'E606_0440	32	—
LSI pin pull-up/down control register 1	PUD1	R/W	H'CE29_8464	H'E606_0444	32	—
LSI pin pull-up/down control register 2	PUD2	R/W	H'A4C3_80F0	H'E606_0448	32	—
LSI pin pull-up/down control register 3	PUD3	R/W	H'0000_079F	H'E606_044C	32	—
LSI pin pull-up/down control register 4	PUD4	R/W	H'FFF0_FFFF	H'E606_0450	32	—
LSI pin pull-up/down control register 5	PUD5	R/W	H'4000_0000	H'E606_0454	32	—
Module select register 0	MOD_SEL0	R/W	H'0000_0000	H'E606_0500	32	—
Module select register 1	MOD_SEL1	R/W	H'0000_0000	H'E606_0504	32	—

Correction (to):

9.1.4 Register Configuration

Table 9.1 Configuration of Registers in PFC

Name	Abbr.	R/W	Initial Value	Address	Access Size	Condition
DRV control register 8	DRVCTRL8	R/W	H'9244_9249	H'E606_0320	32	—
DRV control register 9	DRVCTRL9	R/W	H'2492_4924	H'E606_0324	32	—
DRV control register 10	DRVCTRL10	R/W	H'2492_5258	H'E606_0328	32	—
POC control register 0	POCCTRL0	R/W	H'3FFF_FFFF	H'E606_0380	32	—
POC control register 2	POCCTRL2	R/W	H'FFFF_FFFF	H'E606_0388	32	—
TDSEL control register 0	TDSELCTRL0	R/W	H'0000_0000	H'E606_03C0	32	—
LSI pin pull-enable register 0	PUEN0	R/W	H'FFFF_FFE4	H'E606_0400	32	—
LSI pin pull-enable register 1	PUEN1	R/W	H'CE29_8464	H'E606_0404	32	—
LSI pin pull-enable register 2	PUEN2	R/W	H'A4C3_80F4	H'E606_0408	32	—
LSI pin pull-enable register 3	PUEN3	R/W	H'0000_079F	H'E606_040C	32	—
LSI pin pull-enable register 4	PUEN4	R/W	H'FFF0_FFFF	H'E606_0410	32	—
LSI pin pull-enable register 5	PUEN5	R/W	H'4000_0000	H'E606_0414	32	—
LSI pin pull-up/down control register 0	PUD0	R/W	H'7DF8_0000	H'E606_0440	32	—
LSI pin pull-up/down control register 1	PUD1	R/W	H'CE29_8464	H'E606_0444	32	—
LSI pin pull-up/down control register 2	PUD2	R/W	H'A4C3_80F0	H'E606_0448	32	—
LSI pin pull-up/down control register 3	PUD3	R/W	H'0000_079F	H'E606_044C	32	—
LSI pin pull-up/down control register 4	PUD4	R/W	H'FFF0_FFFF	H'E606_0450	32	—
LSI pin pull-up/down control register 5	PUD5	R/W	H'4000_0000	H'E606_0454	32	—
Module select register 0	MOD_SEL0	R/W	H'0000_0000	H'E606_0500	32	—
Module select register 1	MOD_SEL1	R/W	H'0000_0000	H'E606_0504	32	—

[Description]

Correct initial value of PUEN0 and PUD0 register in RZ/G2E product of RZ/G 2nd Generation.

[Reason for Correction]

General error correction.

[Correction]

2. Section 9. PFC, Page 9-25, 9.2.8 Register Description, Table 9.9 LSI pin pull-enable register 0-5 (PUEN0-5). Correction of Initial value for PUEN0 register.

Current (from):

9.3.8 LSI pin pull-enable register 0-5 (PUEN0-5)

When the all I2C pins are selected, the pull-up/down function of these pins is disabled respectively even if the pull-up/down function is set to enable.

Table 9.9 Configuration of Registers in PUEN0-5

	PUEN0	Initial value	PUEN1	Initial value	PUEN2	Initial value	PUEN3	Initial value	PUEN4	Initial value	PUEN5	Initial value
bit31	PUEN_QSPI0_SPCLK	0	PUEN_RD_WR#	1	PUEN_D5	1	PUEN_SD0_DAT0	0	PUEN_RX1	1	PUEN_USB30_PWEN	0
bit30	PUEN_QSPI0_MOSI/IO0	0	PUEN_EX_WAIT0	1	PUEN_D6	0	PUEN_SD0_DAT1	0	PUEN_TX1	1	PUEN_USB30_OVC *	1
bit29	PUEN_QSPI0_MISO/IO1	0	—	0	PUEN_D7	1	PUEN_SD0_DAT2	0	PUEN_SCK2_A	1	—	0
bit28	PUEN_QSPI0_IO2	0	—	0	PUEN_D8	0	PUEN_SD0_DAT3	0	PUEN_TX2_A	1	—	0
bit27	PUEN_QSPI0_IO3	0	PUEN_A0	1	PUEN_D9	0	PUEN_SD1_CLK	0	PUEN_RX2_A	1	—	0
bit26	PUEN_QSPI0_SSL	0	PUEN_A1	1	PUEN_D10	1	PUEN_SD1_CMD	0	PUEN_MSIOF0_SCK	1	—	0
bit25	PUEN_QSPI1_SPCLK	0	PUEN_A2	1	PUEN_D11	0	PUEN_SD1_DAT0	0	PUEN_MSIOF0_RXD	1	—	0
bit24	PUEN_QSPI1_MOSI/IO0	0	PUEN_A3	0	PUEN_D12	0	PUEN_SD1_DAT1	0	PUEN_MSIOF0_TXD	1	—	0
bit23	PUEN_QSPI1_MISO/IO1	0	PUEN_A4	0	PUEN_D13	1	PUEN_SD1_DAT2	0	PUEN_MSIOF0_SYNC	1	—	0
bit22	PUEN_QSPI1_IO2	0	PUEN_A5	0	PUEN_D14	1	PUEN_SD1_DAT3	0	PUEN_MSIOF0_SS1	1	—	0
bit21	PUEN_QSPI1_IO3	0	PUEN_A6	1	PUEN_D15	0	PUEN_SD3_CLK	0	PUEN_MSIOF0_SS2	1	—	0
bit20	PUEN_QSPI1_SSL	0	PUEN_A7	0	PUEN_PRESETOUT#	0	PUEN_SD3_CMD	0	PUEN_SSI_SDATA9	1	—	0

Correction (to):

9.3.8 LSI pin pull-enable register 0-5 (PUEN0-5)

When all I2C pins are selected, the pull-up/down function of these pins is disabled respectively even if the pull-up/down function is set to enable.

Table 9.9 Configuration of Registers in PUEN0-5

	PUEN0	Initial value	PUEN1	Initial value	PUEN2	Initial value	PUEN3	Initial value	PUEN4	Initial value	PUEN5	Initial value
bit31	PUEN_QSPI0_SPCLK	1	PUEN_RD_WR#	1	PUEN_D5	1	PUEN_SD0_DAT0	0	PUEN_RX1	1	PUEN_USB30_PWEN	0
bit30	PUEN_QSPI0_MOSI/IO0	1	PUEN_EX_WAIT0	1	PUEN_D6	0	PUEN_SD0_DAT1	0	PUEN_TX1	1	PUEN_USB30_OVC *	1
bit29	PUEN_QSPI0_MISO/IO1	1	—	0	PUEN_D7	1	PUEN_SD0_DAT2	0	PUEN_SCK2_A	1	—	0
bit28	PUEN_QSPI0_IO2	1	—	0	PUEN_D8	0	PUEN_SD0_DAT3	0	PUEN_TX2_A	1	—	0
bit27	PUEN_QSPI0_IO3	1	PUEN_A0	1	PUEN_D9	0	PUEN_SD1_CLK	0	PUEN_RX2_A	1	—	0
bit26	PUEN_QSPI0_SSL	1	PUEN_A1	1	PUEN_D10	1	PUEN_SD1_CMD	0	PUEN_MSIOF0_SCK	1	—	0
bit25	PUEN_QSPI1_SPCLK	1	PUEN_A2	1	PUEN_D11	0	PUEN_SD1_DAT0	0	PUEN_MSIOF0_RXD	1	—	0
bit24	PUEN_QSPI1_MOSI/IO0	1	PUEN_A3	0	PUEN_D12	0	PUEN_SD1_DAT1	0	PUEN_MSIOF0_TXD	1	—	0
bit23	PUEN_QSPI1_MISO/IO1	1	PUEN_A4	0	PUEN_D13	1	PUEN_SD1_DAT2	0	PUEN_MSIOF0_SYNC	1	—	0
bit22	PUEN_QSPI1_IO2	1	PUEN_A5	0	PUEN_D14	1	PUEN_SD1_DAT3	0	PUEN_MSIOF0_SS1	1	—	0
bit21	PUEN_QSPI1_IO3	1	PUEN_A6	1	PUEN_D15	0	PUEN_SD3_CLK	0	PUEN_MSIOF0_SS2	1	—	0
bit20	PUEN_QSPI1_SSL	1	PUEN_A7	0	PUEN_PRESETOUT#	0	PUEN_SD3_CMD	0	PUEN_SSI_SDATA9	1	—	0

[Description]

Correct initial value of PUEN0 and PUD0 register in RZ/G2E product of RZ/G 2nd Generation.

[Reason for Correction]

General error correction.

[Correction]

3. Section 9. PFC, Page 9-27, 9.2.9 Register Description, Table 9.10 Configuration of Register PUD00-5. Correction of Initial value for PUEN0 register.

Current (from):

9.3.9 LSI pin pull-up/down control Register 0-5 (PUD0-5)

Table 9.10 Configuration of Registers in PUD0-5

	PUD0	Initial value	PUD1	Initial value	PUD2	Initial value	PUD3	Initial value	PUD4	Initial value	PUD5	Initial value
bit31	PUD_QSPI0_SPCLK	0	PUD_RD_WR#	1	PUD_D5	1	PUD_SD0_DAT0	0	PUD_RX1	1	PUD_USB30_PWEN	0
bit30	PUD_QSPI0_MOSI/IO0	0	PUD_EX_WAIT0	1	PUD_D6	0	PUD_SD0_DAT1	0	PUD_TX1	1	— *	1
bit29	PUD_QSPI0_MISO/IO1	0	—	0	PUD_D7	1	PUD_SD0_DAT2	0	PUD_SCK2_A	1	—	0
bit28	PUD_QSPI0_IO2	0	—	0	PUD_D8	0	PUD_SD0_DAT3	0	PUD_TX2_A	1	—	0
bit27	PUD_QSPI0_IO3	0	PUD_A0	1	PUD_D9	0	PUD_SD1_CLK	0	PUD_RX2_A	1	—	0
bit26	PUD_QSPI0_SSL	0	PUD_A1	1	PUD_D10	1	PUD_SD1_CMD	0	PUD_MSIOF0_SCK	1	—	0
bit25	PUD_QSPI1_SPCLK	0	PUD_A2	1	PUD_D11	0	PUD_SD1_DAT0	0	PUD_MSIOF0_RXD	1	—	0
bit24	PUD_QSPI1_MOSI/IO0	0	PUD_A3	0	PUD_D12	0	PUD_SD1_DAT1	0	PUD_MSIOF0_TXD	1	—	0
bit23	PUD_QSPI1_MISO/IO1	0	PUD_A4	0	PUD_D13	1	PUD_SD1_DAT2	0	PUD_MSIOF0_SYNC	1	—	0
bit22	PUD_QSPI1_IO2	0	PUD_A5	0	PUD_D14	1	PUD_SD1_DAT3	0	PUD_MSIOF0_SS1	1	—	0
bit21	PUD_QSPI1_IO3	0	PUD_A6	1	PUD_D15	0	PUD_SD3_CLK	0	PUD_MSIOF0_SS2	1	—	0
bit20	PUD_QSPI1_SSL	0	PUD_A7	0	PUD_PRESETOUT#	0	PUD_SD3_CMD	0	PUD_SSI_SDATA9	1	—	0
bit19	PUD_RPC_INT#	1	PUD_A8	1	—	0	PUD_SD3_DAT0	0	PUD_MLB_CLK	0	—	0

-Correction (to):

9.3.9 LSI pin pull-up/down control Register 0-5 (PUD0-5)

Table 9.10 Configuration of Registers in PUD0-5

	PUD0	Initial value	PUD1	Initial value	PUD2	Initial value	PUD3	Initial value	PUD4	Initial value	PUD5	Initial value
bit31	PUD_QSPI0_SPCLK	1	PUD_RD_WR#	1	PUD_D5	1	PUD_SD0_DAT0	0	PUD_RX1	1	PUD_USB30_PWEN	0
bit30	PUD_QSPI0_MOSI/IO0	1	PUD_EX_WAIT0	1	PUD_D6	0	PUD_SD0_DAT1	0	PUD_TX1	1	— *	1
bit29	PUD_QSPI0_MISO/IO1	1	—	0	PUD_D7	1	PUD_SD0_DAT2	0	PUD_SCK2_A	1	—	0
bit28	PUD_QSPI0_IO2	1	—	0	PUD_D8	0	PUD_SD0_DAT3	0	PUD_TX2_A	1	—	0
bit27	PUD_QSPI0_IO3	1	PUD_A0	1	PUD_D9	0	PUD_SD1_CLK	0	PUD_RX2_A	1	—	0
bit26	PUD_QSPI0_SSL	1	PUD_A1	1	PUD_D10	1	PUD_SD1_CMD	0	PUD_MSIOF0_SCK	1	—	0
bit25	PUD_QSPI1_SPCLK	1	PUD_A2	1	PUD_D11	0	PUD_SD1_DAT0	0	PUD_MSIOF0_RXD	1	—	0
bit24	PUD_QSPI1_MOSI/IO0	1	PUD_A3	0	PUD_D12	0	PUD_SD1_DAT1	0	PUD_MSIOF0_TXD	1	—	0
bit23	PUD_QSPI1_MISO/IO1	1	PUD_A4	0	PUD_D13	1	PUD_SD1_DAT2	0	PUD_MSIOF0_SYNC	1	—	0
bit22	PUD_QSPI1_IO2	1	PUD_A5	0	PUD_D14	1	PUD_SD1_DAT3	0	PUD_MSIOF0_SS1	1	—	0
bit21	PUD_QSPI1_IO3	1	PUD_A6	1	PUD_D15	0	PUD_SD3_CLK	0	PUD_MSIOF0_SS2	1	—	0
bit20	PUD_QSPI1_SSL	1	PUD_A7	0	PUD_PRESETOUT#	0	PUD_SD3_CMD	0	PUD_SSI_SDATA9	1	—	0
bit19	PUD_RPC_INT#	1	PUD_A8	1	—	0	PUD_SD3_DAT0	0	PUD_MLB_CLK	0	—	0

[Description]

Correct initial value of PUD0 register in RZ/G2E product of RZ/G 2nd Generation.

[Reason for Correction]

General error correction.

- End of Document -