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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RA*-A0014A/E	Rev.	1.00	
Title	RA2A1 Group, RA2L1 Group, RA2E1 Group, RA4M1 Group, RA4W1 Group, RA6M1 Group, RA6M2 Group, RA6M3 Group, RA6T1 Group, Note on ALeRASE command		Information Category	Technical Notification			
		Lot No.		RA2A1 Group User' Hardware Rev.1.00	al		
Applicable Product	RA2A1 Group RA2L1 Group RA2E1 Group RA4M1 Group RA4W1 Group RA6M1 Group RA6M2 Group RA6M3 Group RA6M3 Group RA6T1 Group	All	Reference Document	RA2L1 Group User' Hardware Rev.1.00 RA2E1 Group User' Hardware Rev.1.10 RA4M1 Group User Hardware Rev.1.00 RA4W1 Group User Hardware Rev.1.00 RA6M1 Group User Hardware Rev.1.00 RA6M2 Group User Hardware Rev.1.00 RA6M3 Group User Hardware Rev.1.10 RA6T1 Group User' Hardware Rev.1.00	s Manua 's Manua 's Manua 's Manua 's Manua	al al al al	

This technical update provides a cautionary note regarding ALeRASE command operation.

1. Note

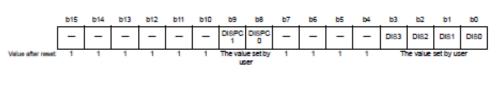
An emulator connection will be refused when OSIS bit [127] is set as 0 however the ALeRASE command will be accepted. When the ALeRASE command is executed, the User memory region and Option memory region are erased. The OSIS register value is also erased, so that the emulator can be connected again.

2. Countermeasures

When OSIS bit [127]=0, disabling acceptance of the ALeRASE command needs some additional settings as below.

User can select between two equivalent workarounds.

- A) Setting SECMPUAC (when boot swap is set, the address of SECMPCAC shifts by 2000h.)
- Please set data as 0xFEFF at SECMPUAC



Bit	Symbol	Bit name	Description	R/W
ь0	DISO	Region 0 Disable	0: Security MPU region 0 is enabled 1: Security MPU region 0 is disabled.	R
b1	DIS1	Region 1 Disable	0: Security MPU region 1 is enabled 1: Security MPU region 1 is disabled.	
b2	DIS2	Region 2 Disable	0: Security MPU region 2 is enabled 1: Security MPU region 2 is disabled.	
b3	DI83	Region 3 Disable	0: Security MPU region 3 is enabled 1: Security MPU region 3 is disabled.	
b7 to b4	-	Reserved	These bits are read as 1. When writing to flash, the write value should always be 1.	
b8	DISPCO	PC Region 0 Disable	0: Security MPU PC region 0 is enabled 1: Security MPU PC region 0 is disabled.	R

Figure 1. SECMPUAC register

• Please set 0xFFFF_FFFC at SECMPUPCS0 and set 0xFFFF_FFFF at SECMPUPCE0.

Or

B) Setting AWSC or AWS

For RA2A1, RA4M1 and RA4W1, please set AWSC bit [14] = 0.

For RA2L1, RA2E1, RA6M1, RA6M2, RA6M3 and RA6T1, please set AWS bit [15] = 0.

AWSC bit [14] or AWS bit [15] cannot be changed to 1 once it is set to 0. After clearing the AWSC or AWS bits, the access window and startup area selection options are permanently fixed and cannot be used again. In this case, the self-programming is prohibited because the startup area cannot be exchanged.