To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

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M32C/81 Group, M32C/82 Group, and M32C/83 Group
Precautions Concerning the UiC1 (i=0 to 4) Register

Classification	Concerned Products
Corrections and supplementary explanation of document √ Notes Knowhow Others	M32C/81 Group M32C/82 Group M32C/83 Group

1. Precautionary Note

The UiERE bit in the UiC1 register is set to “1” automatically (error signal output enabled) when CLKi and CTSi pins are held “H”(NOTE 1) and the SMD2 to SMD0 bits of the UiMR register are changed as follows:

- From “000_2” (serial I/O disabled) to “101_2” (UART mode, 8-bit transfer data)
- From “001_2” (clock synchronous serial I/O mode) to “100_2” (UART mode, 7-bit transfer data)
- From “001_2” (clock synchronous serial I/O mode) to “101_2” (UART mode, 8-bit transfer data)
- From “001_2” (clock synchronous serial I/O mode) to “110_2” (UART mode, 9-bit transfer data)
- From “010_2” (IIC mode) to “101_2” (UART mode, 8-bit transfer data)

If the UiERE bit in the UiMR register is set to “1” (error signal output enabled) and the PRYE bit in the UiMR register is set to “1” (parity enabled), the TxDi pin is held “L” if a parity error occurs during reception,.

NOTE 1: These conditions apply when the pin levels are held “H”, even if these pins are not used as CLKi or CTSi.

2. Countermeasures

Set the UiERE bit after setting the UiMR register.

List of Functions which Share Pins with CTSi and CLKi

	CTSi	CLKi
UART0	$P6_0$ / $\overline{CTS0}$ / $\overline{RTS0}$ / $\overline{SS0}$	$P6_1$ / CLK0
UART1	$P6_4$ / $\overline{CTS1}$ / $\overline{RTS1}$ / $\overline{SS1}$ / $OUTC2_1$ / ISCLK2	$P6_5$ / CLK1
UART2	$P7_3$ / $TA1_{IN}$ / $\overline{V}$ / $\overline{CTS2}$ / $\overline{RTS2}$ / $\overline{SS2}$ / $OUTC1_0$ / ISTxD1 / $BE1_{OUT}$	$P7_2$ / $TA1_{OUT}$ / V / CLK2
UART3	$P9_3$ / DA0 / $TB3_{IN}$ / $\overline{CTS3}$ / $\overline{RTS3}$ / $\overline{SS3}$	$P9_0$ / $TB0_{IN}$
UART4	$P9_4$ / DA1 / $TB4_{IN}$ / $\overline{CTS4}$ / $\overline{RTS4}$ / $\overline{SS4}$	$P9_5$ / ANEX0