To our customers,

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GRADE A

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M32C/80 Series
Cautions for Using DMAC

Classification

Corrections and supplementary explanation of document

✔Notes

Knowhow

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Products Effected

M32C/80 Series

1. Cautions

When using the DMAC of the M32C/80 series, if the DCTi (DMAi transfer count) register of channel i is set to '1', ensure that a DMA request for channel i is not generated when the DMA of the channel i is being enabled (see Note 1).

If a DMA request for channel i is generated when the DMA is being enabled, the following behavior may occur:

(1) An interrupt request is not generated after the completion of the channel i DMA transfer (however, the DMA transfer is performed).
(2) If a DMA request for channel i and a DMA request for another channel (referred to as channel j) are generated simultaneously when the DMA of the channel i is being enabled, an interrupt request will be generated for channel j but not for channel i after the completion of the channel i DMA transfer (however, all DMA transfers are performed).

Note 1: "Enabling DMA" means changing the MDi1 and MDi0 (channel i transfer mode select) bits (i=0 to 3) of the DMD0 and DMD1(DMA mode registers 0 and 1) are changed from '00_2' to '01_2' or '11_2'.

2. Countermeasures

When setting the DCTi register to other than '1', no countermeasure is required.
Even if the DCTi register is set to '1', if none of DMA interrupts is used, then no countermeasure is required.

Other than those above, follow the procedures described below for starting and after completing a DMA transfer.

[Recommended procedure for starting a DMA transfer]

• When writing to the DMiSL (DMAi request cause select) register including overwriting the same value to the DMiSL register;

(1) Set the MDi1 and MDi0 bits of the DMD0 and DMD1 registers to '00$_2$' (DMA disabled).

(2) Set up the peripheral used as the source of the DMA transfer. However, the peripheral should remain disabled at this time. For example, if using UART0 transmit, disable UART0 transmit.

(3) Set the DMiSL register. At this time, write a '1' to the DRQ (DMA request) bit of the DMiSL register (see Note 2).

(4) Set the following SFR registers:

- DSAi (DMAiSFR address) register
- DRAi (DMAi memory address reload) register
- DMAi (DMAi memory address) register
- DRCi (DMAi transfer count reload) register
- DCTi (DMAi transfer count) register

(5) Set the MDi1 and MDi0 bits of the DMD0 and DMD1 registers to '01$_2$' (single transfer) or '11$_2$' (repeat transfer).

(6) Enable the peripheral used as the source of the DMA transfer. For example, if using UART0 transmit, enable UART0 transmit.

Note 2: Do not write a '0' to the DRQ bit of the DMiSL register. (It is not necessary to write a '0' to the DRQ bit in your program for the M32C/80 series).

• When not writing to the DMiSL register;

(1) Set MDi1 and MDi0 bits of the DMD0 and DMD1 registers to '00$_2$' (DMA disabled).

(2) Set up the peripheral used as the source of the DMA transfer. However, the peripheral should remain disabled at this time. For example, if using UART0 transmit, disable UART0 transmit.

(3) Set up the following SFR registers:

- DSAi (DMAiSFR address) register
- DRAi (DMAi memory address reload) register
- DMAi (DMAi memory address) register
- DRCi (DMAi transfer count reload) register
- DCTi (DMAi transfer count) register

(4) Set the MDi1 and MDi0 bits of the DMD0 and DMD1 registers to '01$_2$' (single transfer) or '11$_2$' (repeat transfer).

(5) Enable the peripheral used as the source of the DMA transfer. For example, if using UART0 transmit, enable UART0 transmit.

[Recommended procedure after completing a DMA transfer]

(1) Disable the peripheral used as the source of the DMA transfer to prevent generating a DMA request.

(2) Set MDi1 and MDi0 bits of the DMD0 and DMD1 registers to '00$_2$' (DMA disabled).