To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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RENESAS TECHNICAL UPDATE

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Product Category	MPU & MCU		Document No.	TN-16C-A177A/E	Rev.	1.00
Title	M16C/65, M16C/64A Groups Note on Starting the PLL Clock and 40 MHz On-Chip Oscillator Clock		Information Category	Technical Notification		
Applicable Products	M16C/65, M16C/64A Groups R5F3650ENFA/FB, R5F3650EDFA/FB, R5F36506NFA/FB, R5F36506DFA/FB, R5F364AENFA/FB, R5F364AEDFA/FB, R5F364A6NFA/FB, R5F364A6DFA/FB	Lot No. —	Reference Documents			

The voltage detector and 125 kHz on-chip oscillator clock may be affected when starting oscillation of the PLL clock or 40 MHz on-chip oscillator clock.

1. Starting the PLL Clock

1.1 Notes

1.1.1 When Using Voltage Detector 0, 1, or 2

When changing the PLC07 bit in the PLC0 register from 0 (PLL off) to 1 (PLL on) while any bit from VC25 to VC27 in the VCR2 register is 1 (voltage detector 0, 1, or 2 enabled), the voltage detector may detect the voltage at an incorrect level. Therefore, a voltage detector 0, 1, or 2 reset/interrupt may be generated at a voltage outside the range specified in Electrical Characteristics.

1.1.2 When Using 125 kHz On-chip Oscillator Mode or 125 kHz On-chip Oscillator Low Power Mode

When changing the PLC07 bit from 0 to 1, the MCU may malfunction.

1.1.3 When Selecting fOCO-S as the Count Source for Timer A, Timer B, or the Watchdog Timer

When changing the PLC07 bit from 0 to 1, the fOCO-S cycle may become inaccurate causing the miscount.

1.2 Countermeasures

1.2.1 When Using Voltage Detector 0, 1, or 2

Do not change the PLC07 bit from 0 to 1 when any bit from VC25 to VC27 in the VCR2 register is 1.

To change the PLC07 bit from 0 to 1 while using a voltage detector or power-on reset (1), use the following procedure:

(1) Set bits VC25 to VC27 to 0 (voltage detector off).
(2) Change the PLC07 bit from 0 to 1.
(3) Wait for 1 ms.
(4) Change the bit from VC25 to VC27 that was originally 1, back to 1 (voltage detector on).

Note:
1. To use the power-on reset, the LVDAS bit in address OFS should be 0 (voltage monitor 0 reset enabled after hardware reset). Therefore, the VC25 bit is 1.

1.2.2 When Using 125 kHz On-chip Oscillator Mode or 125 kHz On-chip Oscillator Low Power Mode

Change the PLC07 bit from 0 to 1 while dividing the clock by 8 or 16 (selectable by setting the CM06 bit in the CM0 register and bits CM17 to CM16 in the CM1 register).

1.2.3 Count Source for Timer A and Timer B

When using PLL clock, do not use fOCO-S as the count source for timer A and timer B.

1.2.4 When Using fOCO-S as the Count Source for the Watchdog Timer

Change the PLC07 bit from 0 to 1 using the following procedure:

(1) Write 00h to the WDTR register, then write FFh (watchdog timer refresh).
(2) Change the PLC07 bit from 0 to 1.
(3) Wait for 1 ms.
(4) Write 00h to the WDTR register, then write FFh (watchdog timer refresh).

2. Starting the 40 MHz On-chip Oscillator Clock

2.1 Notes

2.1.1 When Using Voltage Detector 0, 1, or 2

When changing the FRA00 bit in the FRA0 register from 0 (40 MHz on-chip oscillator off) to 1 (40 MHz on-chip oscillator on) while any bit from VC25 to VC27 in the VCR2 register is 1 (voltage detector 0, 1, or 2 enabled), the voltage detector may detect the voltage at an incorrect level. Therefore, a voltage detector 0, 1, or 2 reset/interrupt may be generated at a voltage outside the range specified in Electrical Characteristics.

2.1.2 When Using 125 kHz On-chip Oscillator Mode or 125 kHz On-chip Oscillator Low Power Mode

When changing the FRA00 bit from 0 to 1, the MCU may malfunction.

2.1.3 When Selecting fOCO-S as the Count Source for Timer A, Timer B, or the Watchdog Timer

fOCO-S cycle may become inaccurate causing the miscount by changing the FRA00 bit from 0 to 1.

2.1.4 When Returning from Stop Mode to 40 MHz On-chip Oscillator Mode

The same problem as described in section 2.1.1 may occur.

2.2 Countermeasures

2.2.1 When Using Voltage Detector 0, 1, or 2

Do not change the FRA00 bit from 0 to 1 when any bit from VC25 to VC27 in the VCR2 register is 1.

To change the FRA00 bit from 0 to 1 while using a voltage detector or power-on reset (1), use the following procedure:

(1) Set bits VC25 to VC27 to 0 (voltage detector off).
(2) Change the FRA00 bit from 0 to 1.
(3) Wait for 1 ms.
(4) Change the bit from VC25 to VC27 that was originally 1, back to 1 (voltage detector on).

Note:

1. To use the power-on reset, the LVDAS bit in address OFS should be 0 (voltage monitor 0 reset enabled after hardware reset). Therefore, the VC25 bit is 1.

2.2.2 When Using 125 kHz On-chip Oscillator Mode or 125 kHz On-chip Oscillator Low Power Mode

Change the FRA00 bit from 0 to 1 while dividing the clock by 8 or 16 (selectable by setting the CM06 bit in the CM0 register and bits CM17 to CM16 in the CM1 register).

2.2.3 Count Source for Timer A and Timer B

When using 40 MHz on-chip oscillator clock, do not use fOCO-S as the count source for timer A and timer B.

2.2.4 When Selecting fOCO-S as the Count Source for the Watchdog Timer

Change the FRA00 bit from 0 to 1 using the following procedure:

(1) Write 00h to the WDTR register, then write FFh (watchdog timer refresh).
(2) Change the FRA00 bit from 0 to 1.
(3) Wait for 1 ms.
(4) Write 00h to the WDTR register, then write FFh (watchdog timer refresh).

2.2.5 When Returning from Stop Mode to 40 MHz On-chip Oscillator Mode

Do not use voltage detector when entering stop mode from 40 MHz on-chip oscillator mode. Also, do not enter stop mode from 40 MHz on-chip oscillator mode when using voltage detector.

3. Target MCUs

3.1 M16C/65 Group (For both “1. Starting the PLL Clock” and “2. Starting the 40 MHz On-chip Oscillator Clock”)
R5F3650ENFA, R5F3650ENFB, R5F3650EDFA, R5F3650EDFB,
R5F36506NFA, R5F36506NFB, R5F36506DFA, R5F36506DFB

3.2 M16C/64A Group (For “1. Starting the PLL Clock” only)
R5F364AENFA, R5F364AENFB, R5F364AEDFA, R5F364AEDFB
R5F364A6NFA, R5F364A6NFB, R5F364A6DFA, R5F364A6DFB