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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A013A/E	Rev.	1.00
Title	I^2C bus interface (RIIC) Precautions for stop condition issuance timing when receiving master		Information Category	Technical Notification		
Applicable Product	RX610 group RX62N, RX621 group RX62T group RX630 group RX63N, RX631 group	Lot No. All lots	Reference Document	RX610 group RX62N, RX621 group RX62T group RX630 group RX63N, RX631 group User's Manual, Hardware section		

With I^2C bus interface (RIIC), one clock cycle may be inserted between the ninth clock cycle of master reception and stop condition issuance.

When this clock affects the communication, follow the avoidance flow indicated below.

1. Conditions

(1)RX610, 62N, 621, 62T groups

・When data is read from ICDRR after the falling edge of the ninth clock of master reception and writng SP=1 are detected at the same time in the RIIC.

・After SP=1 is written, when the falling edge of the ninth clock cycle of master reception and data reading from ICDRR are detected at the same time in the RIIC.

(2)RX630, 63N, 631 groups

・While holding at low at the falling edge of the ninth clock cycle, writing SP=1 and reading data from ICDRR are performed in a row.

・When data is read from ICDRR after the falling edge of the ninth clock of master reception and writng SP=1 are detected at the same time in the RIIC.

・After SP=1 is written, when the falling edge of the ninth clock cycle of master reception and data reading from ICDRR are detected at the same time in the RIIC.

2. Phenomenon

One clock cycle is inserted between the ninth clock cycle of master reception and stop condition issuance.

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3. Avoidance Flow

One clock cycle is prevented from inserting before issuing stop condition by writing to the ICMR3.RDRFS bit and the ICMR3.ACKBT bit again when receiving master. Add the procedures marked in red indicated below to the flowchart in the user's manual. .

"xx" as in Figure xx.10 indicates the chapter of I²C of the user's manual respectively. Please refer to the "Target products and Reference" for details.

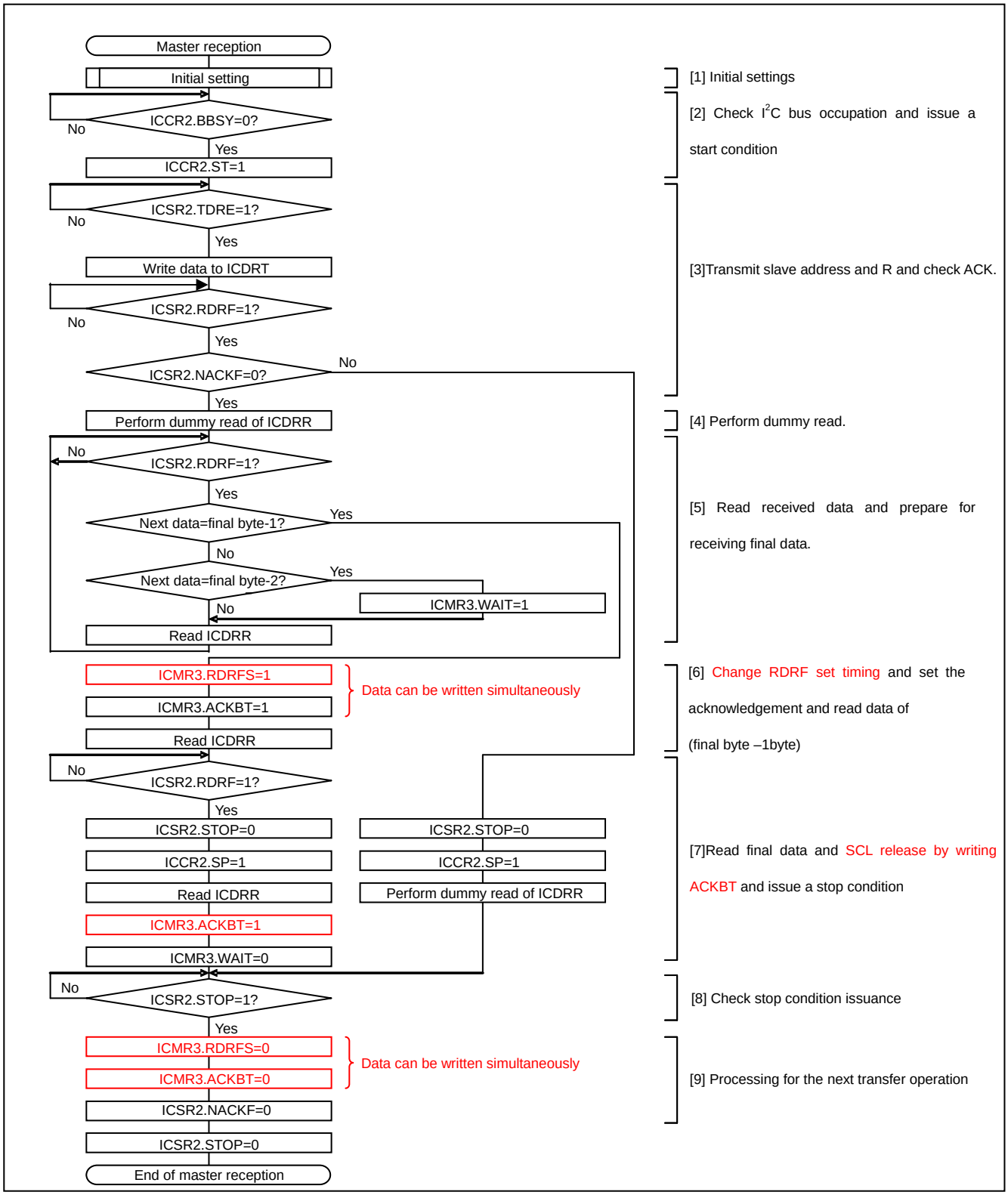

Figure xx.10 Example of Master Reception Flowchart (7-Bit Address Format)

■Target products and Reference

Group	Title	Rev.	Document No.	Chapter of I^2C
RX610 group	RX610 group User's Manual, Hardware section	Rev.1.10	R01UH0032EJ0110	22
RX62N, RX621 group	RX62N group, RX621 group User's Manual, Hardware section	Rev.1.30	R01UH0033EJ0130	31
RX62T group	RX62T group User's Manual, Hardware section	Rev.1.10	R01UH0034EJ0110	23
RX630 group	RX630 group User's Manual, Hardware section	Rev.1.12	R01UH0040EJ0112	32
RX63N, RX631group	RX63N group, RX631 group User's Manual, Hardware section	Rev.0.9	R01UH0041EJ0090	35