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RENESAS TECHNICAL UPDATE

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Title	Errata to R32C/117 Group Hardware Manual		Information Category	Technical Notification		
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This document describes corrections to the R32C/117 Group Hardware Manual, Rev. 1.00.
The corrections are indicated in red in the list below.

- Pages 18 of 601, description “Output of the clock with the same frequency as fC, f8, or f32” for Clock output in Table 1.13 is corrected as follows:
  “Output of the clock with the same frequency as low speed clocks, f8, or f32”

- Page 33 of 601, description of register name “Group 1 Timer Measurement Prescaler Register 6/7” in Table 4.6 is corrected as follows:
  “Group 1 Time Measurement Prescaler Register 6/7”

- Page 36 of 601, description of register name “Group 0 Timer Measurement Prescaler Register 6/7” in Table 4.9 is corrected as follows:
  “Group 0 Time Measurement Prescaler Register 6/7”

- Page 40 of 601, description of register name “UART2 Transmission/Receive Mode Register” in Table 4.13 is corrected as follows:
  “UART2 Transmit/Receive Mode Register”

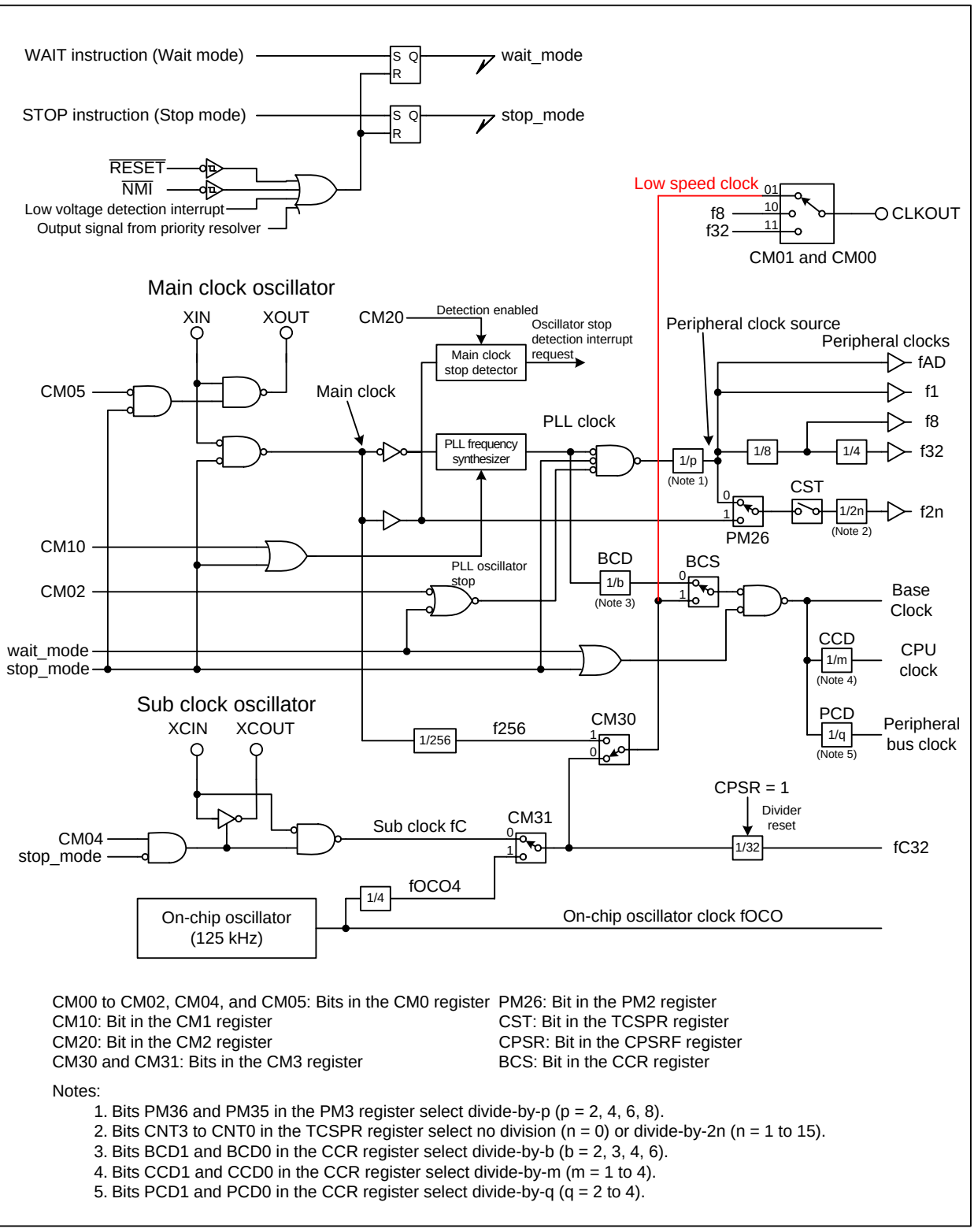
- Page 42 of 601, description of reset value “X00X X000b” for the AD0CON2 register in Table 4.15 is corrected as follows:
  “XX0X X000b”

- Page 51 of 601, description of register name “External Interrupt Source Select Register 1/0” in Table 4.24 is corrected as follows:
  “External Interrupt Request Source Select Register 1/0”

- Page 52 of 601, descriptions of reset values for registers I2CSSCR, I2CCR1, I2CCR2, I2CSR, and I2CMR in Table 4.25 are corrected as follows:
  I2CSSCR: “0001 1010b”
  I2CCR1: “0011 0000b”
  I2CCR2: “0X00 0000b”
  I2CSR: “0001 000Xb”
  I2CMR: “XXXX 0000b”

- Page 80 of 601, descriptions of address “44044h” in Figure 7.1 is corrected as follows:
  “40044h”
- Page 81 of 601, descriptions of addresses “00008000h” and “FFF80000h” in Figure 7.2 are deleted.

•Page 83 of 601, Figure 8.1 is corrected as follows:



CM00 to CM02, CM04, and CM05: Bits in the CM0 register
CM10: Bit in the CM1 register
CM20: Bit in the CM2 register
CM30 and CM31: Bits in the CM3 register
PM26: Bit in the PM2 register
CST: Bit in the TCSPR register
CPSR: Bit in the CPSRF register
BCS: Bit in the CCR register

Notes:
1. Bits PM36 and PM35 in the PM3 register select divide-by-p (p = 2, 4, 6, 8).
2. Bits CNT3 to CNT0 in the TCSPR register select no division (n = 0) or divide-by-2n (n = 1 to 15).
3. Bits BCD1 and BCD0 in the CCR register select divide-by-b (b = 2, 3, 4, 6).
4. Bits CCD1 and CCD0 in the CCR register select divide-by-m (m = 1 to 4).
5. Bits PCD1 and PCD0 in the CCR register select divide-by-q (q = 2 to 4).

Figure 8.1 Clock Generation Circuitry

•Page 84 of 601, descriptions of Notes 2 and 6 in Figure 8.2 is corrected as follows:

Note 2: “2. The divide ratios of the base clock and peripheral bus clock should not be changed simultaneously. Otherwise, the peripheral bus clock frequency may be over the operational maximum.” (“To increase the base clock frequency, the divide ratio of the peripheral bus clock should be increased before reducing the divide ratio of base clock.” is deleted)

Note 6: “To use these low speed clocks, select one of them by setting bits CM31 and CM30 in the CM3 register and then set the BCS bit to 1.”

•Page 85, 99, 106, and 109 of 601, descriptions “fC” in the function column of bits CM01 and CM00 in Figure 8.3, 8.6, Tables 8.3, 8.4, 8.5, and 8.7 are corrected as follows:
Figure 8.3: “0 1 : Output a low speed clock”
8.6: “Low speed clocks, f8, and f32 are available to be output from the CLKOUT pin.”
Table 8.3: “Output a low speed clock”
Table 8.4: “Output a low speed clock”
Table 8.5: “When a low speed clock is selected”
Table 8.7: “When a low speed clock is selected”

•Page 85 of 601, description is added as Note 8 in Figure 8.3 as follows:
“Set this bit before activating the watchdog timer.”

•Page 86 of 601, description of bit name “PLL Clock Oscillator Stop Bit” in Figure 8.4 is corrected as follows:
“PLL Oscillator Stop Bit”

•Page 86 of 601, description is added as Note 4 in Figure 8.4 as follows:
“These bits become 01b when the main clock is stopped. They should be set to 00b or 10b after the main clock is fully stabilized.”

•Page 87 of 601, description is corrected to Note 1 in Figure 8.6 as follows:
“Rewrite this register after setting the PRC27 bit in the PRCR2 register to 1 (write enabled) and while the BCS bit in the CCR register is 0 (PLL clock).”

•Page 89 of 601, description in Note 3 in Figure 8.9 is corrected as follows:
“CM05 bit in the CM0 register (main clock oscillator enabled/disabled)
CM10 bit in the CM1 register (PLL oscillator enabled/disabled)”

•Page 89 of 601, description is added as Note 5 in Figure 8.9 as follows:
“Disable all the peripheral functions that use f2n before rewriting this bit.”

•Page 90 of 601, description is added to Note 1 in Figure 8.10 as follows:
“Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting this register. Disable all the peripheral functions that use fAD, f1, f8, f32, or f2n (when the clock source is the peripheral clock source) to rewrite this register.”

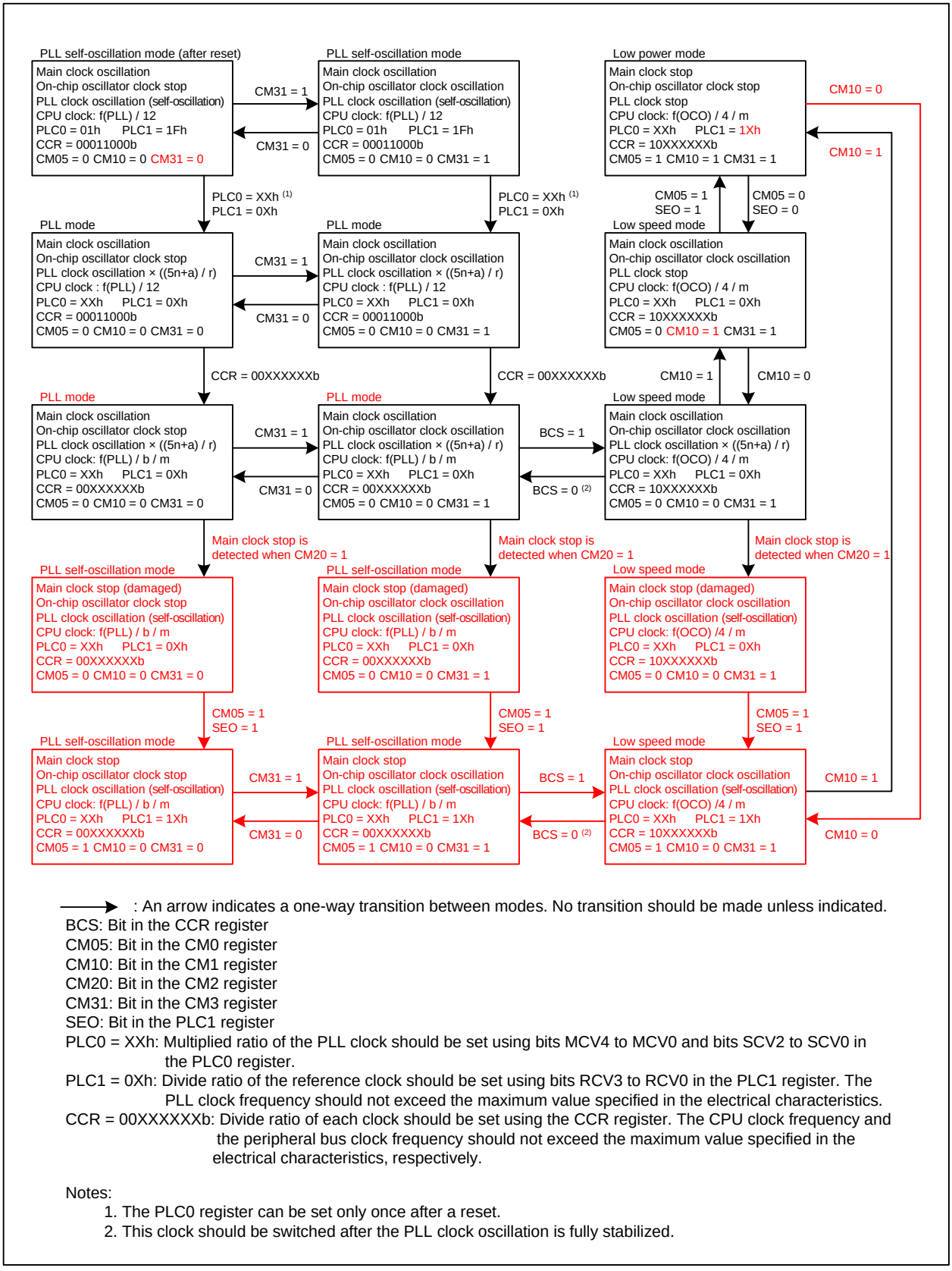
•Page 94 of 601, description for the SEO bit in Figure 8.15 is corrected as follows:

Bit Symbol	Bit Name	Function	RW
SEO	Self-Oscillating Setting Bit	0: PLL lock-in 1: Self-oscillating	RW

•Page 97 of 601, description in 8.2.1 is corrected as follows:
“When the main clock oscillator resumes running after an oscillator stop is detected, the PLL clock frequency may temporarily exceed the preset value before the PLL frequency synthesizer oscillation stabilizes. As soon as an oscillator stop is detected, the main clock oscillator should be stopped from resuming (set the CM05 bit in the CM0 register to 1) or the divide ratios of the base clock and peripheral clock source should be increased by a program. The respective divide ratio can be set by bits BCD1 and BCD0 in the CCR register and bits PM36 and PM35 in the PM3 register.”

•Page 100 of 601, description of 8.7 is corrected as follows:
“Power control contains three modes: wait mode, stop mode, and normal operating mode.
The name “normal operating mode” is used restrictively in this chapter, and it indicates all other modes except wait mode and stop mode. Figure 8.16 shows a block diagram of the state transition in normal operating mode, stop mode, and wait mode.”

•Page 103 of 601, descriptions of “CM31 = 1” in the first row and “CM10 = 0” in the second row in Figure 8.19 are corrected, and the flowchart are clarified as follows:



→ : An arrow indicates a one-way transition between modes. No transition should be made unless indicated.
BCS: Bit in the CCR register
CM05: Bit in the CM0 register
CM10: Bit in the CM1 register
CM20: Bit in the CM2 register
CM31: Bit in the CM3 register
SEO: Bit in the PLC1 register
PLC0 = XXh: Multiplied ratio of the PLL clock should be set using bits MCV4 to MCV0 and bits SCV2 to SCV0 in the PLC0 register.
PLC1 = 0Xh: Divide ratio of the reference clock should be set using bits RCV3 to RCV0 in the PLC1 register. The PLL clock frequency should not exceed the maximum value specified in the electrical characteristics.
CCR = 00XXXXXXb: Divide ratio of each clock should be set using the CCR register. The CPU clock frequency and the peripheral bus clock frequency should not exceed the maximum value specified in the electrical characteristics, respectively.

Notes:
1. The PLC0 register can be set only once after a reset.
2. This clock should be switched after the PLL clock oscillation is fully stabilized.

Figure 8.19 State Transition (when the on-chip oscillator clock is used)

(Note 3 “The CM05 bit is not set to 1 when an oscillator stop is detected through the oscillation stop detector.” is deleted from Figure 8.19)

•Page 107 of 601, description of 8.7.2.4 is corrected as follows:

"Wait mode is exited by the hardware reset, an NMI, or peripheral interrupts assigned to software interrupt numbers from 0 to 63.

To exit wait mode by either the hardware reset or an NMI, without using peripheral interrupts, bits ILVL2 to ILVL0 for the peripheral interrupts should be set to 000b (interrupt disabled) before executing the WAIT instruction.

The CM02 bit setting in the CM0 register affects the peripheral interrupts. When the CM02 bit is set to 0 (peripheral clock source not stopped in wait mode), peripheral interrupts for software interrupt numbers from 0 to 63 can be used to exit wait mode. When this bit is set to 1 (peripheral clock source stopped in wait mode), peripheral functions operated using clocks (f1, f8, f32, f2n whose clock source is the peripheral clock source, and fAD) generated by the peripheral clock source stop operating. Therefore, the peripheral interrupts cannot be used to exit wait mode. However, peripheral functions operated using clocks which are independent from the peripheral clock source (fC32, external clock, and f2n whose clock source is the main clock) do not stop operating. Thus, interrupts generated by peripheral functions and assigned to software interrupt numbers from 0 to 63 can be used to exit wait mode.

The CPU clock used when exiting wait mode by the peripheral interrupts or an NMI is the same clock used when the WAIT instruction is executed.

Table 8.6 lists interrupts to be used to exit wait mode and usage conditions."

•Page 107 of 601, description of Note 1 of Table 8.6 is added as follows:

"INT6 to INT8 are available in the intelligent I/O interrupt only."

•Page 108 of 601, description of 8.7.3 is corrected as follows:

"In stop mode, all of the clocks, except for those that are protected, stop running."

•Page 109 of 601, description in line 1 of 8.7.3.3 is corrected as follows:

"Stop mode is exited by the hardware reset, an NMI, low voltage detection interrupt, or peripheral interrupts assigned to software interrupt numbers from 0 to 63."

•Page 109 of 601, description is added to Table 8.8 as follows:

External interrupt	INT6 to INT8 are available when intelligent I/O interrupt is used

•Page 116 and 117 of 601, description of Note 2 "This register should not be set in single-chip mode." in Figures 9.4 to 9.6 is deleted.

•Page 123 of 601, description of function of P4_0 to P4_3 for multiplexed bus only in Table 9.2 is corrected as follows:

"I/O ports" ("A16 to A19 or" is deleted.)

•Page 131 of 601, Figure 9.15 is corrected as follows:

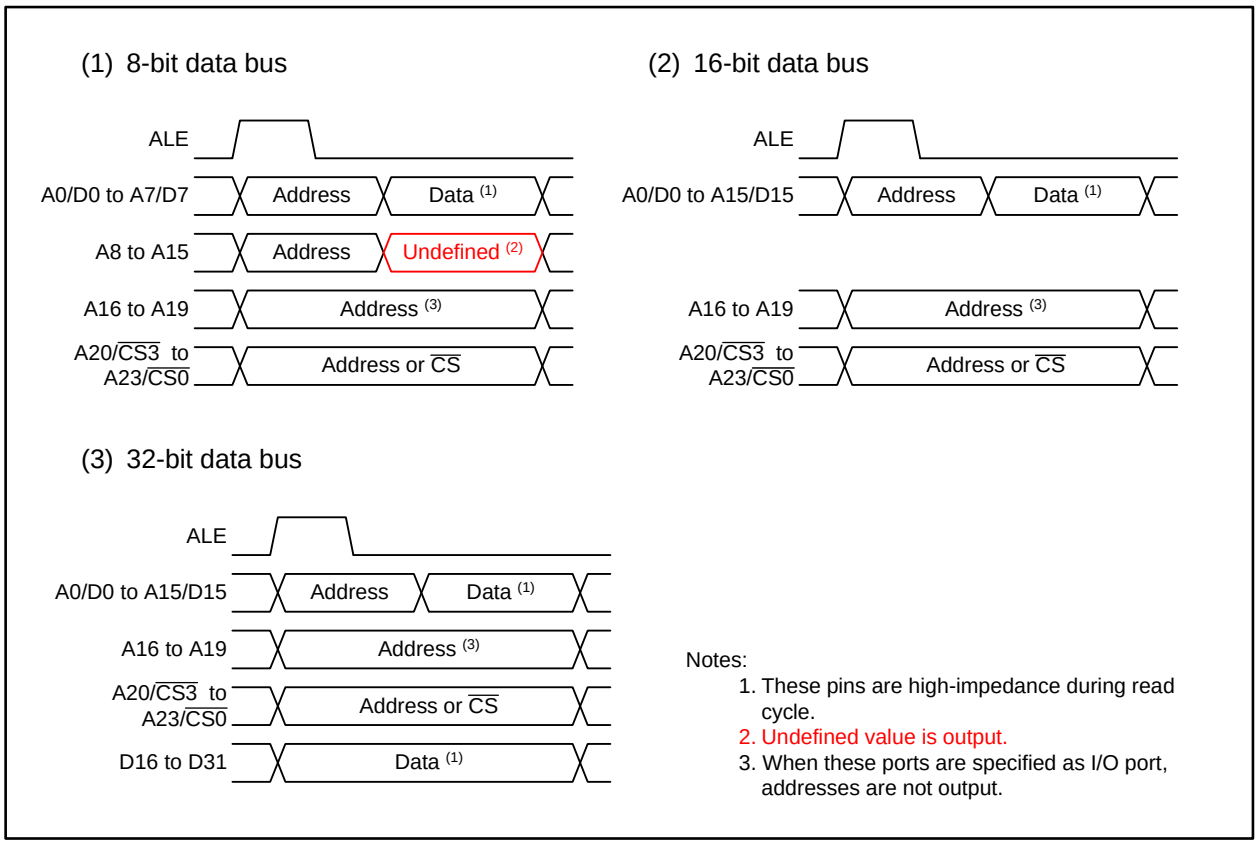


Figure 9.15 ALE Signal and Address Bus/Data Bus

•Page 158 of 601, Figure 11.8 is corrected as follows:

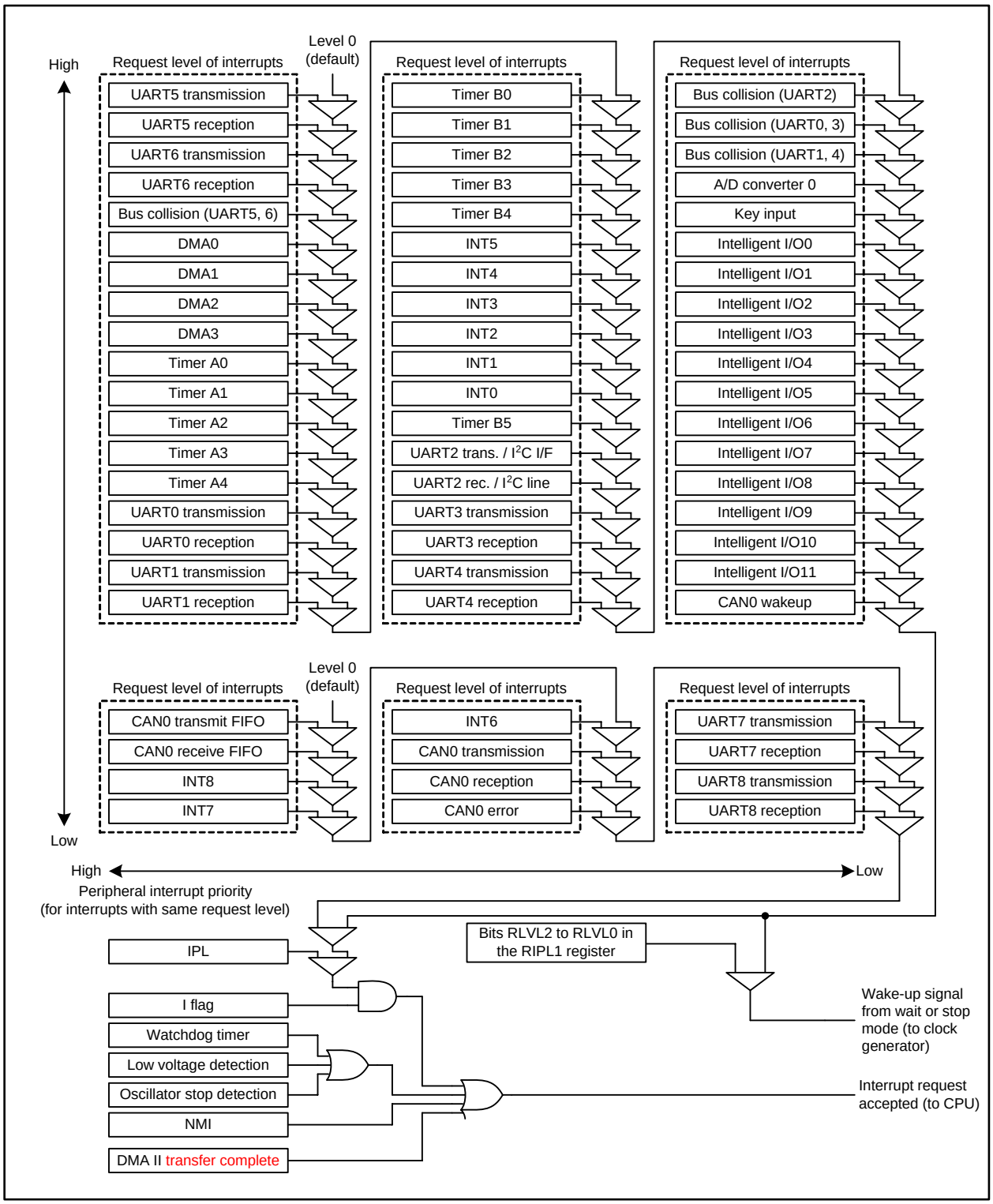


Figure 11.8 Priority Resolver

(Description “Bits RLVL2 to RLVL0 in the RIPL2 register” and associated signal lines are deleted from Figure 11.8)

•Page 163 of 601, descriptions for b0 and Note 3 in Figure 11.13 are corrected as follows:

b0: “No register bit; this bit is read as 1” (“should be written with 0 and” is deleted)

Note 3: “When this bit is function-assigned, it can be set to 0 only. It should not be set to 1. To set to 0, either the AND or BCLR instruction should be used; when the bit is not function-assigned, that is, reserved, it should be set to 0.”

•Page 165 of 601, description of the third bullet point in 11.14.3 is corrected as follows:
"The interrupt input signals to pins $\overline{INT6}$ to $\overline{INT8}$ are also connected to bits INT6R to INT8R in registers IIO9IR to IIO11IR. Therefore, these input signals, when assigned to the intelligent I/O, can be used as a source for exiting wait mode or stop mode. Note that these signals are enabled only on the falling edge and not affected by the following bit settings: bits POL and LVS in the INTiIC register (i = 0 to 8), IFSR0i bit (i = 0 to 5) in the IFSR0 register, and the IFSR1j bit (j = i - 6; i = 6 to 8) in the IFSR1 register."

•Page 167 of 601, description is added as Note 1 in Figure 12.2 as follows:
"Set this bit before activating the watchdog timer."

•Page 188 of 601, descriptions of addresses "001FFFFFh", "00200000h", and "00000000h" in 14.3.1 are corrected as follows:
"Likewise, when SADR or DADR exceeds 01FFFFFFh, it must become 02000000h, but an actual transfer is performed for FE000000h."

•Page 196 of 601, Figure 16.2 is corrected as follows:

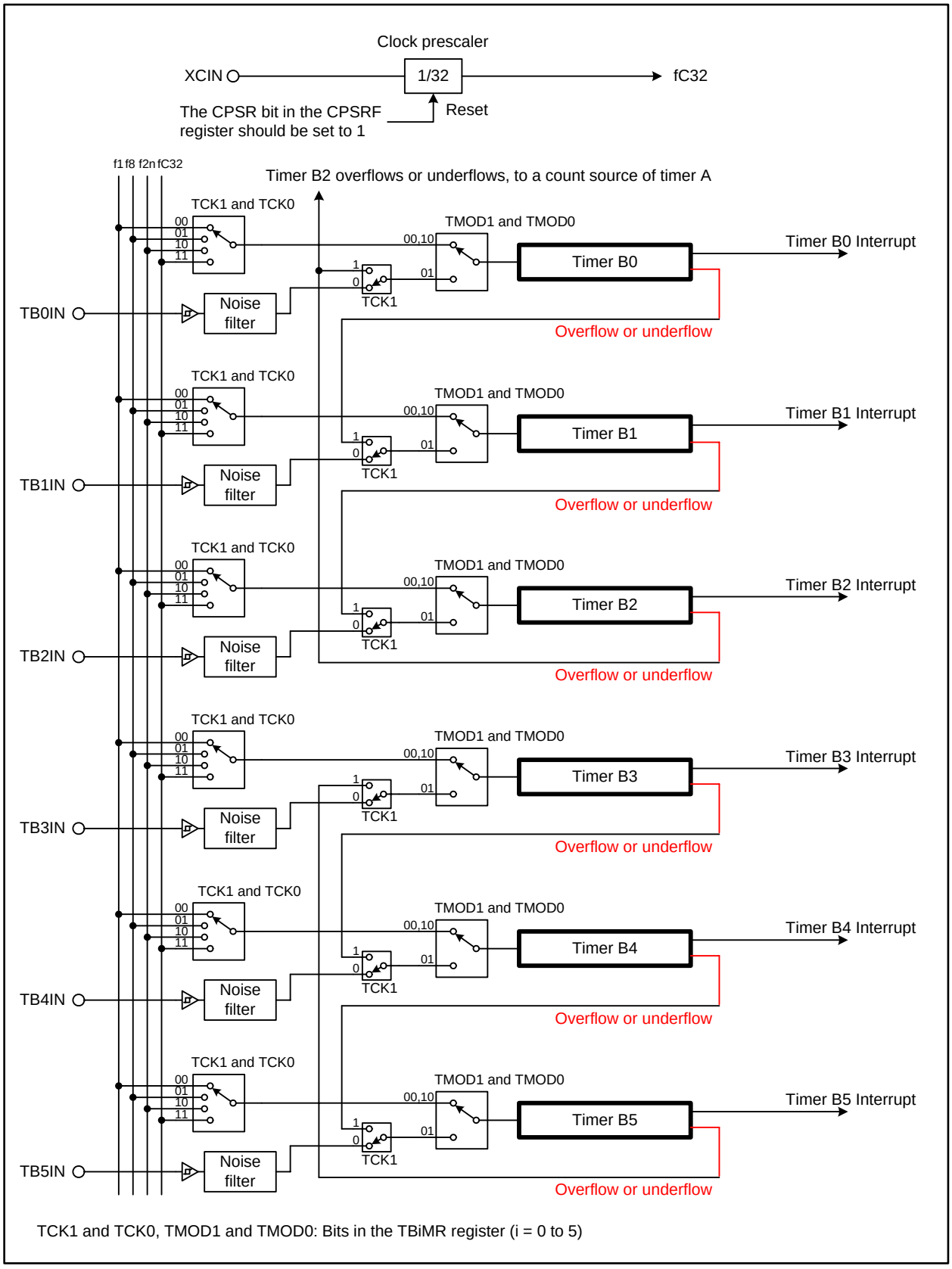


Figure 16.2 Timer B Configuration

- Page 231 and 237 of 601, descriptions of functions of the INV13 bit in Figure 17.3 and the PWCON bit in Figure 17.9 are corrected as follows:
  INV13: "0: Timer A1 reload control signal is 0
  1: Timer A1 reload control signal is 1"
  PWCON: "1: The underflow of timer B2 when the reload control signal for timer A1 is 0"

- Page 236 of 601, descriptions of functions of bits MR2 and MR3 in Figure 17.8 are corrected as follows:
  MR2: "No register bit; should be written with 0 and read as undefined value"
  MR3: "Disabled in the three-phase motor control timers. Should be written with 0 and read as undefined value"

- Page 245 of 601, descriptions "overflows" and "overflow" in 17.6.2 are corrected as follows:
  "Do not write to the TAi1 register (i = 1, 2, 4) in the timing that timer B2 underflows. Before writing to the TAi1 register, read the TB2 register to verify that sufficient time is left until timer B2 underflows. Then, immediately write to the TAi1 register so that no interrupt handler is performed during this write procedure. If the TB2 register indicates little time is left until the underflow, write to the TAi1 register after timer B2 underflows."

- Page 250 of 601, description "0 1 0 : I^2C mode" in the Function column of bits SMD2 to SMD0 in Figure 18.4 is deleted.

- Page 258 and 286 of 601, descriptions "STARREQ" in Note 3 of Figure 18.13 and 18.3.2 are corrected as follows:
  Figure 18.13: "The STSPSEL bit should be set to 1 after setting the STAREQ, RSTAREQ, or STPREQ bit to 1."
  18.3.2: "The start condition, restart condition, and stop condition are generated by bits STAREQ, RSTAREQ, and STPREQ in the UiSMR4 register (i = 0 to 6), respectively."

- Page 273 of 601, description "SUM0" in the Bits column of the UiRB register in Table 18.7 is corrected as follows:
  "OER, FER, PER, and SUM"

- Page 278 and 279 of 601, descriptions "Transmit/receive clock" in Figures 18.29 and 18.30 are corrected as follows:
  "CLKi"

- Page 303 of 601, description "To set the DUS bit to 1" in Note 5 of Figure 19.5 is corrected as follows:
  "To transfer converted results by DMA, configure the DMAC."

- Page 320 of 601, description "CRC_CCITT" in line 2 of Chapter 21 is corrected as follows:
  "A generator polynomial of CRC-CCIT ($X^{16} + X^{12} + X^5 + 1$) generates a CRC."

- Page 328 and 329 of 601, descriptions "Request from the $\overline{INT0}$ pin" in Figure 23.1 and "Request from the $\overline{INT1}$ pin" in Figure 23.2 are corrected as follows:
  Figure 23.1: "Request from the $\overline{INT0}$ pin or the $\overline{INT1}$ pin"
  Figure 23.2: "Request from the $\overline{INT0}$ pin or the $\overline{INT1}$ pin"

- Page 330, 339, 368, and 372 of 601, descriptions "IE_IN", "IE_OUT", "ISRxD2", and "ISTxD2" in Figure 23.3, "ISTxD2" in Figure 23.13, bit names of bits OPOL and IPOL in Figure 23.36, and "ISRX2" in Table 23.15 are corrected as follows:
  Figure 23.3: "IEIN", "IEOUT", "ISRXD2", and "ISTXD2"
  Figure 23.13: "ISTXD2"
  Figure 23.36: "ISTXD2 Output Polarity Switching Bit", and "ISRXD2 Input Polarity Switching Bit"
  Table 23.15: "ISRXD2"

•Page 333 of 601, descriptions in the function column of the RST2 bit and Note 3 in Figure 23.6 are corrected as follows:
RST: "1: A low signal input into the $\overline{INT0}$/$\overline{INT1}$ pin"
Note 3: "The base timer is reset by an input of low signal to the external interrupt input pin selected for the UDiZ signal by the IFS2 register."

•Page 335 of 601, description "bits BT0S to BT3S" in (2) of Note1 in Figure 23.8 is corrected as follows:
"Set all bits BT0S to BT2S to 0 (base timer is reset)"

•Page 342 of 601, description in the second bullet point of specification for reset conditions in Table 23.2 is corrected as follows:
"An input of low signal into the external interrupt pin as follows:
for group 0: selected using bits IFS23 and IFS22 in the IFS2 register
for group 1: selected using bits IFS27 and IFS26 in the IFS2 register"

•Page 343 of 601, description "Low signal input to the $\overline{INTi}$ pin" in Figure 23.18 is corrected as follows:
"Low signal input to the $\overline{INT0}$/$\overline{INT1}$ pin"

•Page 374 of 601, description in the Specification column of Selectable functions in Table 24.1 is corrected as follows:
"This function detects that the MSCL pin level is held high for longer than the specified time while the bus is busy"

•Page 375 of 601, description "In slave transmit/receive mode" in the Specification column of Slave-address match detector in Table 24.2 is corrected as follows:
"In slave-receive mode, this detects whether the address sent from the master device matches the slave address."

•Page 378 of 601, description of bit name "Transmit/Receive Bit Number Set Bit" in Figure 24.5 is corrected as follows:
"Transmit/Receive Bit Length Setting Bit"

•Page 380 of 601, description of "ACKCLK bit" in line 2 of 24.1.4 is corrected as follows:
"While data is being transmitted or received, only rewrite the ACKD bit."

•Page 380 of 601, description in Note 1 in Table 24.3 is corrected as follows:
"The CKS value must be set so the SCL clock frequency is 100 kHz or less in Standard-mode or 400 kHz or less in Fast-mode"

•Page 381 of 601, description of "ϕIIO" in line 2 of 24.1.4.2 is corrected as follows:
"To use the device under the Fast-mode I^2C-bus specification (up to 400 kbit/s), set ϕIIC to be 4 MHz or higher."

•Page 387 of 601, descriptions in line 2 and 3of 24.1.7.3 are corrected as follows:
"Set this bit to 0 to select the long timeout period. In this setting, the internal counter functions as a 16-bit counter. Set this bit to 1 to select the short timeout period."

•Page 395 of 601, description in line 5 of the second paragraph below Figure 24.18 is corrected as follows:
"by setting the ICE bit in the I2CCR0 register to 0 (I^2C-bus interface disabled),"

•Page 396 and 397 of 601, descriptions "VIIC" in Figures 24.19 and 24.22 are corrected as follows:
Figure 24.19: "1.5 cycles of ϕIIC"
Figure 24.22: "0.5 cycles of ϕIIC"

•Page 399 of 601, description of parameter “Successful receive interrupt” for the I2CCR1 register in Table 24.12 is corrected as follows:
“Successful data receive interrupt”

•Page 402 of 601, description for I2CCCR register in 24.7.1 is corrected as follows:
“Do not rewrite bits other than the ACKD bit during transmission or reception. Otherwise the I^2C-bus clock circuit is reset and a normal transmission or reception will not be performed as a result.”

•Page 403 of 601, descriptions “Bits to be zero” in Figures 24.25 and 24.26 are corrected as follows:
“Bits to be reset:”

•Page 403 of 601, description in Figure 24.27 is corrected as follows:
“Bits to be reset:
Bits BC2 to BC0 in the I2CCR0 register
MST bit in the I2CSR register (when arbitration lost is detected)
TRS bit in the I2CSR register (when a NACK is received in slave-transmit mode)

Bit to be set:
TRS bit in the I2CSR register (when the R/W bit of the first byte received is 1 in addressing format in slave-receive mode)”

•Page 404 of 601, description “By a program” in Figure 24.28 is corrected as follows:
“Software wait”

•Page 429 of 601, description of Note 2 “Write 0 to the RFE bit simultaneously with the RFMLF bit.” in Figure 25.11 is corrected as follows:
“When setting the RFE bit to 0, set the RFMLF bit to 0 as well.”

•Page 435 of 601, description “C0TFPCR” in 25.1.13 is corrected as follows:
“Do not write to the C0TFPCR register when the TFE bit in the C0TFCR register is 0 (transmit FIFO disabled).”

•Page 461 of 601, description “C0STR” in 25.2.4 is corrected as follows:
“Transmit mode: A CAN message is being transmitted. The CAN module may receive its own message simultaneously when self-test mode 0 (TSTM bit in the C0TCR register = 10b) or self-test mode 1 (TSTM bit = 11b) is selected.”

•Page 496 of 601, description for the IFS01 bit “1: Port P7/port P9” in Figure 26.20 is corrected as follows:
“Assign timer B input to
0: Port P6
1: Port P9”

•Page 501 and 502 of 601, descriptions of bit names “P9_1 to P9_3 Pull-Up Control Bit” in Figure 26.26 and “P14_1 to P14_3 Pull-Up Control Bit” in Figure 26.28 are corrected as follows:
Figure 26.26: “P9_0 to P9_3 Pull-Up Control Bit”
Figure 26.28: “P14_1 and P14_3 Pull-Up Control Bit”

•Page 509 of 601, Descriptions in Table 27.3 are corrected as follows:

Protection Type	Lock Bit Protection	ROM Code Protection	ID Code Protection
Operations to be protected	Erase, write	Read, write	Read, erase, write

(Deleted description “erase” from the ROM Code Protection column)

Protection deactivated by	Setting the LBD bit in the FMR register to 1 (lock bit protection disabled). Or, by erasing the blocks whose lock bits are set to 0 to permanently deactivate the protection	Erasing all blocks whose protect bits are set to 0	Inputting a proper ID code to the serial programmer

(Deleted description “by using the serial programmer” from the ROM Code Protection column)

•Page 509 of 601, description “use the serial programmer to” in line 3 of 27.2.2 is deleted.

•Page 510 of 601, description “FFFFFE8h” in line 9 of 27.2.3 is corrected as follows:
“ID7, are respectively assigned for addresses FFFFFFE8h, FFFFFFE9h, ..., and FFFFFFEEh as shown in Figure 27.2.”

•Page 513 of 601, descriptions in Table 27.5 are corrected as follows:

Restriction on software command	None	• Do not execute either the program command or the block erase command for blocks where the rewrite control programs are written to • Do not execute the enter read status register mode command • Execute the enter read lock bit status mode command in RAM • Execute the enter read protect bit status mode command in RAM

Flash memory state detection by	• Reading the FMSR0 register by a program • Executing the enter read status register mode command to read data	• Reading the FMSR0 register by a program

•Page 513 of 601, description “Figure 27.11” in the last line below Table 27.5 are corrected as follows:
“Figure 27.12”

•Page 521 and 523 of 601, descriptions in Figures 27.13, 27.14, and 28.5 are corrected as follows:

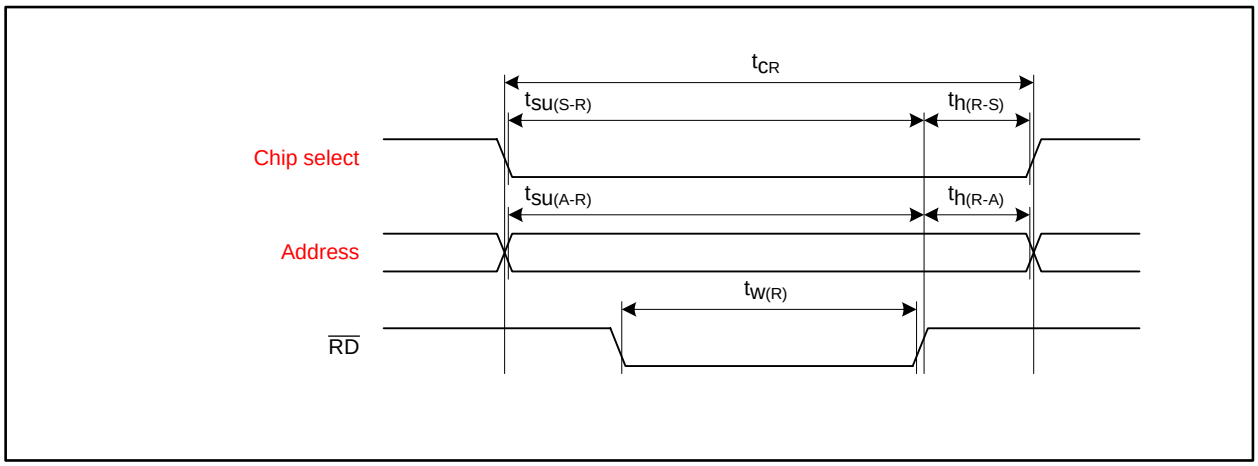


Figure 27.13 Read Timing

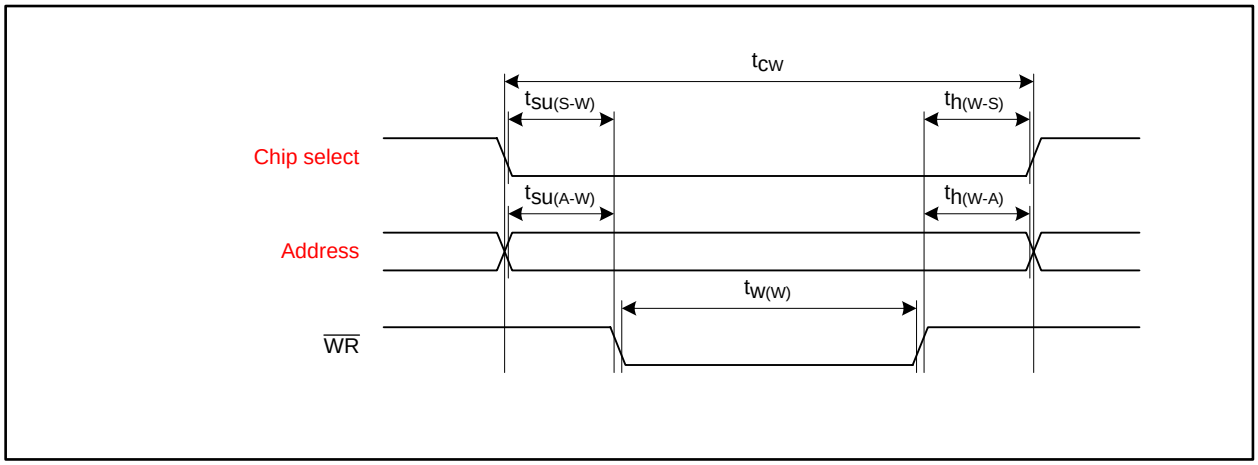


Figure 27.14 Write Timing

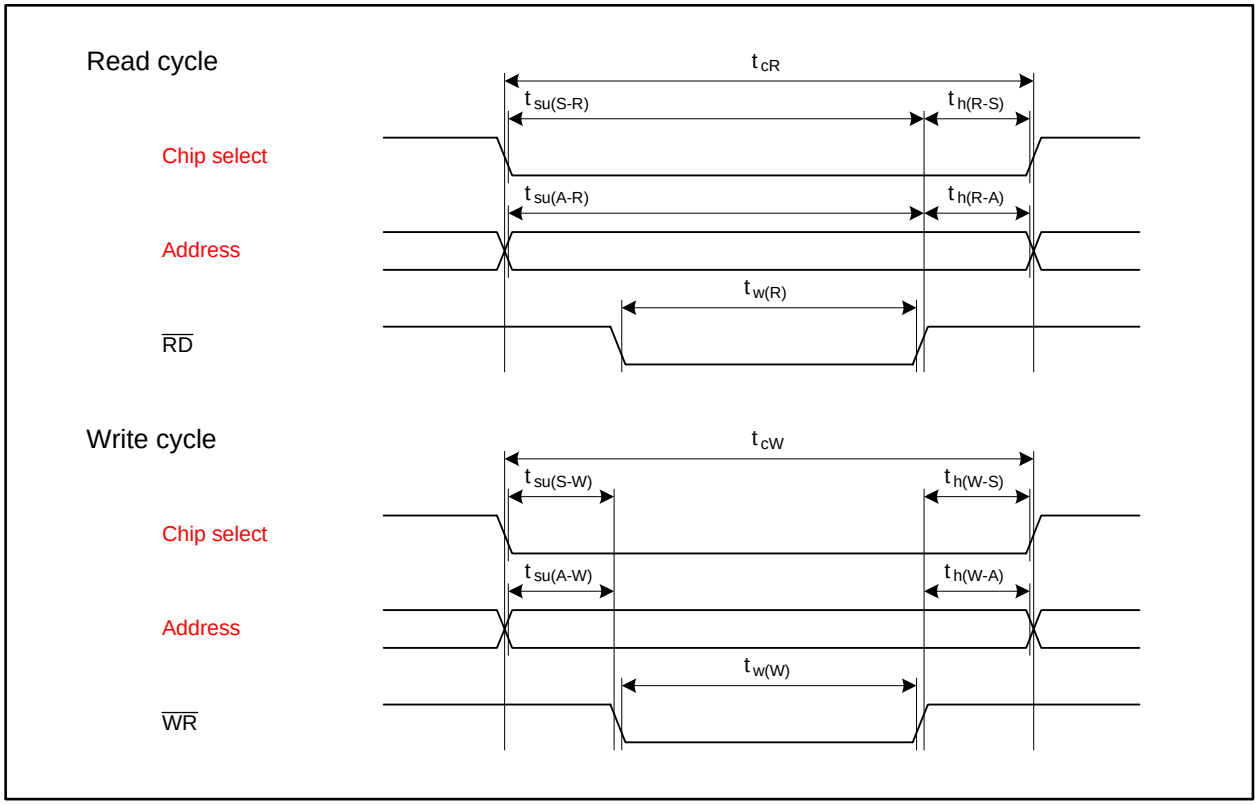


Figure 28.5 Flash Memory CPU Rewrite Mode Timing

•Page 586 of 601, description of the third bullet point in 29.5.3 is corrected as follows:

"The interrupt input signals to pins $\overline{INT6}$ to $\overline{INT8}$ are also connected to bits INT6R to INT8R in registers IIO9IR to IIO11IR. Therefore, these input signals, when assigned to the intelligent I/O, can be used as a source for exiting wait mode or stop mode. Note that these signals are enabled only on the falling edge and not affected by the following bit settings: bits POL and LVS in the INTiIC register (i = 0 to 8), IFSR0i bit (i = 0 to 5) in the IFSR0 register, and the IFSR1j bit (j = i - 6; i = 6 to 8) in the IFSR1 register."

•Page 591 of 601, descriptions "overflows" and "overflow" in 29.8.2 are corrected as follows:

"Do not write to the TAi1 register (i = 1, 2, 4) in the timing that timer B2 underflows. Before writing to the TAi1 register, read the TB2 register to verify that sufficient time is left until timer B2 underflows. Then, immediately write to the TAi1 register so that no interrupt handler is performed during this write procedure. If the TB2 register indicates little time is left until the underflow, write to the TAi1 register after timer B2 underflows."