

RENESAS TECHNICAL UPDATE

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|--------------------|---|---------|----------------------|-------------------------------------|------|------|
| Product Category | MPU & MCU | | Document No. | TN-16C-A221A/E | Rev. | 1.00 |
| Title | Descriptions Changed in the M16C/65, M16C/64A, M16C/65C, and M16C/64C Groups Manual | | Information Category | Technical Notification | | |
| Applicable Product | M16C/65, M16C/64A, M16C/65C, and M16C/64C Groups | Lot No. | Reference Document | User's Manual: Hardware (see below) | | |
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Some specifications of the M16C/65, M16C/64A, M16C/65C, and M16C/64C Groups have been changed. MCU usage and setting procedures have also been added or changed.

➔: Indicates the titles in the following manuals.

- M16C/65 Group User's Manual: Hardware Rev.2.10
- M16C/64A Group User's Manual: Hardware Rev.2.10
- M16C/65C Group User's Manual: Hardware Rev.1.10
- M16C/64C Group User's Manual: Hardware Rev.1.10

1. Bus

➔ 11.3.5.7 BCLK Output

When in memory expansion mode, the value output from the P3_0 pin is not A8, but an undefined value.

Table 11.8 Pin Functions for Each Processor Mode

| Processor Mode | Memory Expansion Mode or Microprocessor Mode | | | | Memory Expansion Mode |
|----------------------------|--|----------------|--|----------------|---|
| Bits PM05 to PM04 | 00b (separate bus) | | 01b ($\overline{CS2}$ is for multiplexed bus and the others are for separate bus) 10b ($\overline{CS1}$ is for multiplexed bus and the others are for separate bus) | | 11b (the entire \overline{CS} space is for multiplexed bus) |
| Data bus width BYTE Pin | 8 bits High | 16 bits Low | 8 bits High | 16 bits Low | 8 bits High |
| (omission) | | | | | |
| P3_0 | A8 | A8 | A8 | A8/D7 | Undefined value is output ⁽¹⁾ |
| (omission) | | | | | |

Note:

1. The change is indicated in bold text.

2. Remote Control Signal Receiver

➔ 22.3.3 Pattern Match Mode (Combined Operation of PMC0 and PMC1) and 22.5.4 Combined Operation
 When using combined operation, set same value to bits TYP1 to TYP0 in the PMC0CON1 register and bits TYP1 to TYP0 in the PMC1CON1 register.

Table 22.12 (M16C/65 and M16C/64A) Table 22.13 (M16C/65C and M16C/64C)
 Registers and Setting Values in Pattern Match Mode (Combined Operation) (1/2)

| Register | Bit | Function | |
|------------|------|--------------------------|--|
| | | PMC0 | PMC1 |
| (omission) | | | |
| PMCiCON1 | TYP0 | Select measuring object. | Select measuring object. Set the same value as PMC0. ⁽¹⁾ |
| | TYP1 | | |
| (omission) | | | |

Note:

1. The change is indicated in bold text.