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RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RX*-A184A/E	Rev.	1.00
Title	Corrections to Descriptions for the P/E Suspend Command of Flash Memory in RX610 Group		Information Category	Technical Notification		
Applicable Product	RX610 Group	Lot No.	Reference Document	RX610 Group User's Manual: Hardware Rev.1.20 (R01UH0032EJ0120)		

This document describes corrections to the descriptions for the SUSRDY bit and the flow chart of the P/E suspend command in the "ROM (Flash Memory for Code Storage)" section of RX610 Group User's Manual: Hardware.

• Page 826 of 1003

Clearing conditions of the SUSRDY bit in section 26.2.5, Flash Status Register 0 (FSTATR0) are corrected as follows.

Before Correction

[Clearing conditions]

- The FCU has accepted a P/E suspend command.
- During programming/erasure process, the FCU enters the command-locked state.

After Correction

[Clearing conditions]

- The FCU has accepted a P/E suspend command.
- During programming/erasure process, the FCU enters the command-locked state.
- When programming/erasure process has been completed.

• Page 864 of 1003

In Figure 26.19, Procedure for Programming/Erasure Suspension, a processing flow never escapes from the loop for a checking procedure if the programming/erasure processing completed before checking the SUSRDY bit.

Therefore, a timeout processing and a breaking processing when the FRDY bit is 1 are to be added.



Before correction

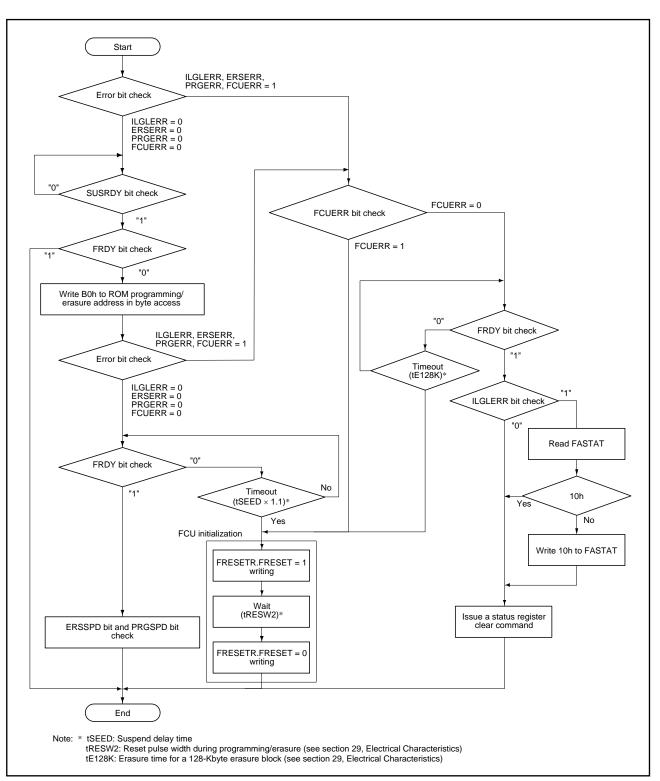


Figure 26.19 Procedure for Programming/Erasure Suspension

After correction Start ILGLERR, ERSERR, PRGERR, FCUERR = 1 Error bit check ILGLERR = 0ERSERR = 0PRGERR = 0 FCUERR = 0 "0" SUSRDY bit check "1" FRDY bit check "1" FRDY bit check No Timeout (tE128K) "0" Yes Write B0h to ROM programming/ erasure address in byte access FCUERR = 1 FCUERR bit check ILGLERR, ERSERR, PRGERR, FCUERR = 1 FCUERR = 0 Error bit check "0 ILGLERR = 0 FRDY bit check ERSERR = 0 PRGERR = 0 "1" Timeout FCUERR = 0 (tE128K)* "0" ILGLERR bit check FRDY bit check "0" "1" No Timeout (tSEED × 1.1) Read FASTAT Yes FCU initialization 10h FRESETR.FRESET = 1 Yes writing No Write 10h to FASTAT Wait (tRESW2)3 ERSSPD bit and PRGSPD bit FRESETR.FRESET = 0Issue a status register check

Figure 26.19 Procedure for Programming/Erasure Suspension

writing

tRESW2: Reset pulse width during programming/erasure (see section 29, Electrical Characteristics) tE128K: Erasure time for a 128-Kbyte erasure block (see section 29, Electrical Characteristics)

End of document

End

Note: * tSEED: Suspend delay time

clear command