Date: Oct. 27, 2015

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A033B/E	Rev.	2.00
Title	Correction for Incorrect Description Notice RL78/L1C Descriptions in the User's Manual: Hardware Rev. 2.00 Changed		Information Category	Technical Notification		
Applicable Product	RL78/L1C Group	Lot No. All lots	Reference Document	RL78/L1C User's Manual: Hardware Rev. 2.00 R01UH0409EJ0200 (Feb. 2014)		

This document describes misstatements found in the RL78/L1C User's Manual: Hardware Rev. 2.00 (R01UH0409EJ0200).

Corrections

Applicable Item	Applicable Page	Contents
5.2 Configuration of Clock Generator	page 170	Additional entry
5.3.2 System clock control register (CKC)	page 174	Incorrect descriptions revised
5.3.6 Peripheral enable registers 0, 1, 2 (PER0, PER1, PER2)	page 180, 181	Incorrect descriptions revised
5.3.10 PLL control register (DSCCTL)	page 187	Additional entry
5.4.5 PLL (Phase Locked Loop)	page 194	Incorrect descriptions revised
5.6.1 Example of setting high-speed on-chip oscillator	page 197	Additional entry
5.6.4 Example of setting PLL circuit	page 199	Incorrect descriptions revised
5.6.5 CPU clock status transition diagram	page 202	Incorrect descriptions revised
5.6.5 CPU clock status transition diagram Table 5 - 4 CPU Clock Transition and SFR Register Setting Examples	pages 203 to 209	Incorrect descriptions revised
5.6.5 CPU clock status transition diagram Table 5 - 11 CPU Clock Transition and SFR Register Setting Examples	page 213	Incorrect descriptions revised
5.6.6 Condition before changing CPU clock and processing after changing CPU clock	pages 216 to 217	Incorrect descriptions revised
6.3.1 Peripheral enable register 0 (PER0)	page 240	Incorrect descriptions revised
8.3.1 Peripheral enable register 0 (PER0)	page 451	Incorrect descriptions revised
8.4.1 Starting operation of real-time clock 2	page 469	Incorrect descriptions revised
12.3.1 Peripheral enable register 0 (PER0)	page 502	Incorrect descriptions revised
15.3.1 Peripheral enable register 0 (PER0)	page 591	Incorrect descriptions revised
16.3.1 Peripheral enable register 0 (PER0)	page 734	Incorrect descriptions revised
34.1 Absolute Maximum Ratings	page 1172	Incorrect descriptions revised
34.3.1 Pin characteristics	page 1175	Incorrect descriptions revised
35.1 Absolute Maximum Ratings	page 1239	Incorrect descriptions revised
35.3.1 Pin characteristics	page 1242	Incorrect descriptions revised

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
	Document No.	English	R01UH0409EJ0200	
1	3.3.4 Special function registers (SFRs) Table 3 - 8 SFR List		Pages 82 and 83	Page 4 and 5
2	6.3.3 Timer mode register mn (TMRmn) Figure 6 - 17 Format of Timer mode register mn (TMRmn) (4/4)		Page 248	Page 6
3	5.3.9 High-speed on-chip oscillator trimming register (HIOTRM)		Page 186	Page 7
4	15.5.7 SNOOZE mode function Timing Chart of SNOOZE Mode Operation (Figure 14-74. and Figure 14-76.)		Pages 663 and 665	Page 8 and 9
5	15.6.3 SNOOZE mode function		Page 688	Page 10
6	15.6.3 SNOOZE mode function Timing Chart of SNOOZE Mode Operation (Figure 15-95., Figure 15-96. and Figure 15-96.)		Pages 690, 691 and 693	Page 11 to 13
7	17.4.5.3 DTC Transfers (D0FIFO and D1FIFO Ports)		Page 895	Page 14
8	34.6.1 34.6.1 A/D converter characteristics		Page 1221	Page 15 and 16
9	34.9 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics		Page 1234	Page 17
10	35.8 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics		Page 1294	Page 18
11	8.3.4 Real-time clock control register 1 (RTCC1)		Page 457	Page 19
12	5.2 Configuration of Clock Generator		page 170	Page 20
13	5.3.2 System clock control register (CKC)		page 174	Page 21
14	5.3.6 Peripheral enable registers 0, 1, 2 (PER0, PER1, PER2)		page 180, 181	Page 22
15	5.3.10 PLL control register (DSCCTL)		page 187	Page 23
16	5.4.5 PLL (Phase Locked Loop)		page 194	Page 24
17	5.6.1 Example of setting high-speed on-chip oscillator		page 197	Pages 25
18	5.6.4 Example of setting PLL circuit		page 199	Page 26 and 27
19	5.6.5 CPU clock status transition diagram		page 202	Pages 28
20	5.6.5 CPU clock status transition diagram Table 5 - 4 CPU Clock Transition and SFR Register Setting Examples		pages 203 to 209	Page 29 to 36
21	5.6.5 CPU clock status transition diagram Table 5 - 11 CPU Clock Transition and SFR Register Setting Examples		page 213	Page 37
22	5.6.6 Condition before changing CPU clock and processing after changing CPU clock		pages 216 to 217	Page 38 and 39
23	6.3.1 Peripheral enable register 0 (PER0)		page 240	Page 40
24	8.3.1 Peripheral enable register 0 (PER0)		page 451	Page 41
25	8.4.1 Starting operation of real-time clock 2		page 469	Page 42
26	12.3.1 Peripheral enable register 0 (PER0)		page 502	Page 43
27	15.3.1 Peripheral enable register 0 (PER0)		page 591	Page 44
28	16.3.1 Peripheral enable register 0 (PER0)		page 734	Pages 45
29	34.1 Absolute Maximum Ratings		page 1172	Page 46
30	34.3.1 Pin characteristics		page 1175	Pages 47 and 48
31	35.1 Absolute Maximum Ratings		page 1239	Page 49
32	35.3.1 Pin characteristics		page 1242	Pages 50 and 51

Incorrect: Bold with underline; Correct: Gray hatched

Revision History

RL78/L1C Correction for incorrect description notice

Document Number	Issue Date	Description
TN-RL*-A033A/E	Aug. 18, 2014	First edition issued Corrections No.1 to No.10 revised
TN-RL*-A046A/E	Jul. 6 , 2015	Correction No.11 revised
TN-RL*-A033B/E	Oct. 27, 2015	Second edition issued Corrections No.12 to No.32 revised (this document)

1. **3.3.4 Special function registers (SFRs)**
   Table 3 - 7 SFR List (Page 82 and 83)

Incorrect:

Table 3-7. SFR List (1/4)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
(omitted)								
FFF10H	Serial data register 00	TXD0/ SIO00	SDR00	R/W	–	√	√	0000H
FFF11H		–			–	–		
FFF12H	Serial data register 01	RXD0	SDR01	R/W	–	√	√	0000H
FFF13H		–			–	–		
FFF14H	Serial data register 12	**TXD3**	SDR12	R/W	–	√	√	0000H
FFF15H		**SIO30**			–	–		
FFF16H	Serial data register 13	RXD3	SDR13	R/W	–	√	√	0000H
FFF17H		–			–	–		
(omitted)								

Correct:

Table 3-7. SFR List (1/4)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
(omitted)								
FFF10H	Serial data register 00	TXD0/ SIO00	SDR00	R/W	–	√	√	0000H
FFF11H		–			–	–		
FFF12H	Serial data register 01	RXD0	SDR01	R/W	–	√	√	0000H
FFF13H		–			–	–		
FFF14H	Serial data register 12	TXD3/ SIO30	SDR12	R/W	–	√	√	0000H
FFF15H					–	–		
FFF16H	Serial data register 13	RXD3	SDR13	R/W	–	√	√	0000H
FFF17H		–			–	–		
(omitted)								

Incorrect:

Table 3-7. SFR List (2/4)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
(omitted)								
FFF44H	Serial data register 02	TXD1/ SIO10	SDR02	R/W	–	√	√	0000H
FFF45H		–			–	–		
FFF46H	Serial data register 03	RXD1	SDR03	R/W	–	√	√	0000H
FFF47H		–			–	–		
FFF48H	Serial data register 10	**TXD2**	SDR10	R/W	–	√	√	0000H
FFF49H		**SIO20**			–	–		
FFF4AH	Serial data register 11	RXD2	SDR11	R/W	–	√	√	0000H
FFF4BH		–			–	–		
(omitted)								

Correct:

Table 3-7. SFR List (2/4)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
(omitted)								
FFF44H	Serial data register 02	TXD1/ SIO10	SDR02	R/W	–	√	√	0000H
FFF45H		–			–	–		
FFF46H	Serial data register 03	RXD1	SDR03	R/W	–	√	√	0000H
FFF47H		–			–	–		
FFF48H	Serial data register 10	TXD2/ SIO20	SDR10	R/W	–	√	√	0000H
FFF49H		–			–	–		
FFF4AH	Serial data register 11	RXD2	SDR11	R/W	–	√	√	0000H
FFF4BH		–			–	–		
(omitted)								

2. 6.3.3 Timer mode register mn (TMRmn)
Figure 6 - 17 Format of Timer mode register mn (TMRmn) (4/4)(p.248)

Incorrect:

Operation mode (Value set by the MDmn3 to MDmn1 bits (see the table above))	MDmn0	Setting of starting counting and interrupt
• Interval timer mode (0, 0, 0) • Capture mode (0, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode Note 2 (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated.
	1	Start trigger is valid during counting operation Note 3. **At that time, interrupt is also generated.**
• Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time interrupt is not generated.
Other than above		Setting prohibited

Correct:

Operation mode (Value set by the MDmn3 to MDmn1 bits (see the table above))	MDmn0	Setting of starting counting and interrupt
• Interval timer mode (0, 0, 0) • Capture mode (0, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode Note 2 (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated.
	1	Start trigger is valid during counting operation Note 3. At that time, interrupt is not generated.
• Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time interrupt is not generated.
Other than above		Setting prohibited

3. 5.3.9 High-speed on-chip oscillator trimming register (HIOTRM) (Page 186)

Incorrect:

5.3.9 High-speed on-chip oscillator trimming register (HIOTRM)

(omitted)

Figure 5-14. Format of High-Speed On-Chip Oscillator Trimming Register (HIOTRM)

Address: F00A0H After reset: undefined Note R/W

Symbol	7	6	5	4	3	2	1	0
HIOTRM	0	0	HIOTRM5	HIOTRM4	HIOTRM3	HIOTRM2	HIOTRM1	HIOTRM0

HIOTRM5	HIOTRM4	HIOTRM3	HIOTRM2	HIOTRM1	HIOTRM0	High-speed on-chip oscillator
0	0	0	0	0	0	Minimum speed
0	0	0	0	0	1	
0	0	0	0	1	0	
0	0	0	0	1	1	
0	0	0	1	0	0	
			•			
			•			
			•			
1	1	1	1	1	0	
1	1	1	1	1	1	Maximum speed

Note The value after reset is the value adjusted at shipment.

Remark1. The HIOTRM register can be used to adjust the high-speed on-chip oscillator clock to an accuracy within about 0.05%.

Remark2. For the usage example of the HIOTRM register, see the application note for RL78 MCU series High-speed On-chip Oscillator (HOCO) Clock Frequency Correction (R01AN0464).

Correct:

5.3.9 High-speed on-chip oscillator trimming register (HIOTRM)

(omitted)

Figure 5-14. Format of High-Speed On-Chip Oscillator Trimming Register (HIOTRM)

Address: F00A0H After reset: undefined Note R/W

Symbol	7	6	5	4	3	2	1	0
HIOTRM	0	0	HIOTRM5	HIOTRM4	HIOTRM3	HIOTRM2	HIOTRM1	HIOTRM0

HIOTRM5	HIOTRM4	HIOTRM3	HIOTRM2	HIOTRM1	HIOTRM0	High-speed on-chip oscillator
0	0	0	0	0	0	Minimum speed
0	0	0	0	0	1	
0	0	0	0	1	0	
0	0	0	0	1	1	
0	0	0	1	0	0	
			•			
			•			
			•			
1	1	1	1	1	0	
1	1	1	1	1	1	Maximum speed

Note The value after reset is the value adjusted at shipment.

Remarks 1. The HIOTRM register holds a six-bit value used to adjust the high-speed on-chip oscillator with an increment of 1 corresponding to an increase of frequency by about 0.05%.

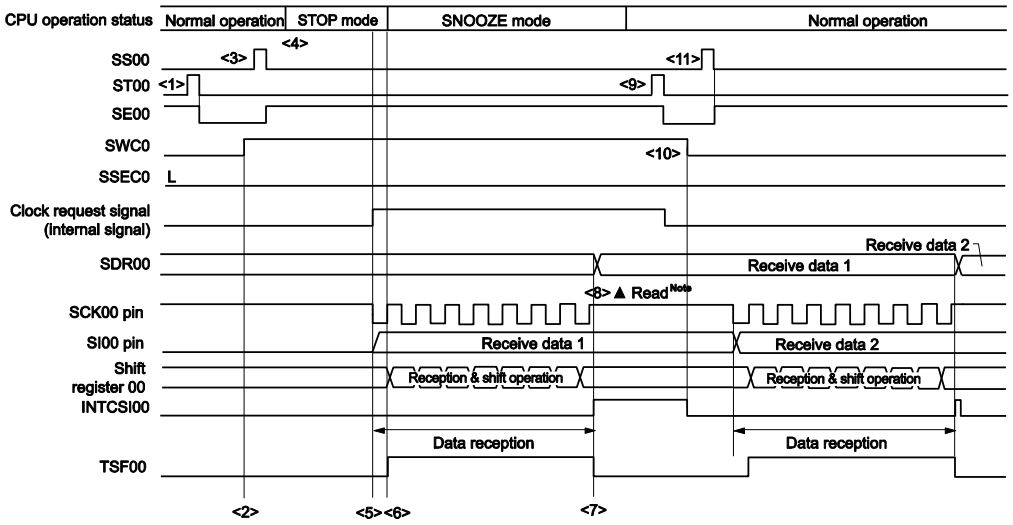
Remark 2. For the usage example of the HIOTRM register, see the application note for RL78 MCU series High-speed On-chip Oscillator (HOCO) Clock Frequency Correction (R01AN0464).

4. 15.5.7 SNOOZE mode function
Timing Chart of SNOOZE Mode Operation (Figure 15-74. and Figure 15-76.) (Pages 663 and 665)

It is correction of “CPU operation status”, “Clock request signal (internal signal)” and “TSF00” in this Figure.

Incorrect:

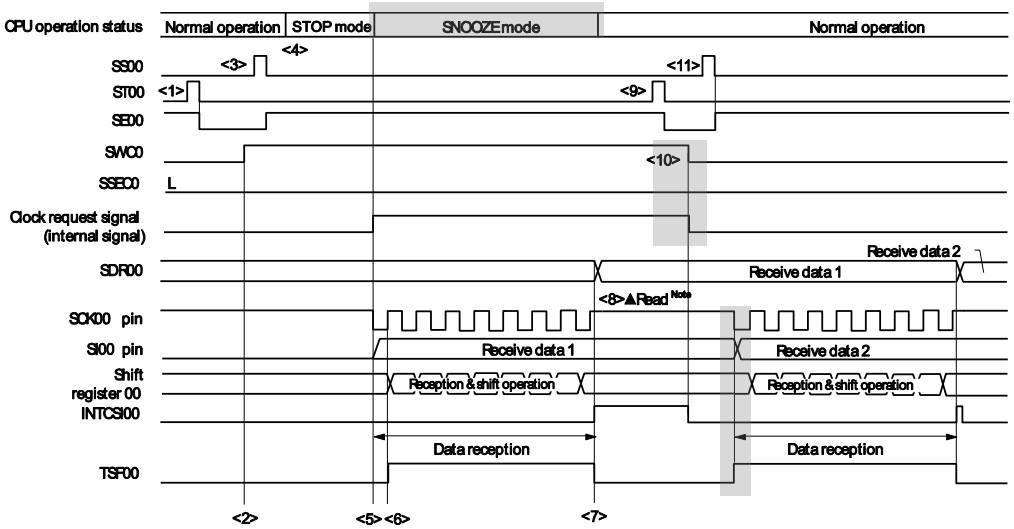
Figure 15-74. Timing Chart of SNOOZE Mode Operation (once startup)
(Type 1: DAPmn = 0, CKPmn = 0)



(omitted)

Correct:

Figure 15-74. Timing Chart of SNOOZE Mode Operation (once startup)
(Type 1: DAPmn = 0, CKPmn = 0)

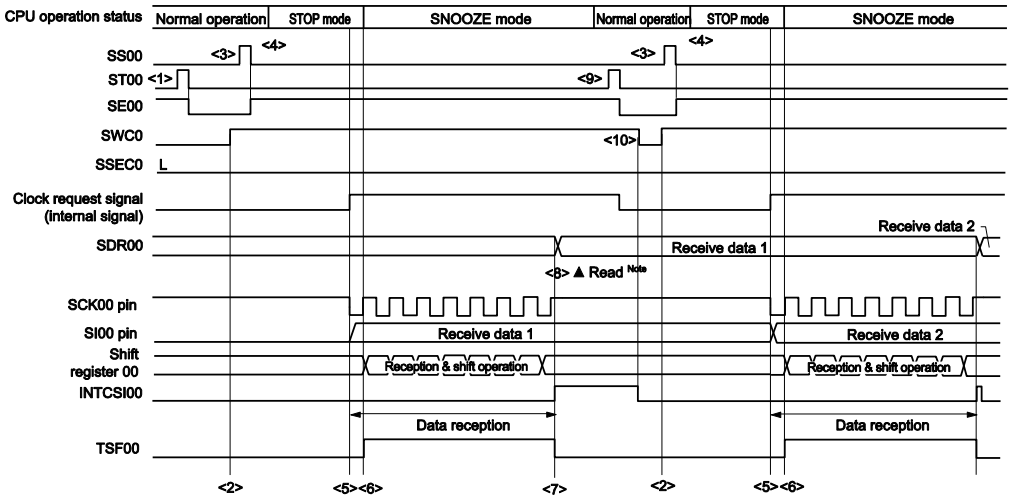


(omitted)

It is correction of “CPU operation status”, “Clock request signal (internal signal)” and “INTCSI00” in this Figure.

Incorrect:

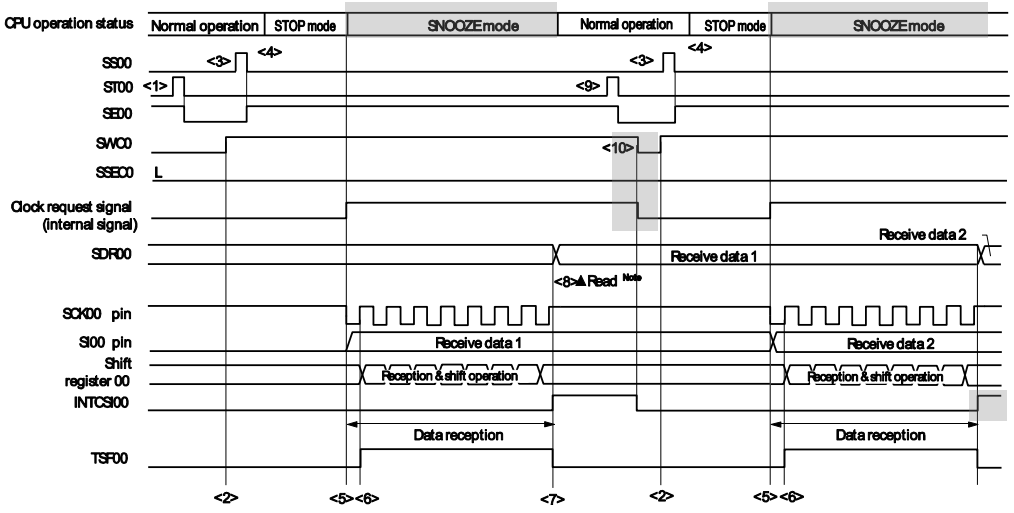
Figure 15-76. Timing Chart of SNOOZE Mode Operation (continuous startup)
(Type 1: DAPmn = 0, CKPmn = 0)



(omitted)

Correct:

Figure 15-76. Timing Chart of SNOOZE Mode Operation (continuous startup)
(Type 1: DAPmn = 0, CKPmn = 0)



(omitted)

5. 15.6.3 SNOOZE mode function (Page 688)

Incorrect:

15.6.3 SNOOZE mode function

The SNOOZE mode makes the UART perform reception operations upon RxDq pin input detection while in the STOP mode. Normally the UART stops communication in the STOP mode. However, using the SNOOZE mode enables the UART to perform reception operations without CPU operation.

(omitted)

Cautions 1. The SNOOZE mode can only be used when the high-speed on-chip oscillator clock (f_{IH}) is selected for f_{CLK}.

(omitted)

Cautions 4. If a parity error, framing error, or overrun error occurs while the SSECm bit is set to 1, the PEFmn, FEFmn, or OVFmn flag is not set and an error interrupt (INTSREq) is not generated. Therefore, when the setting of SSECm = 1 is made, clear the PEFmn, FEFmn, or OVFmn flag before setting the SWC0 bit to 1 and read the value in bits 7 to 0 (RxDq register) of the SDRm1 register.

Correct:

15.6.3 SNOOZE mode function

The SNOOZE mode makes the UART perform reception operations upon RxDq pin input detection while in the STOP mode. Normally the UART stops communication in the STOP mode. However, using the SNOOZE mode enables the UART to perform reception operations without CPU operation.

(omitted)

Cautions 1. The SNOOZE mode can only be used when the high-speed on-chip oscillator clock (f_{IH}) is selected for f_{CLK}.

(omitted)

Cautions 4. If a parity error, framing error, or overrun error occurs while the SSECm bit is set to 1, the PEFmn, FEFmn, or OVFmn flag is not set and an error interrupt (INTSREq) is not generated. Therefore, when the setting of SSECm = 1 is made, clear the PEFmn, FEFmn, or OVFmn flag before setting the SWC0 bit to 1 and read the value in bits 7 to 0 (RxDq register) of the SDRm1 register.

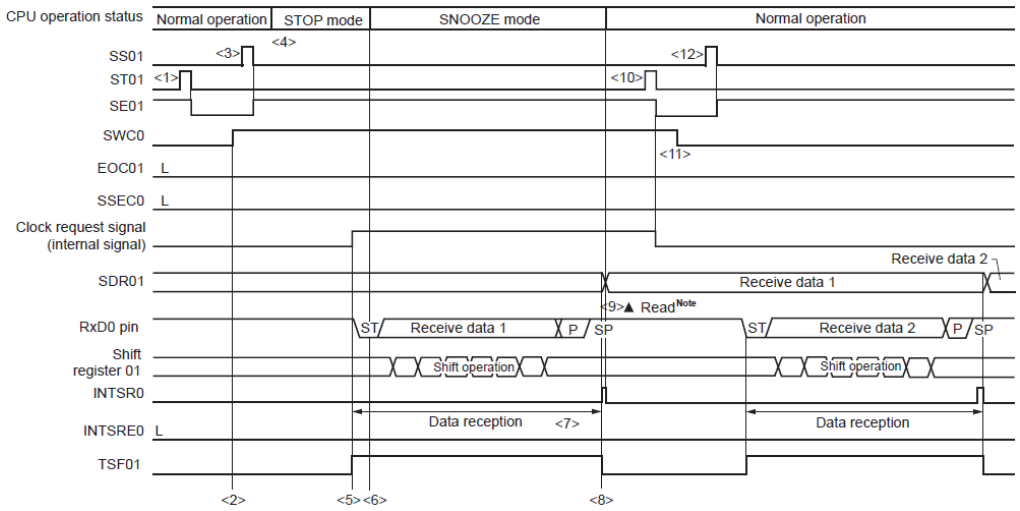
Cautions 5. The CPU shifts from the STOP mode to the SNOOZE mode on detecting the valid edge of the RxDq signal. Note, however, that transfer through the UART channel may not start and the CPU may remain in the SNOOZE mode if an input pulse on the RxDq pin is too short to be detected as a start bit. In such cases, data may not be received correctly, and this may lead to a framing error or parity error in the next UART transfer.

6. 15.6.3 SNOOZE mode function
Timing Chart of SNOOZE Mode Operation (Figure 15-95, Figure 15-96 and Figure 15-98) (Pages 690, 691 and 693)

It is correction of "CPU operation status", "Clock request signal (internal signal)", "INTSR0" and "TSF01" in this Figure.

Incorrect:

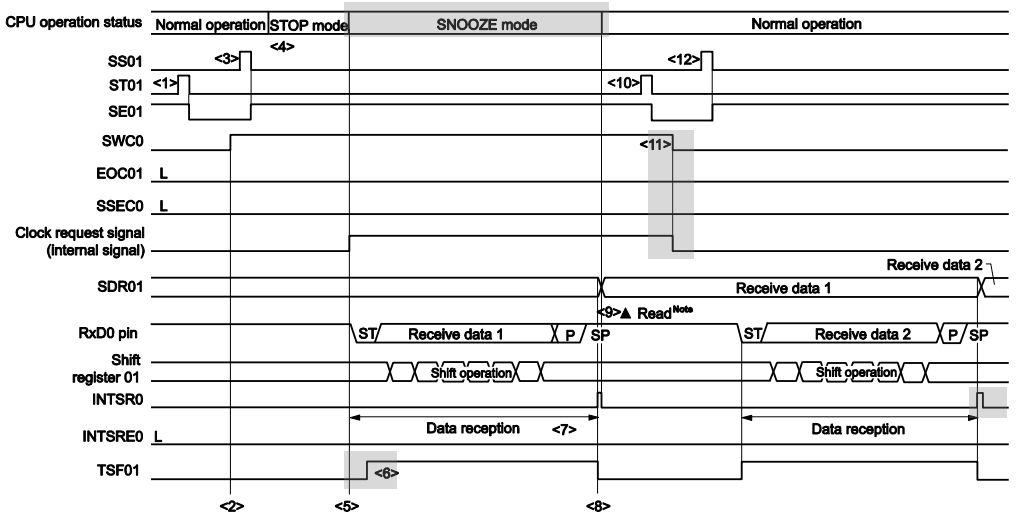
Figure 15-95. Timing Chart of SNOOZE Mode Operation (EOCm1 = 0, SSECm = 0/1)



(omitted)

Correct:

Figure 15-95. Timing Chart of SNOOZE Mode Operation (EOCm1 = 0, SSECm = 0/1)

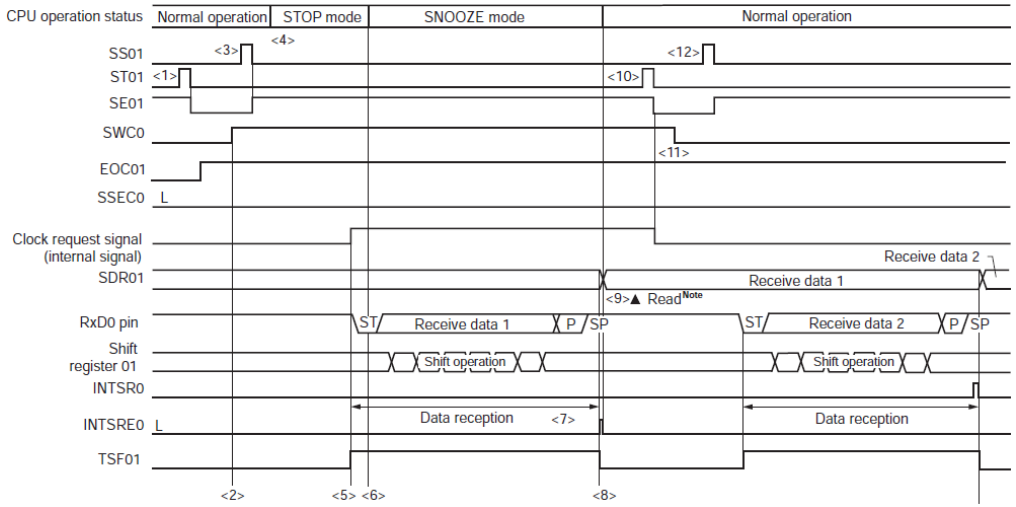


(omitted)

It is correction of “CPU operation status”, “Clock request signal (internal signal)”, “INTSR0” and “TSF01” in this Figure.

Incorrect:

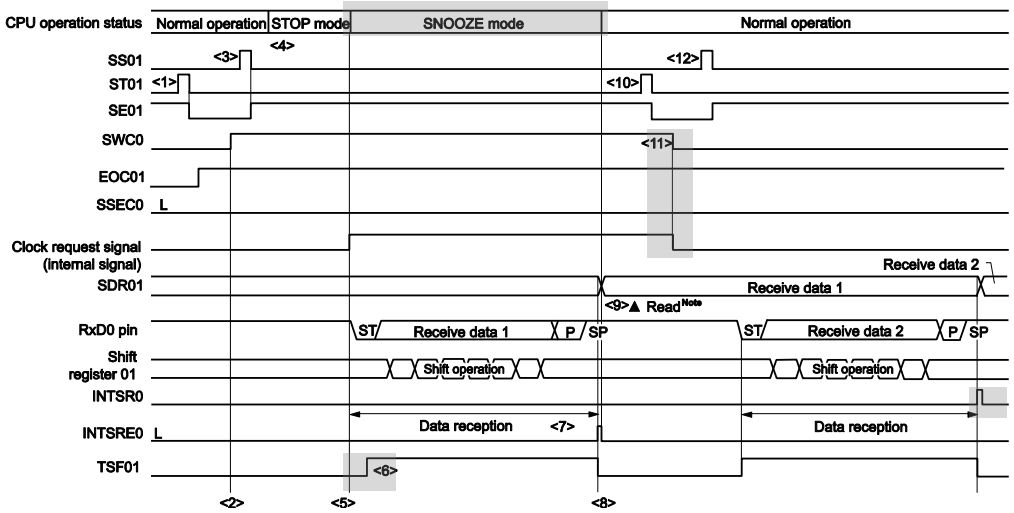
Figure 15-96. Timing Chart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 0)



(omitted)

Correct:

Figure 15-96. Timing Chart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 0)

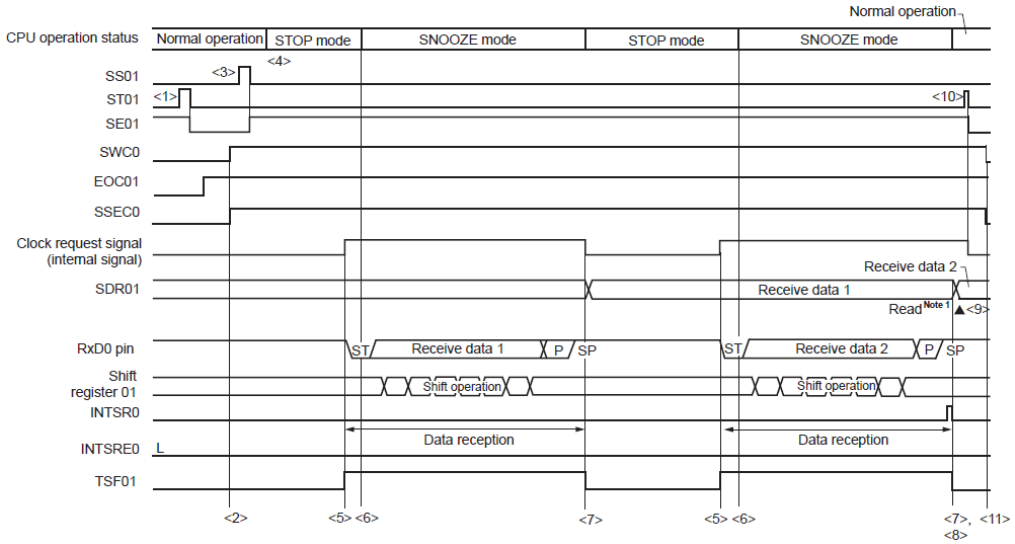


(omitted)

It is correction of “CPU operation status”, “Clock request signal (internal signal)”, “INTSR0” and “TSF01” in this Figure.

Incorrect:

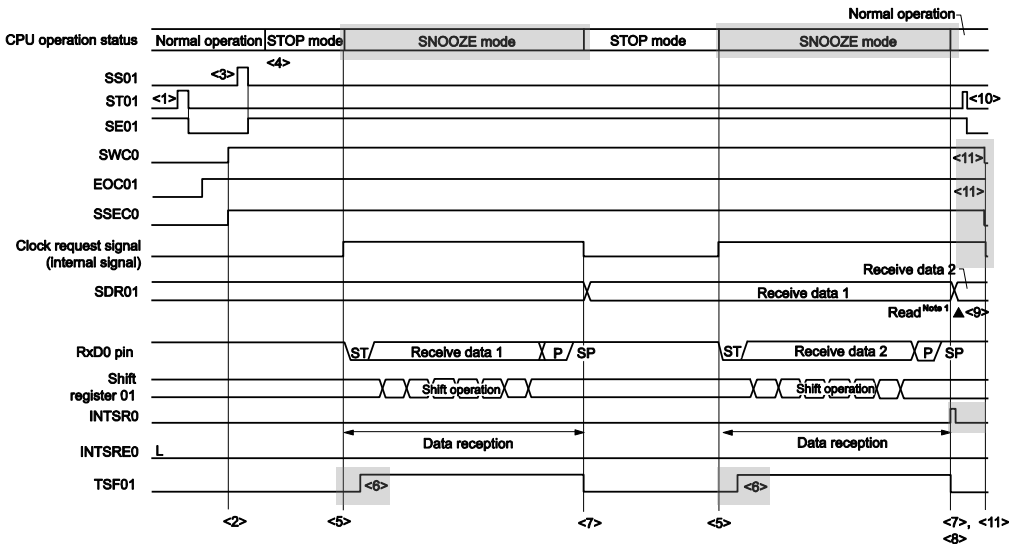
Figure 15-98. Timing Chart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 1)



(omitted)

Correct:

Figure 15-98. Timing Chart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 1)



(omitted)

7. 17.4.5.3 DTC Transfers (D0FIFO and D1FIFO Ports)
Table 17 - 22 DTC Settings(p.895)

Old:

Table 17 - 22 DTC Settings

	Cycle steal transfer	Block transfer
DTCCRj	MODE = 0 (Use this setting in normal mode.) SAMOD = FIFO read direction: 0, FIFO write direction: 1 DAMOD = FIFO read direction: 1, FIFO write direction: 0 (Fix the address of the FIFO side.) CHNE = 0 (Disable chain transfers.) Specify the setting according to the setting of Sz = MBW. Setting other bits is invalid due to normal mode	
DTBLSj (DTC block size)	01H (Sz = 0: 1 byte/Sz = 1: 2 bytes)	Sz = 0: Max. Packet Size Sz = 1: Max. Packet Size/2
DTCCTj	Any value (Max. 256 times)	Any value (Max. 256 times)

New:

Table 17 - 22 DTC Settings

	Cycle steal transfer	Block transfer
DTCCRj	MODE = 0 (Use this setting in normal mode.) SAMOD = FIFO read direction: 0, FIFO write direction: 1 DAMOD = FIFO read direction: 1, FIFO write direction: 0 (Fix the address of the FIFO side.) CHNE = 0 (Disable chain transfers.) Specify the setting according to the setting of Sz = MBW. Setting other bits is invalid due to normal mode	
DTBLSj (DTC block size)	01H (Sz = 0: 1 byte/Sz = 1: 2 bytes)	Sz = 0: Max. Packet Size Sz = 1: Max. Packet Size/2
DTCCTj	Any value (Max. 256 times)	Any value (Max. 256 times)
DTDARj (Destination address)	FIFO Read direction: Data transfer destination address FIFO Write direction : D0FIFOD00/D1FIFOD00	
DTSARj (Source address)	FIFO Read direction : D0FIFOD00/D1FIFOD00 FIFO Write direction: Data transfer source address	

Caution: j=D0FIFO/D1FIFO are assigned to activation source (0~23)
For details of DTC setting, see CHAPTER 19 DATA TRANSFER CONTROLLER

8. 34.6.1 A/D converter characteristics(p.1221)

Voltage Range of A/D conversion was extended.

Old:

(1) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target for conversion: ANI2 to ANI12

(T_A = –40 to +85°C, 2.7 V ≤ AV_{REFP} ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = 0 V, AV_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V, HALT mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}				12	bit
Overall error[Notes 1, 2, 3]	AINL	12-bit resolution		±1.7	±3.3	LSB
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	3.375			μs
Zero-scale error[Notes 1, 2, 3]	E_{ZS}	12-bit resolution		±1.3	±3.2	LSB
Full-scale error[Notes 1, 2, 3]	E_{FS}	12-bit resolution		±0.7	±2.9	LSB
Integral linearity error[Notes 1, 2, 3]	ILE	12-bit resolution		±1.0	±1.4	LSB
Differential linearity error[Notes 1, 2, 3]	DLE	12-bit resolution		±0.9	±1.2	LSB
Analog input voltage	V_{AIN}		0		AV_{REFP}	V

Notes 1. TYP. Value is the average value at AV_{DD} = AV_{REFP} = 3 V and T_A = 25°C. MAX. value is the average value ±3σ at normalized distribution.

2. These values are the results of characteristic evaluation and are not checked for shipment.

3. Excludes quantization error (±1/2 LSB).

Cautions 1. Route the wiring so that noise will not be superimposed on each power line and ground line, and insert a capacitor to suppress noise.

In addition, separate the reference voltage line of AV_{REFP} from the other power lines to keep it free from the influences of noise.

2. During A/D conversion, keep a pulse, such as a digital signal, that abruptly changes its level from being input to or output from the pins adjacent to the converter pins and P20 to P27 and P150 to P154.

New:

(1) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target for conversion: ANI2 to ANI12

(T_A = –40 to +85°C, 2.4 V ≤ AV_{REFP} ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = 0 V, AV_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V, HALT mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}				12	bit
Overall error[Notes 1, 2, 3]	AINL	12-bit resolution		±1.7	±3.3	LSB
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	3.375			μs
Zero-scale error[Notes 1, 2, 3]	E_{ZS}	12-bit resolution		±1.3	±3.2	LSB
Full-scale error[Notes 1, 2, 3]	E_{FS}	12-bit resolution		±0.7	±2.9	LSB
Integral linearity error[Notes 1, 2, 3]	ILE	12-bit resolution		±1.0	±1.4	LSB
Differential linearity error[Notes 1, 2, 3]	DLE	12-bit resolution		±0.9	±1.2	LSB
Analog input voltage	V_{AIN}		0		AV_{REFP}	V

Notes 1. TYP. Value is the average value at AV_{DD} = AV_{REFP} = 3 V and T_A = 25°C. MAX. value is the average value ±3σ at normalized distribution.

2. These values are the results of characteristic evaluation and are not checked for shipment.

3. Excludes quantization error (±1/2 LSB).

Cautions 1. Route the wiring so that noise will not be superimposed on each power line and ground line, and insert a capacitor to suppress noise.

In addition, separate the reference voltage line of AV_{REFP} from the other power lines to keep it free from the influences of noise.

2. During A/D conversion, keep a pulse, such as a digital signal, that abruptly changes its level from being input to or output from the pins adjacent to the converter pins and P20 to P27 and P150 to P154.

9.34.9 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (Page 1234)

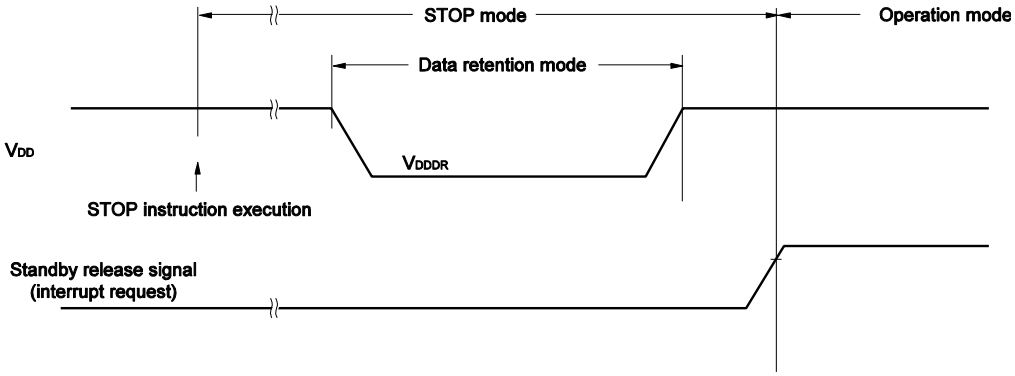
Old:

34.9 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46 Note		3.6	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



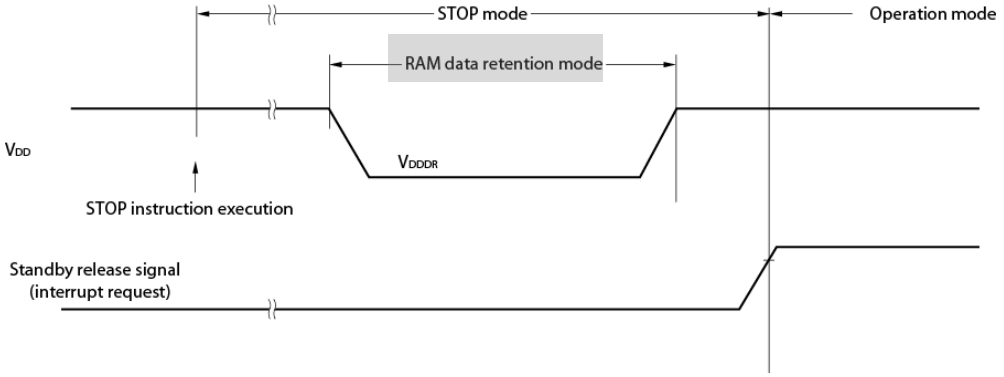
New:

34.9 RAM Data Retention Characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46 Note		3.6	V

Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



10. 35.9 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (Page 1294)

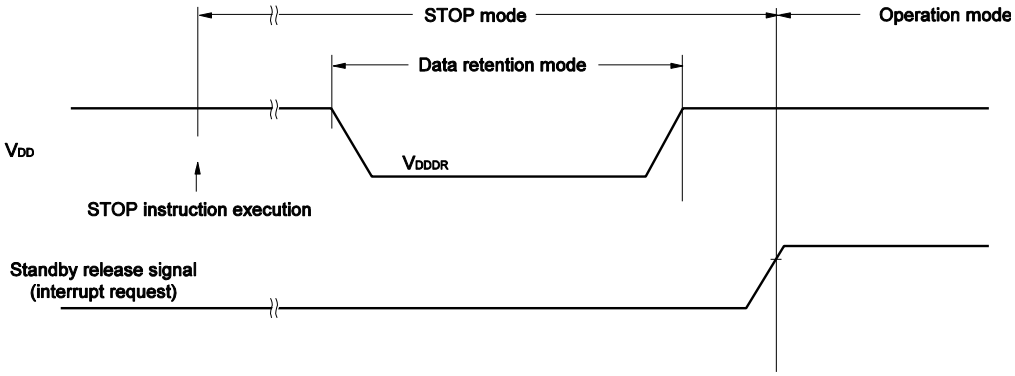
Old:

35.9 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

(T_A = –40 to +105°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44 Note		3.6	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



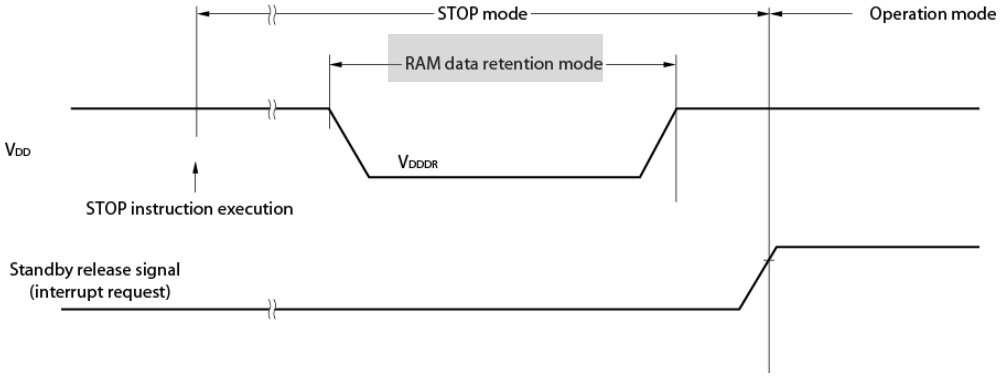
New:

35.9 RAM Data Retention Characteristics

(T_A = –40 to +105°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44 Note		3.6	V

Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



11. 8.3.4 Real-time clock control register 1 (RTCC1)

Additional entry to Figure 8 - 8 Format of Real-time clock control register 1 (RTCC1) (3/3)

Old:

RWAIT	Wait control of real-time clock 2
0	Sets counter operation.
1	Stops SEC to YEAR counters. Mode to read or write counter value

This bit controls the operation of the counter.

Be sure to write “1” to it to read or write the counter value.

As the counter (16-bit) is continuing to run, completereading or writing within one second and turn back to 0.

When RWAIT = 1, it takes up to 1 clock (fRTC) until the counter value can be read or written (RWST = 1).

When the counter (16-bit) overflowed while RWAIT = 1, it keeps the event of overflow until RWAIT = 0, then counts up.

However, when it wrote a value to second count register, it will not keep the overflow event

New:

RWAIT	Wait control of real-time clock 2
0	Sets counter operation.
1	Stops SEC to YEAR counters. Mode to read or write counter value

This bit controls the operation of the counter.

Be sure to write “1” to it to read or write the counter value.

As the counter (16-bit) is continuing to run, completereading or writing within one second and turn back to 0.

When RWAIT = 1, it takes up to 1 clock (fRTC) until the counter value can be read or written (RWST = 1). Notes1,2

When the counter (16-bit) overflowed while RWAIT = 1, it keeps the event of overflow until RWAIT = 0, then counts up.

However, when it wrote a value to second count register, it will not keep the overflow event

Note1. When setting RWAIT=1 during 1 operating clock (f_{RTC}), after setting RTCE=1, it may take two clock time of the operation clock (f_{RTC}), until RWST bit is set to "1".

Note2. When setting RWAIT=1 during 1 operating clock (f_{RTC}), after returning from a stand-by (HALT mode, STOP mode and SNOOZE mode), it may take two clock time of the operation clock (f_{RTC}), until RWST bit is set to "1".

12. 5.2 Configuration of Clock Generator (Page 170)

Additional entry to Figure 5 - 1 Block Diagram of Clock Generator (Products with USB)

Old:

Remark f_X: X1 clock oscillation frequency

f_{HOCO}: High-speed on-chip oscillator clock frequency (48 MHz max.)

f_{IH}: Main system clock source frequency when the high-speed on-chip oscillator clock divided 1,2, 4, or 8, or the PLL clock divided by2, 4, or 8 is selected (24 MHz max.)

f_{EX}: External main system clock frequency

f_{MX}: High-speed system clock frequency

f_{MAIN}: Main system clock frequency

f_{XT}: XT1 clock oscillation frequency

f_{EXT}: External subsystem clock frequency

f_{SUB}: Subsystem clock frequency

f_{CLK}: CPU/peripheral hardware clock frequency

f_{IL}: Low-speed on-chip oscillator clock frequency

New:

Remark f_X: X1 clock oscillation frequency

f_{HOCO}: High-speed on-chip oscillator clock frequency (48 MHz max.)

f_{IH}: Main system clock source frequency when the high-speed on-chip oscillator clock divided 1,2, 4, or 8, or the PLL clock divided by2, 4, or 8 is selected (24 MHz max.)

f_{EX}: External main system clock frequency

f_{MX}: High-speed system clock frequency

f_{MAIN}: Main system clock frequency

f_{XT}: XT1 clock oscillation frequency

f_{EXT}: External subsystem clock frequency

f_{SUB}: Subsystem clock frequency

f_{CLK}: CPU/peripheral hardware clock frequency

f_{IL}: Low-speed on-chip oscillator clock frequency

f_{PLL}:PLL clock frequency

f_{USB}:USB clock frequency

13. 5.3.2 System clock control register (CKC) (Page 174)

Incorrect descriptions revised to Caution 5.

Incorrect:

Caution 5. When using the high-speed on-chip oscillator clock fHOCOset to 48 MHz (FRQSEL4 = 1 in the option byte (000C2H)) or using the PLL clock (48 MHz) for the USB/function controller or 16-bit timers KB20,KB21, and KB22, be sure to set **CCS** to 0.

Correct:

Caution 5. When using the high-speed on-chip oscillator clock fHOCOset to 48 MHz (FRQSEL4 = 1 in the option byte (000C2H)) or using the PLL clock (48 MHz) for the USB/function controller or 16-bit timers KB20,KB21, and KB22, be sure to set CSS to 0.

14. 5.3.6 Peripheral enable registers 0, 1, 2 (PER0, PER1, PER2) (Page 180,181)

Incorrect:

Figure 5 - 8 Format of Peripheral enable register 0 (PER0) (1/2)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	1	<0>
PER0	RTCWEN Note	0	ADCEN	IICA0EN	SAU1EN	SAU0EN	0	TAU0EN

RTCWEN Note	Control of real-time clock 2 (RTC2) input clock supply
0	Stops input clock supply. • SFRs used by the real-time clock 2 (RTC2) cannot be written. • The real-time clock 2 (RTC2) is operable.
1	Enables input clock supply. • SFRs used by the real-time clock 2 (RTC2) can be read and written. • The real-time clock 2 (RTC2) is operable.

ADCEN	Control of A/D converter input clock supply
0	Stops input clock supply. • SFRs used by the A/D converter cannot be written. • The A/D converter is in the reset status.
1	Enables input clock supply. • SFRs used by the A/D converter can be read and written.

Note The RTCWEN bit is reset only by a power-on reset; it retains the value when a reset caused by another factor occurs.

Caution Be sure to clear bits 6 and 1 to 0.

Correct:

Figure 5 - 8 Format of Peripheral enable register 0 (PER0) (1/2)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	1	<0>
PER0	RTCWEN	0	ADCEN	IICA0EN	SAU1EN	SAU0EN	0	TAU0EN

RTCWEN	Control of real-time clock 2 (RTC2) input clock supply
0	Stops input clock supply.(Stops f_{CLK} clock supply) • SFRs used by the real-time clock 2 (RTC2) cannot be written. • The real-time clock 2 (RTC2) is operable.
1	Enables input clock supply. • SFRs used by the real-time clock 2 (RTC2) can be read and written. • The real-time clock 2 (RTC2) is operable.

ADCEN	Control of A/D converter input clock supply
0	Stops input clock supply. • SFRs used by the A/D converter cannot be written. • The A/D converter is in the reset status.
1	Enables input clock supply. • SFRs used by the A/D converter can be read and written.

Caution Be sure to clear bits 6 and 1 to 0.

15. 5.3.10 PLL control register (DSCCTL) (Page 187)

Additional entry to Figure 5 - 15 Format of PLL control register (DSCCTL)

Old:

Figure 5-15. Format of PLL Control Register (DSCCTL)

Address: F02E5H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
DSCCTL	0	0	0	0	0	DSFRDIV	DSCM	DSCON

DSFRDIV	PLL reference clock divider control
0	No division
1	Divided by 2

Remark PLL reference clock is the high-speed system clock (f_{MX}).

DSCM	PLL multiplication selection
0	12 times (6 times)
1	16 times (8 times)

Remark The frequency is divided by 2 in the last stage of the PLL oscillator, therefore the multiplication ratio becomes the value in parentheses.

DSCON	PLL oscillation and output control
0	Stop
1	Ocsillation, output

Caution Be sure to clear bits 3 to 7 to 0.

New:

Figure 5-15. Format of PLL Control Register (DSCCTL)

Address: F02E5H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
DSCCTL	0	0	0	0	0	DSFRDIV	DSCM	DSCON

DSFRDIV	PLL reference clock divider control
0	No division
1	Divided by 2

Remark PLL reference clock is the high-speed system clock (f_{MX}).

DSCM	PLL multiplication selection
0	12 times (6 times)
1	16 times (8 times)

Remark The frequency is divided by 2 in the last stage of the PLL oscillator, therefore the multiplication ratio becomes the value in parentheses.

DSCON	PLL oscillation and output control
0	Stop
1	Ocsillation, output

Caution 1. Be sure to clear bits 3 to 7 to 0.

Caution 2. Be sure to set the DSCON bit to 0 before changing DSFRDIV and DSCM.

Caution 3. Do not set the DSCON bit to 0 while the PLL clock is selected as the system clock.

16. 5.4.5 PLL (Phase Locked Loop) (Page 194)

Incorrect descriptions revised to Caution 2.

Old:

Caution 1. When switching from PLL mode to the internal high-speed oscillation clock and the high speed system clock, stop the function (USB function controller) that provides the PLL output clock (f_{PLL}).

Caution 2. PLL operations cannot be performed while the subsystem clock is operating

New:

Caution 1. When switching from PLL mode to the internal high-speed oscillation clock and the high speed system clock, stop the function (USB function controller) that provides the PLL output clock (f_{PLL}).

Caution 2. Do not set the DSCON bit to 1 to start the PLL operating while the subsystem clock is the operating clock for the CPU.

17. 5.6.1 Example of setting high-speed on-chip oscillator (Page 197)

Incorrect descriptions revised to 5.6.1 Example of setting high-speed on-chip oscillator.

Old:

[Option byte setting]

Address: 000C2H

Option byte (000C2H)	7	6	5	4	3	2	1	0
	CMODE1 1	CMODE0 1	 1	FRQSEL4 1	FRQSEL3 0	FRQSEL2 0	FRQSEL1 0	FRQSEL0 0/1

CMODE1	CMODE0	Setting of flash operation mode
0	0	LV (low voltage main) mode VDD= 1.6 V to 3.6 V @ 1 MHz to 4 MHz
1	0	LS (low speed main) mode VDD= 1.8 V to 3.6 V @ 1 MHz to 8 MHz
1	1	**HS (high speed main) mode** V_{DD} = 2.4 V to 5.5 V @ 1 MHz to 16 MHz V_{DD} = 2.7 V to 5.5 V @ 1 MHz to 24 MHz
Other than above		Setting prohibited

FRQSEL4	FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0	Frequency of the high-speed on-chip oscillator	
					f_{HOCO}	f_{IH}
1	0	0	0	0	**48 MHz**	**24 MHz**
(omitted)						
Other than above					Setting prohibited	

Note See the MCKC register for division ratio settings.

New:

[Option byte setting]

Address: 000C2H

Option byte (000C2H)	7	6	5	4	3	2	1	0
	CMODE1 1	CMODE0 1	 1	FRQSEL4 1	FRQSEL3 0	FRQSEL2 0	FRQSEL1 0	FRQSEL0 0/1

CMODE1	CMODE0	Setting of flash operation mode
0	0	LV (low voltage main) mode VDD= 1.6 V to 3.6 V @ 1 MHz to 4 MHz
1	0	LS (low speed main) mode VDD= 1.8 V to 3.6 V @ 1 MHz to 8 MHz
1	1	HS (high speed main) mode[Note1] V_{DD} = 2.4 V to 5.5 V @ 1 MHz to 16 MHz V_{DD} = 2.7 V to 5.5 V @ 1 MHz to 24 MHz
Other than above		Setting prohibited

FRQSEL4	FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0	Frequency of the high-speed on-chip oscillator	
					f_{HOCO}	f_{IH}
1	0	0	0	0	48 MHz[Note2]	24 MHz[Note3]
(omitted)						
Other than above					Setting prohibited	

Note 1. When you use PLL, please choose HS (high speed Maine) mode.

Note 2. When you use PLL, I set it in FRQSEL4=0, and, please do not choose 48MHz.

Note3. See the MCKC register for division ratio settings.

18. 5.6.4 Example of setting PLL circuit (Page 201)

Incorrect descriptions revised to 5.6.4 Example of setting PLL circuit.

Old:

[Register settings] Set the register in the order of <1> to <5> below.

<1> Set the DSFRDIV bit and DSCM bit in the DSCCTL register to set the PLL multiplication and division.

	7	6	5	4	3	2	1	0
DSCCTL	0	0	0	0	0	DSFRDIV 0/1	DSCM 0/1	DSCON 0

<2> Set the RDIV1, RDIV0 bits of the MCKC register to set the division of the system clock.

	7	6	5	4	3	2	1	0
MCKC	0	0	0	0	0	RDIV1 0/1	RDIV0 0/1	CKSELR 0

AMPHS0 and AMPHS1 bits: These bits are used to specify the oscillation mode of the XT1 oscillator.

<3> Set (1) the DSCON bit of the DSCCTL register to operate the PLL circuit Note.

	7	6	5	4	3	2	1	0
DSCCTL	0	0	0	0	0	DSFRDIV 0/1	DSCM 0/1	DSCON 1

<4> Wait for 40 μs by using software.

<5> Set (1) the CKSELR bit of the MCKC register to select PLL output for the system clock.

	7	6	5	4	3	2	1	0
MCKC	0	0	0	0	0	RDIV1 0/1	RDIV0 0/1	CKSELR 1

Note After the X1 oscillator clock stabilizes, allow at least 1 μs to elapse before operating the PLL. When operating the PLL again after it has been stopped, wait for at least 4 μs before operating.

New:

[Register settings] Set the register in the order of <1> to <5> below.

<1> Set the HIOSTOP bit in the CSC register to make the high-speed on-chip oscillator run.

	7	6	5	4	3	2	1	0
CSC	0/1	0/1	0	0	0	0	0	HIOSTOP 0Note1

<2> Set the DSFRDIV bit and DSCM bit in the DSCCTL register to set the PLL multiplication and division.

	7	6	5	4	3	2	1	0
DSCCTL	0	0	0	0	0	DSFRDIV 0/1	DSCM 0/1	DSCON 0

<3> Set the RDIV1, RDIV0 bits of the MCKC register to set the division of the system clock.

	7	6	5	4	3	2	1	0
MCKC	0	0	0	0	0	RDIV1 0/1	RDIV0 0/1	CKSELR 0

AMPHS0 and AMPHS1 bits: These bits are used to specify the oscillation mode of the XT1 oscillator.

<4> Set (1) the DSCON bit of the DSCCTL register to operate the PLL circuit Note.

	7	6	5	4	3	2	1	0
DSCCTL	0	0	0	0	0	DSFRDIV 0/1	DSCM 0/1	DSCON 1

<5> Set (1) the CKSELR bit of the MCKC register to select PLL output for the system clock.

	7	6	5	4	3	2	1	0
MCKC	0	0	0	0	0	RDIV1 0/1	RDIV0 0/1	CKSELR 1

<6> Use software to set up a wait of 65 μs.[Note3]

<7> Set the HIOSTOP bit in the CSC register to stop the high-speed on-chip oscillator.[Note2]

	7	6	5	4	3	2	1	0
CSC	0/1	0/1	0	0	0	0	0	HIOSTOP 1[Note1]

<8> When the PLL clock frequency divided by 2, 4, or 8 is selected as the main system clock (f_{MAIN}), set the MCM0 bit in the CKC register to select the source for deriving the main system clock as a signal with a frequency (f_{IH}) of up to 24 MHz.

	7	6	5	4	3	2	1	0
CKC	CLS 0/1	CSS 0/1	MCS 0	MCM0 0	0	0	0	0

Note 1. No setting is required to change to the PLL while the CKSELR bit is 1.

When setting the CKSELR bit to 1, ensure that the high-speed on-chip oscillator is running.

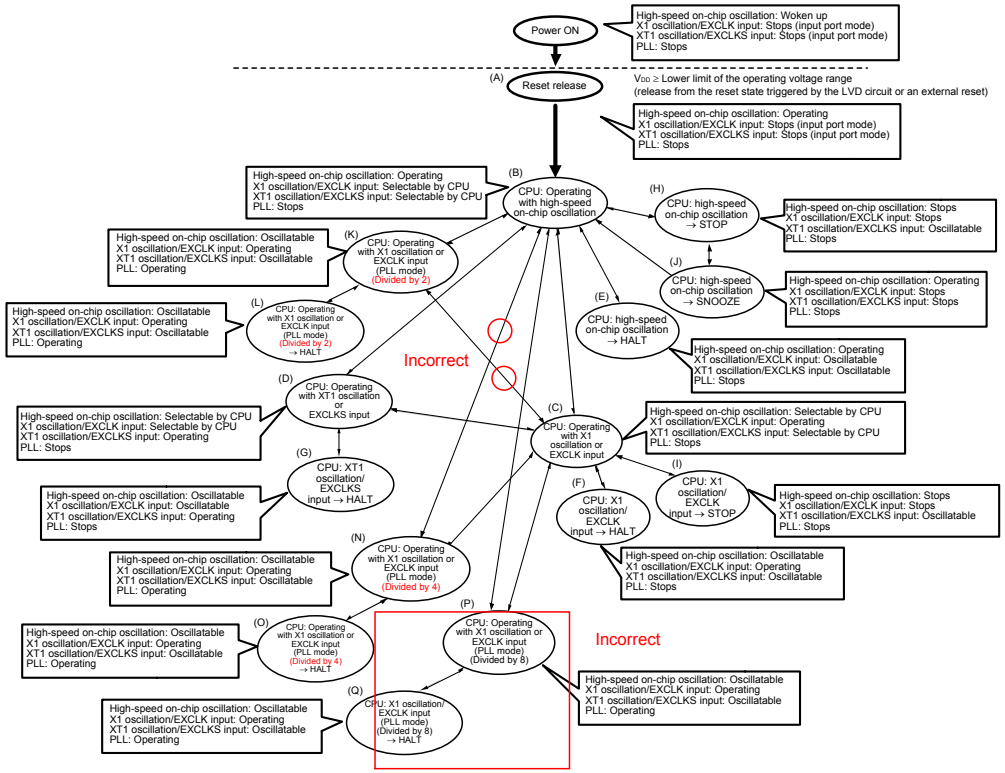
Note 2. After oscillation by the X1 oscillator clock has become stable, allow at least 1 μs to elapse before starting the PLL. When restarting the PLL after it has been stopped, wait for at least 4 μs before using it in operations.

Note 3. Wait for 40 μs for oscillation by the oscillator clock to become stabled if the HIOSTOP bit is not set to 0.

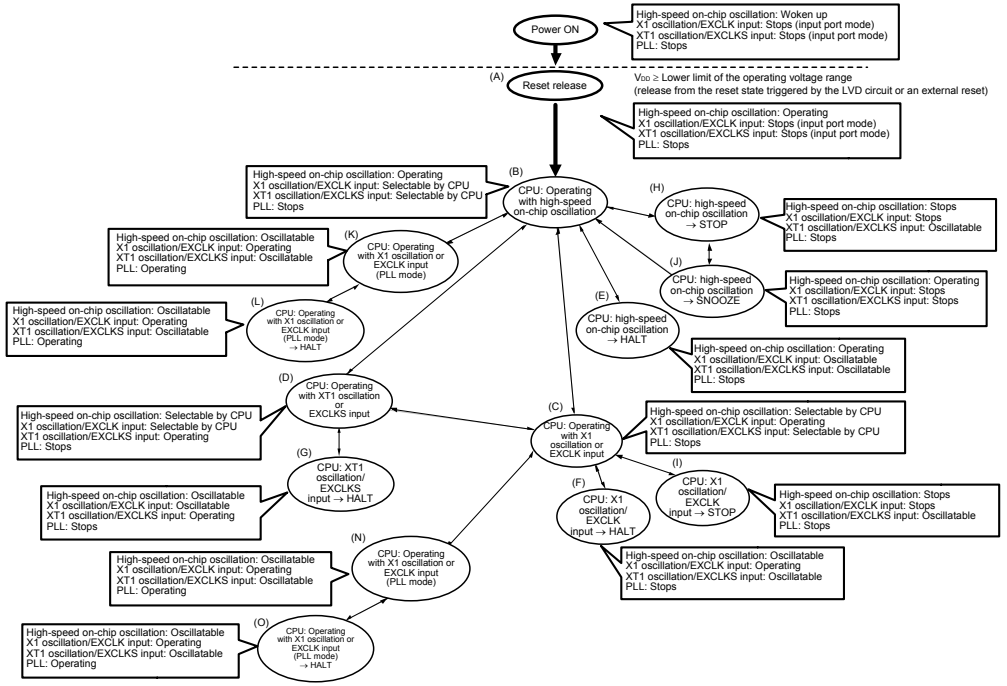
19. 5.6.5 CPU clock status transition diagram (Page 202)

Incorrect descriptions revised to Figure 5 - 24 CPU Clock Status Transition Diagram (Products with USB).

Old:



New:



20. 5.6.5 CPU clock status transition diagram

Table 5 - 4 CPU Clock Transition and SFR Register Setting Examples (pages 203 to 209)

Old:

(2) CPU operating with high-speed system clock (C) after reset release (A)

(The CPU operates with the high-speed on-chip oscillator clock immediately after a reset release (B).)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	CMC Register Note 1			OSTS Register	CSC Register	OSTC Register	CKC Register
	EXCLK	OSCSEL	AMPH		MSTOP		MCM0
(A) → (B) → (C) (X1 clock: 1 MHz ≤ f_X ≤ 10 MHz)	0	1	0	**Note 2**	0	Must be checked	1
(A) → (B) → (C) (X1 clock: 10 MHz < f_X ≤ 20 MHz)	0	1	**0**	**Note 2**	0	Must be checked	1
(A) → (B) → (C) (external main clock)	1	1	×	**Note 2**	0	Must not be checked	1

New:

(2) CPU operating with high-speed system clock (C) after reset release (A)

(The CPU operates with the high-speed on-chip oscillator clock immediately after a reset release (B).)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	CMC Register Note 1			OSTS Register	CSC Register	OSTC Register	CKC Register
	EXCLK	OSCSEL	AMPH		MSTOP		MCM0
(A) → (B) → (C) (X1 clock: 1 MHz ≤ f_X ≤ 10 MHz)	0	1	0	**Note 2**	0	Must be checked	1
(A) → (B) → (C) (X1 clock: 10 MHz < f_X ≤ 20 MHz)	0	1	1	**Note 2**	0	Must be checked	1
(A) → (B) → (C) (external main clock)	1	1	×	**Note 2**	0	Must not be checked	1

Old:

(4) CPU clock changing from high-speed on-chip oscillator clock (B) to high-speed system clock (C)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	CMC Register Note 1			OSTS Register	CSC Register	OSTC Register	CKC Register
	EXCLK	OSCSEL	AMPH		MSTOP		MCM0
(B) → (C) (X1 clock: 1 MHz ≤ f_X ≤ 10 MHz)	0	1	0	**Note 2**	0	Must be checked	1
(B) → (C) (X1 clock: 10 MHz < f_X ≤ 20 MHz)	0	1	1	**Note 2**	0	Must be checked	1
(B) → **(D)** (external main clock)	1	1	×	**Note 2**	0	Must not be checked	1

Unnecessary if these registers are already set

Unnecessary if the CPU is operating with the high-speed system clock

(6) CPU clock changing from high-speed system clock (C) to high-speed on-chip oscillator clock (B)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	CSC Register	Oscillation accuracy stabilization time	CKC Register
	HIOSTOP		MCM0
(C) → (B)	0	Note	0

Unnecessary if the CPU is operating with the high-speed on-chip oscillator clock

Note When FRQSEL4 = 0: 18 μs to 65 μs

When FRQSEL4 = 1: 18 μs to 75 μs

New:

(4) CPU clock changing from high-speed on-chip oscillator clock (B) to high-speed system clock (C)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	CMC Register Note 1			OSTS Register	CSC Register	OSTC Register	CKC Register
	EXCLK	OSCSEL	AMPH		MSTOP		MCM0
(B) → (C) (X1 clock: 1 MHz ≤ f_X ≤ 10 MHz)	0	1	0	**Note 2**	0	Must be checked	1
(B) → (C) (X1 clock: 10 MHz < f_X ≤ 20 MHz)	0	1	1	**Note 2**	0	Must be checked	1
(B) → (C) (external main clock)	1	1	×	**Note 2**	0	Must not be checked	1

Unnecessary if these registers are already set

Unnecessary if the CPU is operating with the high-speed system clock

(6) CPU clock changing from high-speed system clock (C) to high-speed on-chip oscillator clock (B)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	CSC Register	Oscillation accuracy stabilization time	CKC Register
	HIOSTOP		MCM0
(C) → (B)	0	Note	0

Unnecessary if the CPU is operating with the high-speed on-chip oscillator clock

Note When FRQSEL4 = 0: 18 μs to 65 μs

When FRQSEL4 = 1: 18 μs to 135 μs

Old:

(8) CPU clock changing from subsystem clock (D) to high-speed on-chip oscillator clock (B)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	CSC Register HIOSTOP	Oscillation accuracy stabilization time	CKC Register CSS
(D) → (B)	0	Note	0

Unnecessary if the CPU is operating with the high-speed on-chip oscillator clock

Note When FRQSEL4 = 0: 18 μs to 65 μs

When FRQSEL4 = 1: 18 μs to 75 μs

New:

(8) CPU clock changing from subsystem clock (D) to high-speed on-chip oscillator clock (B)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	CSC Register HIOSTOP	Oscillation accuracy stabilization time	CKC Register CSS
(D) → (B)	0	Note	0

Unnecessary if the CPU is operating with the high-speed on-chip oscillator clock

Note When FRQSEL4 = 0: 18 μs to 65 μs

When FRQSEL4 = 1: 18 μs to 135 μs

Old:

(10) • **CPU clock changing from high-speed on-chip oscillator clock (B) to high-speed system clock (PLL mode) (divided by 2) (K)**

• **CPU clock changing from high-speed on-chip oscillator clock (B) to high-speed system clock (PLL mode) (divided by 4) (N)**

• **CPU clock changing from high-speed on-chip oscillator clock (B) to high-speed system clock (PLL mode) (divided by 8) (P)**

• CPU clock changing from high-speed system clock (C) to high-speed system clock (PLL mode) **(divided by 2)** (K)

• **CPU clock changing from high-speed system clock (C) to high-speed system clock (PLL mode) (divided by 4) (N)**

• **CPU clock changing from high-speed system clock (C) to high-speed system clock (PLL mode) (divided by 8) (P)**

(Setting sequence of SFR registers) ⟶

Setting Flag of SFR Register / Status Transition	DSCCTL Register		MCKC Register		Waiting for Oscillation Stabilization	MCKC Register
	DSFRDIV	DSCM	RDIV1	RDIV0		CKSELR
(B) → (K) (B) → (N) (B) → (P) (C) → (K) (C) → (N) (C) → (P)	0/1	0/1	0/1	0/1	40 μs	1

New:

(10) • CPU clock changing from high-speed on-chip oscillator clock (B) to high-speed system clock (PLL mode) (K)

• CPU clock changing from high-speed system clock (C) to high-speed system clock (PLL mode) (N)

Continue

（Setting sequence of SFR registers）

Setting Flag of SFR Register / Status Transition	CMC Register Note 1			OSTS Register	CSC Register	OSTC Register	DSCCTL Register		MCKC Register		Waiting for Oscillation Stabilization	DSCCTL Register	Waiting for Oscillation Stabilization	MCKC Register
	EXCLK	OSCSEL	AMPH		MSTOP		DSFRDIV	DSCM	RDIV1	RDIV0		DSCON		CKSELR
(B) → (K) (divided by 2)	0/1	1	0/1	Note 2	0	Must be checked	0/1	0/1	0	0	1us	1	40us	1
(B) → (K) (divided by 4)	0/1	1	0/1	Note 2	0	Must be checked	0/1	0/1	0	1		1		1
(B) → (K) (divided by 8)	0/1	1	0/1	Note 2	0	Must be checked	0/1	0/1	1	0		1		1

Note 1. Writing to the clock operating mode control register (CMC) can only proceed once and must be by an 8-bit memory manipulation instruction after release from the reset state.

Note 2. Set the oscillation stabilization time in the oscillation stabilization time select register (OSTS) as follows.

・Desired oscillation stabilization time setting of the oscillation stabilization time counter status register (OSTC) ≤ Oscillation stabilization time set in the OSTS register

Caution: Completion of clock switching after the CKSELR bit has been set to 1 requires up to 2 clock cycles when the FRQSEL4 bit is 1, and up to 10 clock cycles when the FRQSEL4 bit is 0. Until the clock switching is completed, do not stop the high-speed on-chip oscillator.

（Setting sequence of SFR registers）

Setting Flag of SFR Register / Status Transition	CSC Register	DSCCTL Register		MCKC Register		DSCCTL Register	MCKC Register	Waiting for Oscillation Stabilization	CSC Register	CKC Register
	HIOSTOP	DSFRDIV	DSCM	RDIV1	RDIV0	DSCON	CKSELR		HIOSTOP	MCM0
(C) → (N) (divided by 2)	0 Note3	0/1	0/1	0	0	1	1 Note3	65us Note4	1 Note3	0
(C) → (N) (divided by 2)	0 Note3	0/1	0/1	0	1	1	1 Note3		1 Note3	0
(C) → (N) (divided by 2)	0 Note3	0/1	0/1	1	0	1	1 Note3		1 Note3	0

Note 3. No setting is required to change to the PLL while the CKSELR bit is 1. When setting the CKSELR bit to 1, ensure that the high-speed on-chip oscillator is running.

Note 4. Wait for 40 μs for oscillation by the oscillator clock to become stable if the HIOSTOP bit is not set to 0.

Old:

(11) • CPU clock changing from high-speed system clock (PLL mode) **(divided by 2)** (K) to high-speed on-chip oscillator clock (B)

• CPU clock changing from high-speed system clock (PLL mode) (divided by 4) (N) to high-speed on-chip oscillator clock (B)

• CPU clock changing from high-speed system clock (PLL mode) (divided by 8) (P) to high-speed on-chip oscillator clock (B)

• CPU clock changing from high-speed system clock (PLL mode) (divided by 2) (K) to high-speed system clock (C)

• CPU clock changing from high-speed system clock (PLL mode) (divided by 4) (N) to high-speed system clock (C)

• CPU clock changing from high-speed system clock (PLL mode) (divided by 8) (P) to high-speed system clock (C)

(Setting sequence of SFR registers) ⟶

Setting Flag of SFR Register / Status Transition	MCKC Register	DSCCTL Register
	CKSELR	DSCON
(K) → (B) (N) → (B) (P) → (B) (K) → (C) (N) → (C) (P) → (C)	0	0

New:

(11) • CPU clock changing from high-speed system clock (PLL mode) (K) to high-speed on-chip oscillator clock (B)

• CPU clock changing from high-speed system clock (PLL mode) (N) to high-speed system clock (C)

Setting Flag of SFR Register / Status Transition	CSC Register	Waiting for Oscillation Stabilization	MCKC Register	Waiting for clock change	DSCCTL Register
	HIOSTOP		CKSELR		DSCON
(K) → (B) FRQSEL4=0	0	18～65 μs	0	256 clokc	0
(K) → (B) FRQSEL4=1		18～135 μs		16 clock	

(Setting sequence of SFR registers) ⟶

Setting Flag of SFR Register / Status Transition	CKC Register MCM0	Waiting for clock change	DSCCTL Register DSCON
(N) → (C) (divided by 2) (RDIV1,0 = 00) High-speed system clock (fMX) = 16MHz	1	3 Clock	0
(N) → (C) (divided by 2) (RDIV1,0 = 00) High-speed system clock (fMX) = 12MHz		4 Clock	
(N) → (C) (divided by 2) (RDIV1,0 = 00) High-speed system clock (fMX) = 8MHz		6 Clock	
(N) → (C) (divided by 2) (RDIV1,0 = 00) High-speed system clock (fMX) = 6MHz		8 Clock	
(N) → (C) (divided by 4) (RDIV1,0 = 01) High-speed system clock (fMX) = 16MHz		2 Clock	
(N) → (C) (divided by 4) (RDIV1,0 = 01) High-speed system clock (fMX) = 12MHz		2 Clock	
(N) → (C) (divided by 4) (RDIV1,0 = 01) High-speed system clock (fMX) = 8MHz		3 Clock	
(N) → (C) (divided by 4) (RDIV1,0 = 01) High-speed system clock (fMX) = 6MHz		4 Clock	
(N) → (C) (divided by 8) (RDIV1,0 = 10) High-speed system clock (fMX) = 16MHz		2 Clock	
(N) → (C) (divided by 8) (RDIV1,0 = 10) High-speed system clock (fMX) = 12MHz		2 Clock	
(N) → (C) (divided by 8) (RDIV1,0 = 10) High-speed system clock (fMX) = 8MHz		2 Clock	
(N) → (C) (divided by 8) (RDIV1,0 = 10) High-speed system clock (fMX) = 6MHz		2 Clock	

Old:

(12) • HALT mode (E) set while CPU is operating with high-speed on-chip oscillator clock (B)

• HALT mode (F) set while CPU is operating with high-speed system clock (C)

• HALT mode (G) set while CPU is operating with subsystem clock (D)

• HALT mode (L) set while CPU is operating with high-speed system clock (PLL mode) **(divided by 2)** (K)

• HALT mode (O) set while CPU is operating with high-speed system clock (PLL mode) (divided by 4) (N)

• HALT mode (Q) set while CPU is operating with high-speed system clock (PLL mode) (divided by 8) (P)

Status Transition	Setting
(B) → (E) (C) → (F) (D) → (G) (K) → (L) **(N) → (O)** **(P) → (Q)**	Executing HALT instruction

(15) • STOP mode (I) set while CPU is operating with high-speed system clock (PLL mode) **(divided by 2)** (K)

・ STOP mode (I) set while CPU is operating with high-speed system clock (PLL mode) (divided by 4) (N)

・ STOP mode (I) set while CPU is operating with high-speed system clock (PLL mode) (divided by 8) (P)

Switch from PLL mode operation to **high-speed on-chip oscillator clock** and high-speed system clock operations

(refer to 5.6.5 (11)) and stop the PLL (DSCON = 0), then execute the STOP instruction

New:

(12) • HALT mode (E) set while CPU is operating with high-speed on-chip oscillator clock (B)

• HALT mode (F) set while CPU is operating with high-speed system clock (C)

• HALT mode (G) set while CPU is operating with subsystem clock (D)

• HALT mode (L) set while CPU is operating with high-speed system clock (PLL mode) (K)

• HALT mode (O) set while CPU is operating with high-speed system clock (PLL mode) (N)

Status Transition	Setting
(B) → (E) (C) → (F) (D) → (G) (K) → (L) (N) → (O)	Executing HALT instruction

(15) • Changing to STOP mode (I) from the high-speed system clock (PLL mode) as the operating clock for the CPU (K)

Switch to high-speed system clock operation from PLL mode, stop the PLL (DSCON = 0), and then execute the STOP instruction.

21. 5.6.5 CPU clock status transition diagram

Table 5 - 11 CPU Clock Transition and SFR Register Setting Examples (page 213)

Old:

(6) CPU clock changing from high-speed system clock (C) to high-speed on-chip oscillator clock (B)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	CSC Register HIOSTOP	Oscillation accuracy stabilization time	CKC Register MCM0
(C) → (B)	0	When FRQSEL4 = 0: 18	0

Unnecessary if the CPU is operating with the high-speed on-chip oscillator clock

Note When FRQSEL4 = 0: 18 μs to 65 μs

When FRQSEL4 = 1: 18 μs to 75 μs

(8) CPU clock changing from subsystem clock (D) to high-speed on-chip oscillator clock (B)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	CSC Register HIOSTOP	Oscillation accuracy stabilization time	CKC Register CSS
(D) → (B)	0	When FRQSEL4 = 0: 18	0

Unnecessary if the CPU is operating with the high-speed on-chip oscillator clock

Note When FRQSEL4 = 0: 18 μs to 65 μs

When FRQSEL4 = 1: 18 μs to 75 μs

New:

(6) CPU clock changing from high-speed system clock (C) to high-speed on-chip oscillator clock (B)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	CSC Register HIOSTOP	Oscillation accuracy stabilization time	CKC Register MCM0
(C) → (B)	0	When FRQSEL4 = 0: 18	0

Unnecessary if the CPU is operating with the high-speed on-chip oscillator clock

Note When FRQSEL4 = 0: 18 μs to 65 μs

When FRQSEL4 = 1: 18 μs to 135 μs

(8) CPU clock changing from subsystem clock (D) to high-speed on-chip oscillator clock (B)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	CSC Register HIOSTOP	Oscillation accuracy stabilization time	CKC Register CSS
(D) → (B)	0	When FRQSEL4 = 0: 18	0

Unnecessary if the CPU is operating with the high-speed on-chip oscillator clock

Note When FRQSEL4 = 0: 18 μs to 65 μs

When FRQSEL4 = 1: 18 μs to 135 μs

22. 5.6.6 Condition before changing CPU clock and processing after changing CPU clock (pages 216 217)

Old:

Table 5-16. Changing CPU Clock (1/3)

CPU Clock		Condition Before Change	Processing After Change
Before Change	After Change		
X1 clock	(omitted)		
	PLL clock	Oscillation of PLL • DSCON = 1	–

New:

Table 5-16. Changing CPU Clock (1/3)

CPU Clock		Condition Before Change	Processing After Change
Before Change	After Change		
X1 clock	(omitted)		
	PLL clock	Oscillation of PLL • DSCON = 1 Enabling oscillation of high-speed on-chip oscillator · HIOSTOP = 0 · The oscillation accuracy stabilization time has elapsed	–

Old:

Table 5-16. Changing CPU Clock (2/3)

CPU Clock		Condition Before Change	Processing After Change
Before Change	After Change		
External main system clock	High-speed on-chip oscillator clock	Enabling oscillation of high-speed on-chip oscillator • HIOSTOP = 0 • After elapse of oscillation accuracy stabilization time	External main system clock input can be disabled (MSTOP = 1).
	X1 clock	Transition not possible	–
	XT1 clock	Stabilization of XT1 oscillation • OSCSELS = 1, EXCLKS = 0, XTSTOP = 0 • After elapse of oscillation stabilization time	External main system clock input can be disabled (MSTOP = 1).
	External subsystem clock	Enabling input of external clock from the EXCLKS pin • OSCSELS = 1, EXCLKS = 1, XTSTOP = 0	External main system clock input can be disabled (MSTOP = 1).
	PLL clock	Oscillation of PLL • DSCON = 1	–
(omitted)			

New:

Table 5-16. Changing CPU Clock (2/3)

CPU Clock		Condition Before Change	Processing After Change
Before Change	After Change		
External main system clock	High-speed on-chip oscillator clock	Enabling oscillation of high-speed on-chip oscillator • HIOSTOP = 0 • After elapse of oscillation accuracy stabilization time	External main system clock input can be disabled (MSTOP = 1).
	X1 clock	Transition not possible	–
	XT1 clock	Stabilization of XT1 oscillation • OSCSELS = 1, EXCLKS = 0, XTSTOP = 0 • After elapse of oscillation stabilization time	External main system clock input can be disabled (MSTOP = 1).
	External subsystem clock	Enabling input of external clock from the EXCLKS pin • OSCSELS = 1, EXCLKS = 1, XTSTOP = 0	External main system clock input can be disabled (MSTOP = 1).
	PLL clock	Oscillation of PLL • DSCON = 1 Enabling oscillation of high-speed on-chip oscillator · HIOSTOP = 0 · The oscillation accuracy stabilization time has elapsed	–
(omitted)			

23. 6.3.1 Peripheral enableregister 0 (PER0) (Page 240)

Incorrect:

Figure 6 - 11 Format of Peripheral enable register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	1	<0>
PER0	RTCWEN Note	0	ADCEN	IICA0EN	SAU1EN	SAU0EN	0	TAU0EN

TAU0EN	Control of timer array unit input clock
0	Stops supply of input clock. · SFR used by the timer array unit cannot be written. · The timer array unit is in the reset status
1	Supplies input clock. · SFR used by the timer array unit can be read/written.

Note The RTCWEN bit is reset only by a power-on reset; it retains the value when a reset caused by another factor occurs.

Correct:

Figure 6 - 11 Format of Peripheral enable register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	1	<0>
PER0	RTCWEN	0	ADCEN	IICA0EN	SAU1EN	SAU0EN	0	TAU0EN

TAU0EN	Control of timer array unit input clock
0	Stops supply of input clock. · SFR used by the timer array unit cannot be written. · The timer array unit is in the reset status
1	Supplies input clock. · SFR used by the timer array unit can be read/written.

24. 8.3.1 Peripheral enableregister 0 (PER0) (Page 451)

Incorrect:

Figure 8 - 2 Format of Peripheral enable register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	1	<0>
PER0	RTCWEN	0	ADCEN	IICA0EN	SAU1EN	SAU0EN	0	TAU0EN

RTCWEN Note	Control of internal clock supply to real-time clock 2
0	Stops input clock supply. · SFR used by the real-time clock 2 cannot be written. · The real-time clock 2 can operate.
1	Enables input clock supply. · SFR used by the real-time clock 2 can be read/written. · The real-time clock 2 can operate

Note The RTCWEN bit is reset only by a power-on reset; it retains the value when a reset caused by another factor occurs.

Caution 1. When using the real-time clock 2, first set the RTCWEN bit to 1, while oscillation of the input clock (fRTC)is stable. If RTCWEN = 0, writing to a control register of the real-time clock 2 is ignored.

Caution 2. Be sure to set bits 1 and 6 to 0

Correct:

Figure 8 - 2 Format of Peripheral enable register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	1	<0>
PER0	RTCWEN	0	ADCEN	IICA0EN	SAU1EN	SAU0EN	0	TAU0EN

RTCWEN	Control of internal clock supply to real-time clock 2
0	Stops input clock supply. (Stops f_{CLK} clock supply) · SFR used by the real-time clock 2 cannot be written. · The real-time clock 2 can operate.
1	Enables input clock supply. · SFR used by the real-time clock 2 can be read/written. · The real-time clock 2 can operate

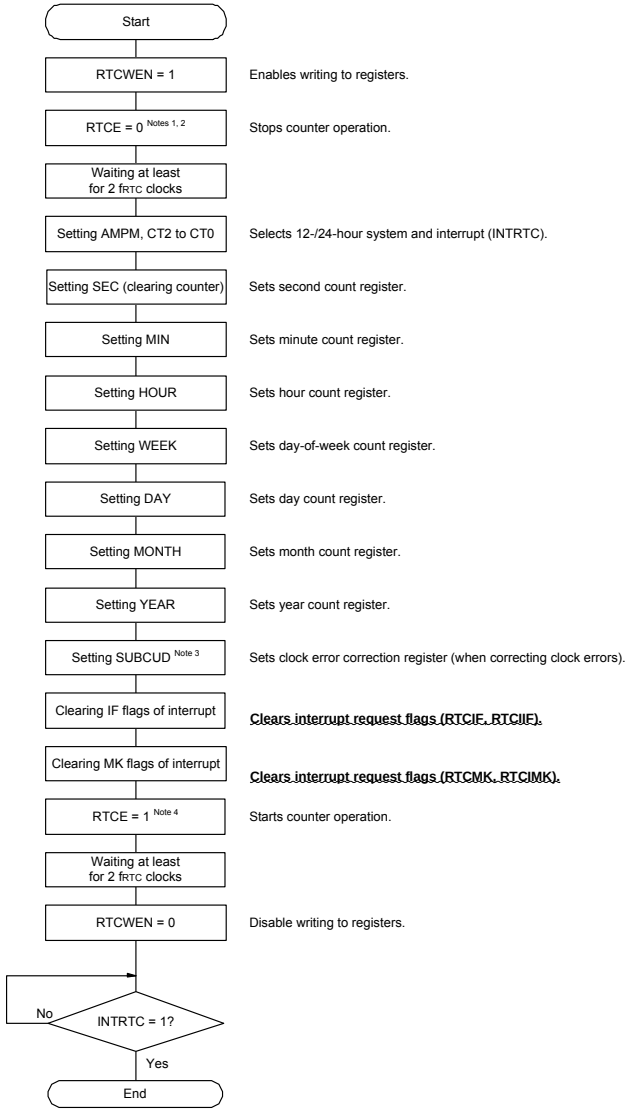
Caution 1. When using the real-time clock 2, first set the RTCWEN bit to 1, while oscillation of the input clock (fRTC)is stable. If RTCWEN = 0, writing to a control register of the real-time clock 2 is ignored.

Caution 2. Be sure to set bits 1 and 6 to 0

25. 8.4.1 Starting operation of real-time clock 2 (Page 469)

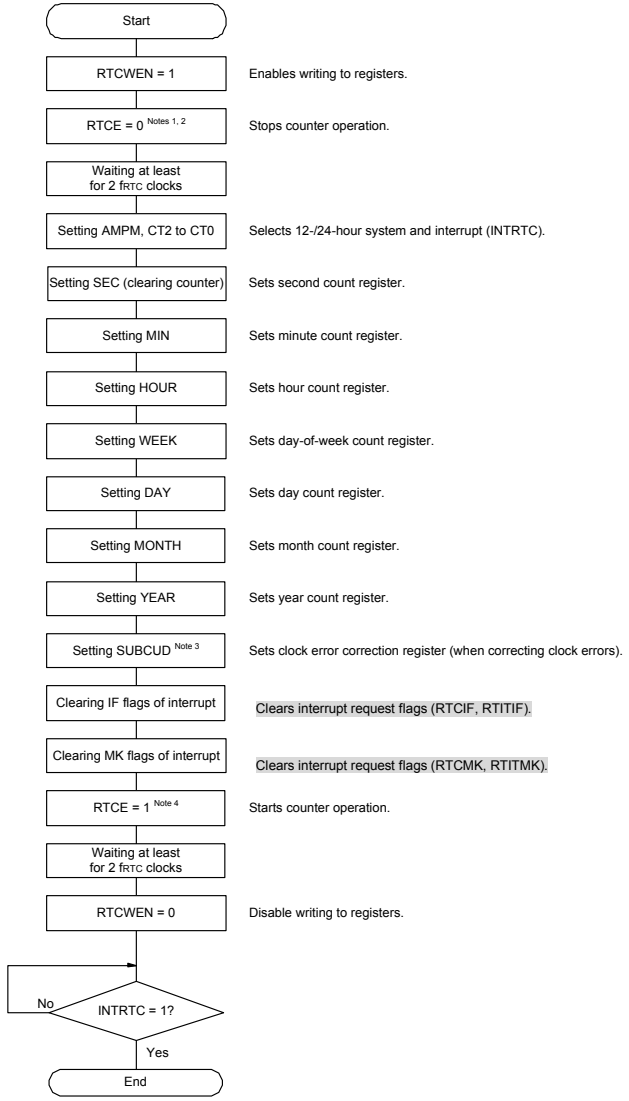
Incorrect:

Figure 8 - 20 Procedure for Starting Operation of Real-time Clock 2



Correct:

Figure 8 - 20 Procedure for Starting Operation of Real-time Clock 2



26. 12.3.1 Peripheral enableregister 0 (PER0) (Page 451)

Incorrect:

Figure 12 - 2 Format of Peripheral enable register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	1	<0>
PER0	RTCWEN Note	0	ADCEN	IICA0EN	SAU1EN	SAU0EN	0	TAU0EN

ADCEN	Control of A/D converter input clock supply
0	Stops input clock supply. · SFR used by the A/D converter cannot be written. · The A/D converter is in the reset status.
1	Enables input clock supply. · SFR used by the A/D converter can be read/written.

Note The RTCWEN bit is reset only by a power-on reset; it retains the value when a reset caused by another factor occurs.

Correct:

Figure 12 - 2 Format of Peripheral enable register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	1	<0>
PER0	RTCWEN	0	ADCEN	IICA0EN	SAU1EN	SAU0EN	0	TAU0EN

ADCEN	Control of A/D converter input clock supply
0	Stops input clock supply. · SFR used by the A/D converter cannot be written. · The A/D converter is in the reset status.
1	Enables input clock supply. · SFR used by the A/D converter can be read/written.

27. 15.3.1 Peripheral enableregister 0 (PER0) (Page 451)

Incorrect:

Figure 12 - 2 Format of Peripheral enable register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	1	<0>
PER0	RTCWEN Note	0	ADCEN	IICA0EN	SAU1EN	SAU0EN	0	TAU0EN

SAUmEN	Control of serial array unit m input clock supply
0	Stops supply of input clock. · SFR used by serial array unit m cannot be written. · Serial array unit m is in the reset status.
1	Enables input clock supply. · SFR used by serial array unit m can be read/written.

Note The RTCWEN bit is reset only by a power-on reset; it retains the value when a reset caused by another factor occurs.

Correct:

Figure 12 - 2 Format of Peripheral enable register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	1	<0>
PER0	RTCWEN	0	ADCEN	IICA0EN	SAU1EN	SAU0EN	0	TAU0EN

SAUmEN	Control of serial array unit m input clock supply
0	Stops supply of input clock. · SFR used by serial array unit m cannot be written. · Serial array unit m is in the reset status.
1	Enables input clock supply. · SFR used by serial array unit m can be read/written.

28. 16.3.1 Peripheral enableregister 0 (PER0) (Page 451)

Incorrect:

Figure 12 - 2 Format of Peripheral enable register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	1	<0>
PER0	RTCWEN Note	0	ADCEN	IICA0EN	SAU1EN	SAU0EN	0	TAU0EN

IICAnEN	Control of serial interface IICAn input clock supply
0	Stops input clock supply. · SFR used by serial interface IICAn cannot be written. · Serial interface IICAn is in the reset status
1	Enables input clock supply. · SFR used by serial interface IICAn can be read/written

Note The RTCWEN bit is reset only by a power-on reset; it retains the value when a reset caused by another factor occurs.

Correct:

Figure 12 - 2 Format of Peripheral enable register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	1	<0>
PER0	RTCWEN	0	ADCEN	IICA0EN	SAU1EN	SAU0EN	0	TAU0EN

IICAnEN	Control of serial interface IICAn input clock supply
0	Stops input clock supply. · SFR used by serial interface IICAn cannot be written. · Serial interface IICAn is in the reset status
1	Enables input clock supply. · SFR used by serial interface IICAn can be read/written

29. 34.1 Absolute Maximum Ratings (page 1172)

Incorrect:

Absolute Maximum Ratings (TA= 25°C) (3/3)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	IOH1	Per pin	P00-P07, P10-P17, P20-P27, P30-P37, P40-P46, P50-P57, P70-P77, P80-P83, P125-P127, P140-P143	-40	mA
		Total of all pins -170 mA	P40-P46	-70	mA
			P00-P07, P10-P17, P20-P27, P30-P37, P50-P57, P70-P77, P80-P83, P125-P127, P140-P143	-100	mA
	IOH2	Per pin	P130, P150-P156	-0.1	mA
		Total of all pins		-0.8	mA
	IOH3	Per pin	UDP, UDM	-3	mA
Output current, low	IOL1	Per pin	P00-P07, P10-P17, P20-P27, P30-P37, P40-P46, P50-P57, P60, P61, P70-P77, P80-P83, P125-P127, P140-P143	40	mA
		Total of all pins 170 mA	P40-P46	70	mA
			P00-P07, P10-P17, P20-P27, P30-P37, P50-P57, P70-P77, P80-P83, P125-P127, P140-P143	100	mA
	IOL2	Per pin	P130, P150-P156	0.4	mA
		Total of all pins		3.2	mA
	IOL3	1端子	UDP, UDM	3	mA

Correct:

Absolute Maximum Ratings (TA= 25°C) (3/3)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	IOH1	Per pin	P00-P07, P10-P17, P20-P27, P30-P37, P40-P46, P50-P57, P70-P77, P80-P83, P125-P127, P130, P140-P143	-40	mA
		Total of all pins -170 mA	P40-P46	-70	mA
			P00-P07, P10-P17, P20-P27, P30-P37, P50-P57, P70-P77, P80-P83, P125-P127, P130, P140-P143	-100	mA
	IOH2	Per pin	P150-P156	-0.1	mA
		Total of all pins		-0.7	mA
	IOH3	Per pin	UDP, UDM	-3	mA
Output current, low	IOL1	Per pin	P00-P07, P10-P17, P20-P27, P30-P37, P40-P46, P50-P57, P60, P61, P70-P77, P80-P83, P125-P127, P130, P140-P143	40	mA
		Total of all pins 170 mA	P40-P46	70	mA
			P00-P07, P10-P17, P20-P27, P30-P37, P50-P57, P70-P77, P80-P83, P125-P127, P130, P140-P143	100	mA
	IOL2	Per pin	P150-P156	0.4	mA
		Total of all pins		2.8	mA
	IOL3	Per pin	UDP, UDM	3	mA

30. 34.3.1 Pin characteristics (page 1175)

Incorrect:

(TA = -40～+85 ℃, 1.6 V≦AVDD = VDD≦3.6 V, VSS = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output Current, high Note1	IOH1	Per pin fot P00-P07, P10-P17, P20-P27, P30-P37, P40-P46, P50-P57, P70-P77, P80-P83, P125-P127, P140-P143				-10.0 Note2	mA
		Total of P00 to P07,P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P70 to P77, P80 to P83,P125 to P127, P140 to P143 (When duty = 70% Note 3)	2.7 V≦VDD≦3.6 V			-15.0	mA
			1.8 V≦VDD＜2.7 V			-7.0	mA
			1.6 V≦VDD＜1.8 V			-3.0	mA
	IOH2	Per pin for P130, P150-P156	1.6 V≦VDD≦3.6 V			-0.1 Note2	mA
		Total of all pins	1.6 V≦VDD≦3.6 V			-0.8	mA

Correct:

(TA = -40～+85 ℃, 1.6 V≦AVDD = VDD≦3.6 V, VSS = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output Current, high Note1	IOH1	per pin for P00-P07, P10-P17, P20-P27, P30-P37, P40-P46, P50-P57, P70-P77, P80-P83, P125-P127, P130, P140-P143				-10.0 Note2	mA
		Total of P00-P07, P10-P17, P20-P27, P30-P37, P40-P46, P50-P57, P70-P77, P80-P83, P125-P127, P130, P140-P143 (When duty = 70% Note 3)	2.7 V≦VDD≦3.6 V			-15.0	mA
			1.8 V≦VDD＜2.7 V			-7.0	mA
			1.6 V≦VDD＜1.8 V			-3.0	mA
	IOH2	Per pin for P150-P156	1.6 V≦VDD≦3.6 V			-0.1 Note2	mA
		Total of all pins	1.6 V≦VDD≦3.6 V			-0.7	mA

Incorrect:

(TA = -40～+85 ℃, 1.6 V≦AVDD = VDD≦3.6 V, VSS = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low Note 1	IOL1	Per pin for P00-P07, P10-P17, P20-P27, P30-P37, P40-P46, P50-P57, P60, P61, P70-P77, P80-P83, P125-P127, P140-P143				20.0 Note 2	mA
		Per pin P60, P61				15.0 Note 2	mA
		Total of P40-P46 (when duty = 70% Note 3)	2.7 V≦VDD≦3.6 V			15.0	mA
			1.8 V≦VDD＜2.7 V			9.0	mA
			1.6 V≦VDD＜1.8 V			4.5	mA
		Total of P00-P07, P10-P17, P20-P27, P30-P37, P50-P57, P60, P61, P70-P77, P80-P83, P125-P127, P140-P143 (when duty = 70% Note 3)	2.7 V≦VDD≦3.6 V			35.0	mA
			1.8 V≦VDD＜2.7 V			20.0	mA
			1.6 V≦VDD＜1.8 V			10.0	mA
		Total of all pins (when duty = 70% Note 3)				50.0	mA
	IOL2	Per pin for P130, P150-P156				0.4 Note 2	mA
		Total of all pins	1.6 V≦VDD≦3.6 V			3.2	mA

Correct:

(TA = -40～+85 ℃, 1.6 V≦AVDD = VDD≦3.6 V, VSS = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low Note 1	IOL1	Per pin for P00-P07, P10-P17, P20-P27, P30-P37, P40-P46, P50-P57, P60, P61, P70-P77, P80-P83, P125-P127, P130, P140-P143				20.0 Note 2	mA
		Per pin P60, P61				15.0 Note 2	mA
		Total of P40-P46 (when duty = 70% Note 3)	2.7 V≦VDD≦3.6 V			15.0	mA
			1.8 V≦VDD＜2.7 V			9.0	mA
			1.6 V≦VDD＜1.8 V			4.5	mA
		Total of P00-P07, P10-P17, P20-P27, P30-P37, P50-P57, P60, P61, P70-P77, P80-P83, P125-P127, P130, P140-P143 (when duty = 70% Note 3)	2.7 V≦VDD≦3.6 V			35.0	mA
			1.8 V≦VDD＜2.7 V			20.0	mA
			1.6 V≦VDD＜1.8 V			10.0	mA
		Total of all pins (when duty = 70% Note 3)				50.0	mA
	IOL2	Per pin for P150-P156				0.4 Note 2	mA
		Total of all pins	1.6 V≦VDD≦3.6 V			2.8	mA

31. 35.1 Absolute Maximum Ratings (pages 1239)

Incorrect:

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	IOH1	Per pin	P00-P07, P10-P17, P20-P27, P30-P37, P40-P46, P50-P57, P70-P77, P80-P83, P125-P127, P140-P143	-40	mA
		Total of all pins -170 mA	P40-P46	-70	mA
			P00-P07, P10-P17, P20-P27, P30-P37, P50-P57, P70-P77, P80-P83, P125-P127, P140-P143	-100	mA
	IOH2	Per pin	P130, P150-P156	-0.1	mA
		Total of all pins		-0.8	mA
	IOH3	Per pin	UDP, UDM	-3	mA
Output current, low	IOL1	Per pin	P00-P07, P10-P17, P20-P27, P30-P37, P40-P46, P50-P57, P60, P61, P70-P77, P80-P83, P125-P127, P140-P143	40	mA
		Total of all pins 170 mA	P40-P46	70	mA
			P00-P07, P10-P17, P20-P27, P30-P37, P50-P57, P70-P77, P80-P83, P125-P127, P140-P143	100	mA
	IOL2	Per pin	P130, P150-P156	0.4	mA
		Total of all pins		3.2	mA
	IOL3	1端子	UDP, UDM	3	mA

Correct:

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	IOH1	Per pin	P00-P07, P10-P17, P20-P27, P30-P37, P40-P46, P50-P57, P70-P77, P80-P83, P125-P127, P130, P140-P143	-40	mA
		Total of all pins -170 mA	P40-P46	-70	mA
			P00-P07, P10-P17, P20-P27, P30-P37, P50-P57, P70-P77, P80-P83, P125-P127, P130, P140-P143	-100	mA
	IOH2	Per pin	P150-P156	-0.1	mA
		Total of all pins		-0.7	mA
	IOH3	Per pin	UDP, UDM	-3	mA
Output current, low	IOL1	Per pin	P00-P07, P10-P17, P20-P27, P30-P37, P40-P46, P50-P57, P60, P61, P70-P77, P80-P83, P125-P127, P130, P140-P143	40	mA
		Total of all pins 170 mA	P40-P46	70	mA
			P00-P07, P10-P17, P20-P27, P30-P37, P50-P57, P70-P77, P80-P83, P125-P127, P130, P140-P143	100	mA
	IOL2	Per pin	P150-P156	0.4	mA
		Total of all pins		2.8	mA
	IOL3	1端子	UDP, UDM	3	mA

32. 35.3.1 Pin characteristics (page 1242)

Incorrect:

(TA = -40～+105 ℃, 2.4 V≦AVDD = VDD≦3.6 V, VSS = 0 V)

Items	Symbol	Conditions		MIN	TYP.	MAX.	Unit
Output current, high Note 1	IOH1	Per pin for P00-P07, P10-P17, P20-P27, P30-P37, P40-P46, P50-P57, P70-P77, P80-P83, P125-P127, P140-P143				-10.0 Note 2	mA
		Total of P00-P07, P10-P17, P20-P27, P30-P37, P40-P46, P50-P57, P70-P77, P80-P83, P125-P127, P140-P143 (when duty = 70% Note 3)	2.7 V≦VDD≦3.6 V			-15.0	mA
			2.4 V≦VDD＜2.7 V			-7.0	mA
	IOH2	Per pin for P130, P150-P156				-0.1 Note 2	mA
		Total of all pins	2.4 V≦VDD≦3.6 V			-0.8	mA

Correct:

(TA = -40～+105 ℃, 2.4 V≦AVDD = VDD≦3.6 V, VSS = 0 V)

Items	Symbol	Conditions		MIN	TYP.	MAX.	Unit
Output current, high Note 1	IOH1	Per pin for P00-P07, P10-P17, P20-P27, P30-P37, P40-P46, P50-P57, P70-P77, P80-P83, P125-P127, P130, P140-P143				-10.0 Note 2	mA
		Total of P00-P07, P10-P17, P20-P27, P30-P37, P40-P46, P50-P57, P70-P77, P80-P83, P125-P127, P130, P140-P143 (when duty = 70% Note 3)	2.7 V≦VDD≦3.6 V			-15.0	mA
			2.4 V≦VDD＜2.7 V			-7.0	mA
	IOH2	Per pin for P150-P156				-0.1 Note 2	mA
		Total of all pins	2.4 V≦VDD≦3.6 V			-0.7	mA

Incorrect:

(TA = -40～+105 ℃, 2.4 V≦AVDD = VDD≦3.6 V, VSS = 0 V)

Items	Symbol	Conditions		MIN	TYP.	MAX.	Unit
Output current, low Note 1	IOL1	Per pin for P00-P07, P10-P17, P20-P27, P30-P37, P40-P46, P50-P57, P60, P61, P70-P77, P80-P83, P125-P127, P140-P143				20.0 Note 2	mA
		Per pin for P60, P61				15.0 Note 2	mA
		Total of P40-P46 (when duty = 70% Note 3)	2.7 V≦VDD≦3.6 V			15.0	mA
			2.4 V≦VDD＜2.7 V			9.0	mA
		Total of P00-P07, P10-P17, P20-P27, P30-P37, P50-P57, P60, P61, P70-P77, P80-P83, P125-P127, P140-P143 (when duty = 70% Note 3)	2.7 V≦VDD≦3.6 V			35.0	mA
			2.4 V≦VDD＜2.7 V			20.0	mA
		Total of all pins(when duty = 70% Note 3)				50.0	mA
	IOL2	Per pin for P130, P150-P156				0.4 Note 2	mA
		Total of all pins	2.4 V≦VDD≦3.6 V			3.2	mA

Correct:

(TA = -40～+105 ℃, 2.4 V≦AVDD = VDD≦3.6 V, VSS = 0 V)

Items	Symbol	Conditions		MIN	TYP.	MAX.	Unit
Output current, low Note 1	IOL1	Per pin for P00-P07, P10-P17, P20-P27, P30-P37, P40-P46, P50-P57, P60, P61, P70-P77, P80-P83, P125-P127, P130, P140-P143				20.0 Note 2	mA
		Per pin for P60, P61				15.0 Note 2	mA
		Total of P40-P46 ((when duty = 70% Note 3)	2.7 V≦VDD≦3.6 V			15.0	mA
			2.4 V≦VDD＜2.7 V			9.0	mA
		Total of P00-P07, P10-P17, P20-P27, P30-P37, P50-P57, P60, P61, P70-P77, P80-P83, P125-P127, P130, P140-P143 (when duty = 70% Note 3)	2.7 V≦VDD≦3.6 V			35.0	mA
			2.4 V≦VDD＜2.7 V			20.0	mA
		Total of all pins (when duty = 70% Note 3)				50.0	mA
	IOL2	Per pin for P150-P156				0.4 Note 2	mA
		Total of all pins	2.4 V≦VDD≦3.6 V			2.8	mA