Date: Feb. 24, 2016

# RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

| Product Category | MPU/MCU | | Document No. | TN-RL*-A055B/E | Rev. | 2.00 |
|---|---|---|---|---|---|---|
| Title | Correction for Incorrect Description Notice<br>RL78/G1C Descriptions in the User's Manual: Hardware Rev. 1.10 Changed | | Information Category | Technical Notification | | |
| Applicable Product | RL78/G1C Group | Lot No.<br>All Lots | Reference Document | RL78/G1C User's Manual: Hardware Rev. 1.10<br>R01UH0348EJ0110 (Nov. 2013) | | |

This document describes misstatements found in the RL78/G1C User's Manual: Hardware Rev. 1.10 (R01UH0348EJ0110).

## Corrections

| Applicable Item | Applicable Page | Contents |
|---|---|---|
| 2.4 Block Diagrams of Pins Figure 2-7. Pin Block Diagram for Pin Type 7-1-4 | Page 32 | Caution added |
| 2.4 Block Diagrams of Pins Figure 2-9. Pin Block Diagram for Pin Type 8-1-4 | Page 34 | Caution added |
| 2.4 Block Diagrams of Pins Figure 2-10. Pin Block Diagram for Pin Type 8-3-4 | Page 35 | Caution added |
| 3.2.5 Extended special function registers (2nd SFRs: 2nd Special Function Registers) | Page 66 | Incorrect descriptions revised |

## Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

## Corrections in the User's Manual: Hardware

| No | Corrections and Applicable Items | | | | Pages in this document for corrections |
|---|---|---|---|---|---|
| | | Document No. | English | R01UH0348EJ0110 | |
| **1** | 5.3.10 PLL control register (DSCCTL) | | | Page 136 | Page 3 |
| **2** | 5.4.5 PLL (Phase Locked Loop) | | | Page 142 | Page 4 |
| **3** | 5.6.4 Example of setting PLL circuit | | | Page 148 | Pages 6 to 7 |
| **4** | 5.6.5 CPU clock status transition diagram | | | Page 149 | Page 8 |
| **5** | 5.6.5 CPU clock status transition diagram Table 5-4. CPU Clock Transition and SFR Register Setting Examples | | | Pages 150 to 154 | Pages 9 to 15 |
| **6** | 5.6.6 Condition before changing CPU clock and processing after changing CPU clock | | | Pages 157 to 168 | Pages 16 to 17 |
| **7** | 7.3.4 Real-time clock control register 1 (RTCC1) | | | Page 280 | Page 18 |
| **8** | 2.4 Block Diagrams of Pins Figure 2-7. Pin Block Diagram for Pin Type 7-1-4 | | | Page 32 | Page 19 |
| **9** | 2.4 Block Diagrams of Pins Figure 2-9. Pin Block Diagram for Pin Type 8-1-4 | | | Page 34 | Page 20 |
| **10** | 2.4 Block Diagrams of Pins Figure 2-10. Pin Block Diagram for Pin Type 8-3-4 | | | Page 35 | Page 21 |
| **11** | 3.2.5 Extended special function registers (2nd SFRs: 2nd Special Function Registers) | | | Page 66 | Page 22 |

**Incorrect, Old: Bold with underline**; Correct, New: Gray hatched

## Revision History

RL78/G1C Correction for incorrect description notice

| Document Number | Issue Date | Description |
|---|---|---|
| TN-RL*-A046A/E | Jul. 6 , 2015 | Correction No.7 revised |
| TN-RL*-A055A/E | Oct. 28, 2015 | First edition issued<br>Corrections No.1 to No.6 revised |
| TN-RL*-A055B/E | Feb. 24, 2016 | Second edition issued<br>Corrections No.8 to No.11 revised (This document) |

## 1. 5.3.10 PLL control register (DSCCTL) (Page 136)

Additional entry to Figure 5 - 11 Format of PLL control register (DSCCTL)

**Old:**

**Figure 5-11. Format of PLL Control Register (DSCCTL)**

Address: F02E5H After reset: 00H R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| DSCCTL | 0 | 0 | 0 | 0 | 0 | DSFRDIV | DSCM | DSCON |

| DSFRDIV | PLL reference clock divider control |
|---|---|
| 0 | No division |
| 1 | Divided by 2 |

**Remark** PLL reference clock is the high-speed system clock ($f_{MX}$).

| DSCM | PLL multiplication selection |
|---|---|
| 0 | 12 times (6 times) |
| 1 | 16 times (8 times) |

**Remark** The frequency is divided by 2 in the last stage of the PLL oscillator, therefore the multiplication ratio becomes the value in parentheses.

| DSCON | PLL oscillation and output control |
|---|---|
| 0 | Stop |
| 1 | Ocsillation, output |

**Caution Be sure to clear bits 3 to 7 to 0.**

**New:**

**Figure 5-11. Format of PLL Control Register (DSCCTL)**

Address: F02E5H After reset: 00H R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| DSCCTL | 0 | 0 | 0 | 0 | 0 | DSFRDIV | DSCM | DSCON |

| DSFRDIV | PLL reference clock divider control |
|---|---|
| 0 | No division |
| 1 | Divided by 2 |

**Remark** PLL reference clock is the high-speed system clock ($f_{MX}$).

| DSCM | PLL multiplication selection |
|---|---|
| 0 | 12 times (6 times) |
| 1 | 16 times (8 times) |

**Remark** The frequency is divided by 2 in the last stage of the PLL oscillator, therefore the multiplication ratio becomes the value in parentheses.

| DSCON | PLL oscillation and output control |
|---|---|
| 0 | Stop |
| 1 | Ocsillation, output |

Caution 1. Be sure to clear bits 3 to 7 to 0.

Caution 2. Be sure to set the DSCON bit to 0 before changing DSFRDIV and DSCM.

Caution 3. Do not set the DSCON bit to 0 while the PLL clock is selected as the system clock.

## 2. 5.4.5 PLL (Phase Locked Loop) (Page 142)

Incorrect descriptions revised to Caution 2.

**Old:**

Caution 1. When switching from PLL mode to the internal high-speed oscillation clock and the high speed system clock, stop the function (USB function controller) that provides the PLL output clock ($f_{PLL}$).

**Caution 2. PLL operations cannot be performed while the subsystem clock is operating**

**New:**

Caution 1. When switching from PLL mode to the internal high-speed oscillation clock and the high speed system clock, stop the function (USB function controller) that provides the PLL output clock ($f_{PLL}$).

Caution 2. Do not set the DSCON bit to 1 to start the PLL operating while the subsystem clock is the operating clock for the CPU.

## 3. 5.6.4 Example of setting PLL circuit (Page 148)

Incorrect descriptions revised to 5.6.4 Example of setting PLL circuit.

### Old:

[Register settings] Set the register in the order of <1> to <5> below.

<1> Set the DSFRDIV bit and DSCM bit in the DSCCTL register to set the PLL multiplication and division.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| DSCCTL | 0 | 0 | 0 | 0 | 0 | DSFRDIV 0/1 | DSCM 0/1 | DSCON 0 |

<2> Set the RDIV1, RDIV0 bits of the MCKC register to set the division of the system clock.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| MCKC | 0 | 0 | 0 | 0 | 0 | RDIV1 0/1 | RDIV0 0/1 | CKSELR 0 |

AMPHS0 and AMPHS1 bits: These bits are used to specify the oscillation mode of the XT1 oscillator.

<3> Set (1) the DSCON bit of the DSCCTL register to operate the PLL circuit Note.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| DSCCTL | 0 | 0 | 0 | 0 | 0 | DSFRDIV 0/1 | DSCM 0/1 | DSCON 1 |

**<4> Wait for 40 μs by using software.**

<5> Set (1) the CKSELR bit of the MCKC register to select PLL output for the system clock.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| MCKC | 0 | 0 | 0 | 0 | 0 | RDIV1 0/1 | RDIV0 0/1 | CKSELR 1 |

**Note** After the X1 oscillator clock stabilizes, allow at least 1 μs to elapse before operating the PLL. When operating the PLL again after it has been stopped, wait for at least 4 μs before operating.

### New:

[Register settings] Set the register in the order of <1> to <5> below.

<1> Set the HIOSTOP bit in the CSC register to make the high-speed on-chip oscillator run.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| CSC | 0/1 | 0/1 | 0 | 0 | 0 | 0 | 0 | HIOSTOP 0 Note1 |

<2> Set the DSFRDIV bit and DSCM bit in the DSCCTL register to set the PLL multiplication and division.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| DSCCTL | 0 | 0 | 0 | 0 | 0 | DSFRDIV 0/1 | DSCM 0/1 | DSCON 0 |

<3> Set the RDIV1, RDIV0 bits of the MCKC register to set the division of the system clock.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| MCKC | 0 | 0 | 0 | 0 | 0 | RDIV1 0/1 | RDIV0 0/1 | CKSELR 0 |

AMPHS0 and AMPHS1 bits: These bits are used to specify the oscillation mode of the XT1 oscillator.

<4> Set (1) the DSCON bit of the DSCCTL register to operate the PLL circuit Note.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| DSCCTL | 0 | 0 | 0 | 0 | 0 | DSFRDIV 0/1 | DSCM 0/1 | DSCON 1 |

<5> Set (1) the CKSELR bit of the MCKC register to select PLL output for the system clock.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| MCKC | 0 | 0 | 0 | 0 | 0 | RDIV1 0/1 | RDIV0 0/1 | CKSELR 1 |

<6> Use software to set up a wait of 65 μs.[Note3]

<7> Set the HIOSTOP bit in the CSC register to stop the high-speed on-chip oscillator.[Note2]

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| CSC | 0/1 | 0/1 | 0 | 0 | 0 | 0 | 0 | HIOSTOP 1[Note1] |

<8> When the PLL clock frequency divided by 2, 4, or 8 is selected as the main system clock ($f_{MAIN}$), set the MCM0 bit in the CKC register to select the source for deriving the main system clock as a signal with a frequency ($f_{IH}$) of up to 24 MHz.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| CKC | CLS 0/1 | CSS 0/1 | MCS 0 | MCM0 0 | 0 | 0 | 0 | 0 |

Note 1. No setting is required to change to the PLL while the CKSELR bit is 1.
When setting the CKSELR bit to 1, ensure that the high-speed on-chip oscillator is running.

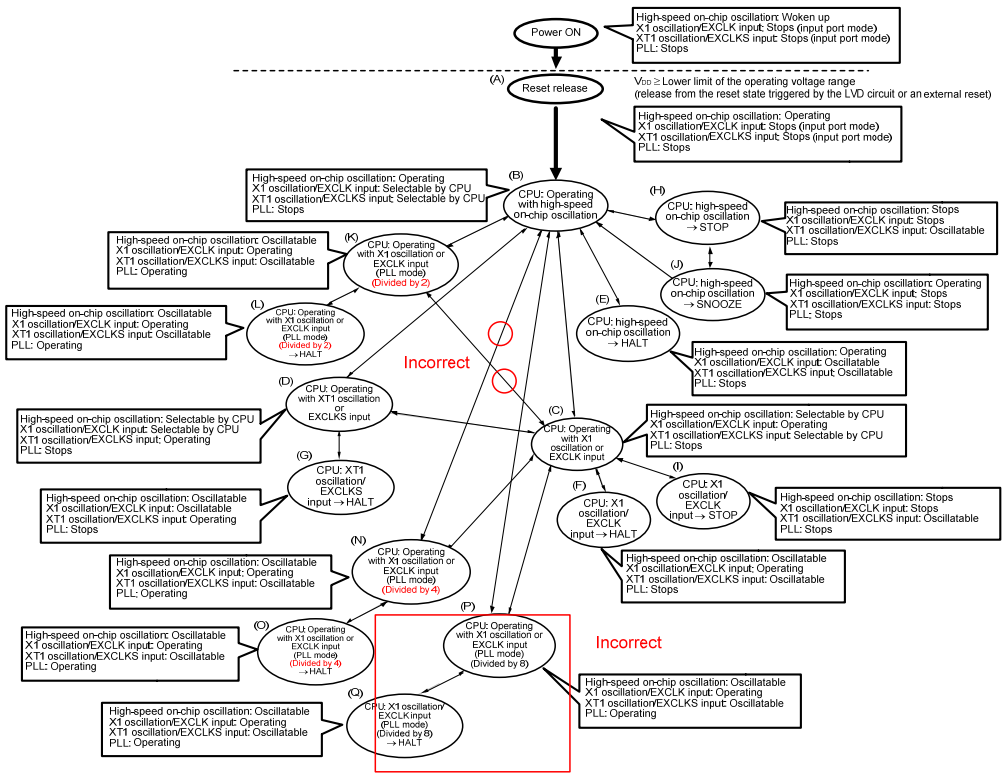
Note 2. After oscillation by the X1 oscillator clock has become stable, allow at least 1 μs to elapse before starting the PLL. When restarting the PLL after it has been stopped, wait for at least 4 μs before using it in operations.

Note 3. Wait for 40 μs for oscillation by the oscillator clock to become stabled if the HIOSTOP bit is not set to 0.

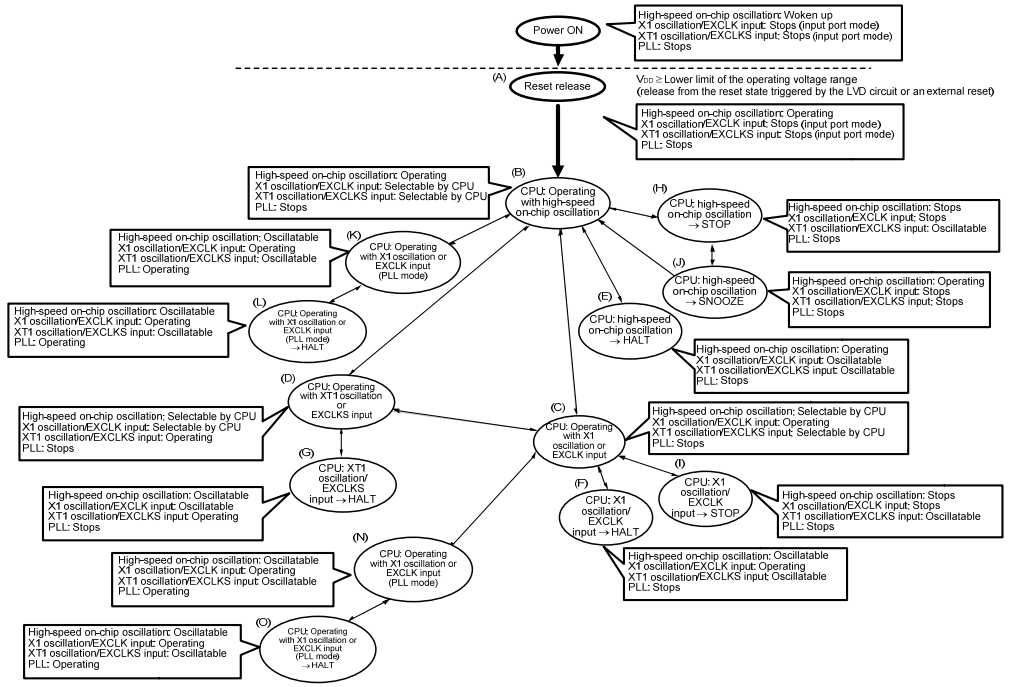
## 4. 5.6.5 CPU clock status transition diagram (Page 149)

Incorrect descriptions revised to Figure 5 - 18 CPU Clock Status Transition Diagram

**Old:**




**New:**



**5. 5.6.5 CPU clock status transition diagram**

**Table 5 - 4 CPU Clock Transition and SFR Register Setting Examples (pages 150 to 154)**

**Old:**

(2) CPU operating with high-speed system clock (C) after reset release (A)

(The CPU operates with the high-speed on-chip oscillator clock immediately after a reset release (B).)

(Setting sequence of SFR registers) ⟶

| Setting Flag of SFR Register / Status Transition | CMC Register Note 1 | | | OSTS Register | CSC Register | OSTC Register | CKC Register |
|---|---|---|---|---|---|---|---|
| | EXCLK | OSCSEL | AMPH | | MSTOP | | MCM0 |
| (A) → (B) → (C)<br>(X1 clock: 1 MHz ≤ fx ≤ 10 MHz) | 0 | 1 | 0 | **Note 2** | 0 | Must be checked | 1 |
| (A) → (B) → (C)<br>(X1 clock: 10 MHz < fx ≤ 20 MHz) | 0 | 1 | **0** | **Note 2** | 0 | Must be checked | 1 |
| (A) → (B) → (C)<br>(external main clock) | 1 | 1 | × | **Note 2** | 0 | Must not be checked | 1 |

**New:**

(2) CPU operating with high-speed system clock (C) after reset release (A)

(The CPU operates with the high-speed on-chip oscillator clock immediately after a reset release (B).)

(Setting sequence of SFR registers) ⟶

| Setting Flag of SFR Register / Status Transition | CMC Register Note 1 | | | OSTS Register | CSC Register | OSTC Register | CKC Register |
|---|---|---|---|---|---|---|---|
| | EXCLK | OSCSEL | AMPH | | MSTOP | | MCM0 |
| (A) → (B) → (C)<br>(X1 clock: 1 MHz ≤ fx ≤ 10 MHz) | 0 | 1 | 0 | **Note 2** | 0 | Must be checked | 1 |
| (A) → (B) → (C)<br>(X1 clock: 10 MHz < fx ≤ 20 MHz) | 0 | 1 | 1 | **Note 2** | 0 | Must be checked | 1 |
| (A) → (B) → (C)<br>(external main clock) | 1 | 1 | × | **Note 2** | 0 | Must not be checked | 1 |

**Old:**

(4) CPU clock changing from high-speed on-chip oscillator clock (B) to high-speed system clock (C)

(Setting sequence of SFR registers) →

| Setting Flag of SFR Register / Status Transition | CMC Register Note 1 | | | OSTS Register | CSC Register | OSTC Register | CKC Register |
|---|---|---|---|---|---|---|---|
| | EXCLK | OSCSEL | AMPH | | MSTOP | | MCM0 |
| (B) → (C) (X1 clock: 1 MHz ≤ $f_X$ ≤ 10 MHz) | 0 | 1 | 0 | **Note 2** | 0 | Must be checked | 1 |
| (B) → (C) (X1 clock: 10 MHz < $f_X$ ≤ 20 MHz) | 0 | 1 | 1 | **Note 2** | 0 | Must be checked | 1 |
| (B) → **(D)** (external main clock) | 1 | 1 | × | **Note 2** | 0 | Must not be checked | 1 |

Unnecessary if these registers are already set

Unnecessary if the CPU is operating with the high-speed system clock

(6) CPU clock changing from high-speed system clock (C) to high-speed on-chip oscillator clock (B)

(Setting sequence of SFR registers) →

| Setting Flag of SFR Register / Status Transition | CSC Register | Oscillation accuracy stabilization time | CKC Register |
|---|---|---|---|
| | HIOSTOP | | MCM0 |
| (C) → (B) | 0 | Note | 0 |

Unnecessary if the CPU is operating with the high-speed on-chip oscillator clock

Note When FRQSEL4 = 0: 18 μs to 65 μs

**When FRQSEL4 = 1: 18 μs to 75 μs**

**New:**

(4) CPU clock changing from high-speed on-chip oscillator clock (B) to high-speed system clock (C)

(Setting sequence of SFR registers) →

| Setting Flag of SFR Register / Status Transition | CMC Register Note 1 | | | OSTS Register | CSC Register | OSTC Register | CKC Register |
|---|---|---|---|---|---|---|---|
| | EXCLK | OSCSEL | AMPH | | MSTOP | | MCM0 |
| (B) → (C) (X1 clock: 1 MHz ≤ $f_X$ ≤ 10 MHz) | 0 | 1 | 0 | **Note 2** | 0 | Must be checked | 1 |
| (B) → (C) (X1 clock: 10 MHz < $f_X$ ≤ 20 MHz) | 0 | 1 | 1 | **Note 2** | 0 | Must be checked | 1 |
| (B) → (C) (external main clock) | 1 | 1 | × | **Note 2** | 0 | Must not be checked | 1 |

Unnecessary if these registers are already set

Unnecessary if the CPU is operating with the high-speed system clock

(6) CPU clock changing from high-speed system clock (C) to high-speed on-chip oscillator clock (B)

(Setting sequence of SFR registers) →

| Setting Flag of SFR Register / Status Transition | CSC Register | Oscillation accuracy stabilization time | CKC Register |
|---|---|---|---|
| | HIOSTOP | | MCM0 |
| (C) → (B) | 0 | Note | 0 |

Unnecessary if the CPU is operating with the high-speed on-chip oscillator clock

Note When FRQSEL4 = 0: 18 μs to 65 μs

When FRQSEL4 = 1: 18 μs to 135 μs

**Old:**

(8) CPU clock changing from subsystem clock (D) to high-speed on-chip oscillator clock (B)

(Setting sequence of SFR registers) →

| Setting Flag of SFR Register / Status Transition | CSC Register HIOSTOP | Oscillation accuracy stabilization time | CKC Register CSS |
|---|---|---|---|
| (D) → (B) | 0 | Note | 0 |

Unnecessary if the CPU is operating with the high-speed on-chip oscillator clock

Note When FRQSEL4 = 0: 18 μs to 65 μs

**When FRQSEL4 = 1: 18 μs to 75 μs**

**New:**

(8) CPU clock changing from subsystem clock (D) to high-speed on-chip oscillator clock (B)

(Setting sequence of SFR registers) →

| Setting Flag of SFR Register / Status Transition | CSC Register HIOSTOP | Oscillation accuracy stabilization time | CKC Register CSS |
|---|---|---|---|
| (D) → (B) | 0 | Note | 0 |

Unnecessary if the CPU is operating with the high-speed on-chip oscillator clock

Note When FRQSEL4 = 0: 18 μs to 65 μs

When FRQSEL4 = 1: 18 μs to 135 μs

**Old:**

(10) • **CPU clock changing from high-speed on-chip oscillator clock (B) to high-speed system clock (PLL mode) (divided by 2) (K)**

• **CPU clock changing from high-speed on-chip oscillator clock (B) to high-speed system clock (PLL mode) (divided by 4) (N)**

• **CPU clock changing from high-speed on-chip oscillator clock (B) to high-speed system clock (PLL mode) (divided by 8) (P)**

• CPU clock changing from high-speed system clock (C) to high-speed system clock (PLL mode) **(divided by 2)** (K)

• **CPU clock changing from high-speed system clock (C) to high-speed system clock (PLL mode) (divided by 4) (N)**

• **CPU clock changing from high-speed system clock (C) to high-speed system clock (PLL mode) (divided by 8) (P)**

(Setting sequence of SFR registers) ——————————→

| Setting Flag of SFR Register / Status Transition | DSCCTL Register | | MCKC Register | | Waiting for Oscillation Stabilization | MCKC Register |
|---|---|---|---|---|---|---|
| | DSFRDIV | DSCM | RDIV1 | RDIV0 | | CKSELR |
| (B) → (K) | 0/1 | 0/1 | 0/1 | 0/1 | 40 μs | 1 |
| (B) → (N) | | | | | | |
| (B) → (P) | | | | | | |
| (C) → (K) | | | | | | |
| (C) → (N) | | | | | | |
| (C) → (P) | | | | | | |

**New:**

(10) • CPU clock changing from high-speed on-chip oscillator clock (B) to high-speed system clock (PLL mode) (K)

• CPU clock changing from high-speed system clock (C) to high-speed system clock (PLL mode) (N)

Continue

(Setting sequence of SFR registers) ▶

| Setting Flag of SFR Register / Status Transition | CMC Register Note 1 | | | OSTS Register | CSC Register | OSTC Register | DSCCTL Register | | MCKC Register | | Waiting for Oscillation Stabilization | DSCCTL Register | Waiting for Oscillation Stabilization | MCKC Register |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | EXCLK | OSCSEL | AMPH | | MSTOP | | DSFRDIV | DSCM | RDIV1 | RDIV0 | | DSCON | | CKSELR |
| (B) → (K) (divided by 2) | 0/1 | 1 | 0/1 | Note 2 | 0 | Must be checked | 0/1 | 0/1 | 0 | 0 | 1us | 1 | 40us | 1 |
| (B) → (K) (divided by 4) | 0/1 | 1 | 0/1 | Note 2 | 0 | Must be checked | 0/1 | 0/1 | 0 | 1 | | 1 | | 1 |
| (B) → (K) (divided by 8) | 0/1 | 1 | 0/1 | Note 2 | 0 | Must be checked | 0/1 | 0/1 | 1 | 0 | | 1 | | 1 |

Note 1. Writing to the clock operating mode control register (CMC) can only proceed once and must be by an 8-bit memory manipulation instruction after release from the reset state.

Note 2. Set the oscillation stabilization time in the oscillation stabilization time select register (OSTS) as follows.

• Desired oscillation stabilization time setting of the oscillation stabilization time counter status register (OSTC) ≤ Oscillation stabilization time set in the OSTS register

Caution: Completion of clock switching after the CKSELR bit has been set to 1 requires up to 2 clock cycles when the FRQSEL4 bit is 1, and up to 10 clock cycles when the FRQSEL4 bit is 0. Until the clock switching is completed, do not stop the high-speed on-chip oscillator.

(Setting sequence of SFR registers) ▶

| Setting Flag of SFR Register / Status Transition | CSC Register | DSCCTL Register | | MCKC Register | | DSCCTL Register | MCKC Register | Waiting for Oscillation Stabilization | CSC Register | CKC Register |
|---|---|---|---|---|---|---|---|---|---|---|
| | HIOSTOP | DSFRDIV | DSCM | RDIV1 | RDIV0 | DSCON | CKSELR | | HIOSTOP | MCM0 |
| (C) → (N) (divided by 2) | 0 Note3 | 0/1 | 0/1 | 0 | 0 | 1 | 1 Note3 | 135us Note4 | 1 Note3 | 0 |
| (C) → (N) (divided by 2) | 0 Note3 | 0/1 | 0/1 | 0 | 1 | 1 | 1 Note3 | | 1 Note3 | 0 |
| (C) → (N) (divided by 2) | 0 Note3 | 0/1 | 0/1 | 1 | 0 | 1 | 1 Note3 | | 1 Note3 | 0 |

Note 3. No setting is required to change to the PLL while the CKSELR bit is 1. When setting the CKSELR bit to 1, ensure that the high-speed on-chip oscillator is running.

Note 4. Wait for 40 μs for oscillation by the oscillator clock to become stable if the HIOSTOP bit is not set to 0

**Old:**

(11) • CPU clock changing from high-speed system clock (PLL mode) **(divided by 2)** (K) to high-speed on-chip oscillator clock (B)

**• CPU clock changing from high-speed system clock (PLL mode) (divided by 4) (N) to high-speed on-chip oscillator clock (B)**

**• CPU clock changing from high-speed system clock (PLL mode) (divided by 8) (P) to high-speed on-chip oscillator clock (B)**

• CPU clock changing from high-speed system clock (PLL mode) (divided by 2) (K) to high-speed system clock (C)

**• CPU clock changing from high-speed system clock (PLL mode) (divided by 4) (N) to high-speed system clock (C)**

**• CPU clock changing from high-speed system clock (PLL mode) (divided by 8) (P) to high-speed system clock (C)**

(Setting sequence of SFR registers) ——————————→

| Setting Flag of SFR Register / Status Transition | MCKC Register | DSCCTL Register |
|---|---|---|
| | CKSELR | DSCON |
| (K) → (B)<br>(N) → (B)<br>(P) → (B)<br>(K) → (C)<br>(N) → (C)<br>(P) → (C) | 0 | 0 |

**New:**

(11) • CPU clock changing from high-speed system clock (PLL mode) (K) to high-speed on-chip oscillator clock (B)

• CPU clock changing from high-speed system clock (PLL mode) (N) to high-speed system clock (C)

| Setting Flag of SFR Register / Status Transition | CSC Register | Waiting for Oscillation Stabilization | MCKC Register | Waiting for clock change | DSCCTL Register |
|---|---|---|---|---|---|
| | HIOSTOP | | CKSELR | | DSCON |
| (K) → (B) FRQSEL4=0 | 0 | 18～65 μs | 0 | 256 clokc | 0 |
| (K) → (B) FRQSEL4=1 | | 18～135 μs | | 16 clock | |

Continue

(Setting sequence of SFR registers) ⟶

| Status Transition \ Setting Flag of SFR Register | CKC Register MCM0 | Waiting for clock change | DSCCTL Register DSCON |
|---|---|---|---|
| (N) → (C) (divided by 2) (RDIV1,0 = 00) High-speed system clock (fMX) = 16MHz | 1 | 3 Clock | 0 |
| (N) → (C) (divided by 2) (RDIV1,0 = 00) High-speed system clock (fMX) = 12MHz | | 4 Clock | |
| (N) → (C) (divided by 2) (RDIV1,0 = 00) High-speed system clock (fMX) = 8MHz | | 6 Clock | |
| (N) → (C) (divided by 2) (RDIV1,0 = 00) High-speed system clock (fMX) = 6MHz | | 8 Clock | |
| (N) → (C) (divided by 4) (RDIV1,0 = 01) High-speed system clock (fMX) = 16MHz | | 2 Clock | |
| (N) → (C) (divided by 4) (RDIV1,0 = 01) High-speed system clock (fMX) = 12MHz | | 2 Clock | |
| (N) → (C) (divided by 4) (RDIV1,0 = 01) High-speed system clock (fMX) = 8MHz | | 3 Clock | |
| (N) → (C) (divided by 4) (RDIV1,0 = 01) High-speed system clock (fMX) = 6MHz | | 4 Clock | |
| (N) → (C) (divided by 8) (RDIV1,0 = 10) High-speed system clock (fMX) = 16MHz | | 2 Clock | |
| (N) → (C) (divided by 8) (RDIV1,0 = 10) High-speed system clock (fMX) = 12MHz | | 2 Clock | |
| (N) → (C) (divided by 8) (RDIV1,0 = 10) High-speed system clock (fMX) = 8MHz | | 2 Clock | |
| (N) → (C) (divided by 8) (RDIV1,0 = 10) High-speed system clock (fMX) = 6MHz | | 2 Clock | |

**Old:**

(12) • HALT mode (E) set while CPU is operating with high-speed on-chip oscillator clock (B)

• HALT mode (F) set while CPU is operating with high-speed system clock (C)

• HALT mode (G) set while CPU is operating with subsystem clock (D)

• HALT mode (L) set while CPU is operating with high-speed system clock (PLL mode) **(divided by 2)** (K)

**• HALT mode (O) set while CPU is operating with high-speed system clock (PLL mode) (divided by 4) (N)**

**• HALT mode (Q) set while CPU is operating with high-speed system clock (PLL mode) (divided by 8) (P)**

| Status Transition | Setting |
|---|---|
| (B) → (E)<br>(C) → (F)<br>(D) → (G)<br>(K) → (L)<br>**(N) → (Q)**<br>**(P) → (Q)** | Executing HALT instruction |

(15) • STOP mode (I) set while CPU is operating with high-speed system clock (PLL mode) **(divided by 2)** (K)

**・ STOP mode (I) set while CPU is operating with high-speed system clock (PLL mode) (divided by 4) (N)**

**・ STOP mode (I) set while CPU is operating with high-speed system clock (PLL mode) (divided by 8) (P)**

Switch from PLL mode operation to **high-speed on-chip oscillator clock** and high-speed system clock operations

**(refer to 5.6.5 (11))** and stop the PLL (DSCON = 0), then execute the STOP instruction

**New:**

(12) • HALT mode (E) set while CPU is operating with high-speed on-chip oscillator clock (B)

• HALT mode (F) set while CPU is operating with high-speed system clock (C)

• HALT mode (G) set while CPU is operating with subsystem clock (D)

• HALT mode (L) set while CPU is operating with high-speed system clock (PLL mode) (K)

• HALT mode (O) set while CPU is operating with high-speed system clock (PLL mode) (N)

| Status Transition | Setting |
|---|---|
| (B) → (E)<br>(C) → (F)<br>(D) → (G)<br>(K) → (L)<br>(N) → (O) | Executing HALT instruction |

(15) • Changing to STOP mode (I) from the high-speed system clock (PLL mode) as the operating clock for the CPU (K)

Switch to high-speed system clock operation from PLL mode, stop the PLL (DSCON = 0), and then execute the STOP instruction.

## 6.5.6.6 Condition before changing CPU clock and processing after changing CPU clock (pages 157 158)

**Old:**

**Table 5-5. Changing CPU Clock (1/3)**

| CPU Clock | | Condition Before Change | Processing After Change |
|---|---|---|---|
| Before Change | After Change | | |
| X1 clock | (omitted) | | |
| | PLL clock | Oscillation of PLL<br>• DSCON = 1 | – |

**New:**

**Table 5-5. Changing CPU Clock (1/3)**

| CPU Clock | | Condition Before Change | Processing After Change |
|---|---|---|---|
| Before Change | After Change | | |
| X1 clock | (omitted) | | |
| | PLL clock | Oscillation of PLL<br>• DSCON = 1<br>Enabling oscillation of high-speed on-chip oscillator<br>· HIOSTOP = 0<br>· The oscillation accuracy stabilization time has elapsed | – |

**Old:**

**Table 5-5. Changing CPU Clock (2/3)**

| CPU Clock | | Condition Before Change | Processing After Change |
|---|---|---|---|
| Before Change | After Change | | |
| External main system clock | High-speed on-chip oscillator clock | Enabling oscillation of high-speed on-chip oscillator<br>• HIOSTOP = 0<br>• After elapse of oscillation accuracy stabilization time | External main system clock input can be disabled (MSTOP = 1). |
| | X1 clock | Transition not possible | – |
| | XT1 clock | Stabilization of XT1 oscillation<br>• OSCSELS = 1, EXCLKS = 0, XTSTOP = 0<br>• After elapse of oscillation stabilization time | External main system clock input can be disabled (MSTOP = 1). |
| | External subsystem clock | Enabling input of external clock from the EXCLKS pin<br>• OSCSELS = 1, EXCLKS = 1, XTSTOP = 0 | External main system clock input can be disabled (MSTOP = 1). |
| | PLL clock | Oscillation of PLL<br>• DSCON = 1 | – |
| (omitted) | | | |

**New:**

**Table 5-5. Changing CPU Clock (2/3)**

| CPU Clock | | Condition Before Change | Processing After Change |
|---|---|---|---|
| Before Change | After Change | | |
| External main system clock | High-speed on-chip oscillator clock | Enabling oscillation of high-speed on-chip oscillator<br>• HIOSTOP = 0<br>• After elapse of oscillation accuracy stabilization time | External main system clock input can be disabled (MSTOP = 1). |
| | X1 clock | Transition not possible | – |
| | XT1 clock | Stabilization of XT1 oscillation<br>• OSCSELS = 1, EXCLKS = 0, XTSTOP = 0<br>• After elapse of oscillation stabilization time | External main system clock input can be disabled (MSTOP = 1). |
| | External subsystem clock | Enabling input of external clock from the EXCLKS pin<br>• OSCSELS = 1, EXCLKS = 1, XTSTOP = 0 | External main system clock input can be disabled (MSTOP = 1). |
| | PLL clock | Oscillation of PLL<br>• DSCON = 1<br>Enabling oscillation of high-speed on-chip oscillator<br>· HIOSTOP = 0<br>· The oscillation accuracy stabilization time has elapsed | – |
| (omitted) | | | |

## 7. 7.3.4 Real-time clock control register 1 (RTCC1)

Additional entry to Figure 7 - 5 Format of Real-time clock control register 1 (RTCC1) (2/2)

**Old:**

| RWAIT | Wait control of real-time clock 2 |
|---|---|
| 0 | Sets counter operation. |
| 1 | Stops SEC to YEAR counters. Mode to read or write counter value |

This bit controls the operation of the counter.
Be sure to write “1” to it to read or write the counter value.
As the internal counter (16-bit) is continuing to run, complete reading or writing within one second and turn back to
0.
When RWAIT = 1, it takes up to one cycle of fRTCuntil the counter value can be read or written (RWST = 1).
When the internal counter (16-bit) overflowed while RWAIT = 1, it keeps the event of overflow until RWAIT = 0, then counts up.
However, when it wrote a value to second count register, it will not keep the overflow event.

**New:**

| RWAIT | Wait control of real-time clock 2 |
|---|---|
| 0 | Sets counter operation. |
| 1 | Stops SEC to YEAR counters. Mode to read or write counter value |

This bit controls the operation of the counter.
Be sure to write “1” to it to read or write the counter value.
As the internal counter (16-bit) is continuing to run, complete reading or writing within one second and turn back to
0.
When RWAIT = 1, it takes up to one cycle of fRTC until the counter value can be read or written (RWST = 1). . Notes1,2
When the internal counter (16-bit) overflowed while RWAIT = 1, it keeps the event of overflow until RWAIT = 0, then counts up.
However, when it wrote a value to second count register, it will not keep the overflow event.

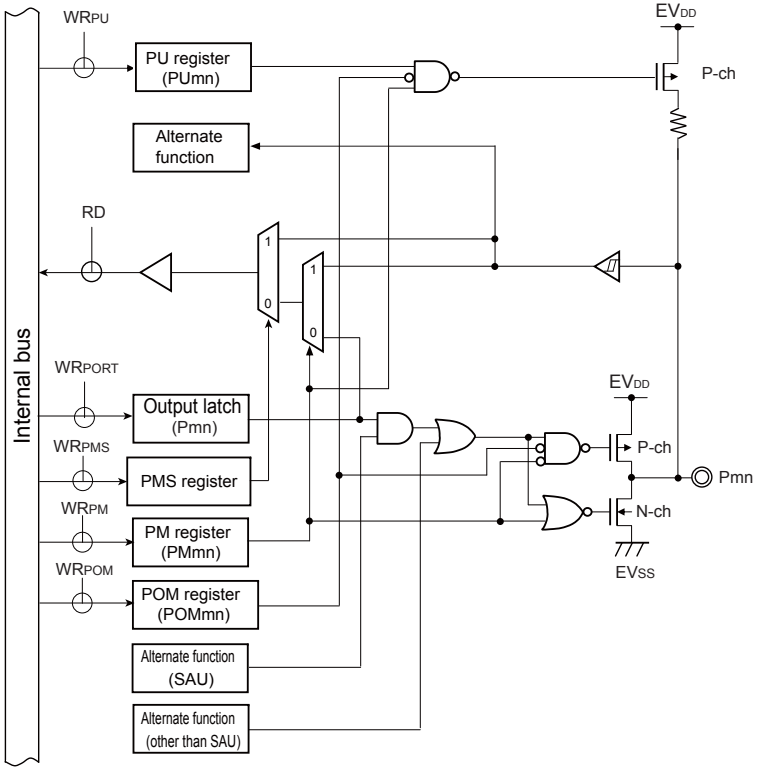
Note1. When setting RWAIT=1 during 1 operating clock ($f_{RTC}$), after setting RTCE=1, it may take two clock time of the operation clock ($f_{RTC}$), until RWST bit is set to "1".

Note2. When setting RWAIT=1 during 1 operating clock ($f_{RTC}$), after returning from a stand-by (HALT mode, STOP mode and SNOOZE mode), it may take two clock time of the operation clock ($f_{RTC}$), until RWST bit is set to "1".

## 8. 2.4 Block Diagrams of Pins Figure 2-7. Pin Block Diagram for Pin Type 7-1-4(Page 32)

**Old:**

Figure 2-7. Pin Block Diagram for Pin Type 7-1-4

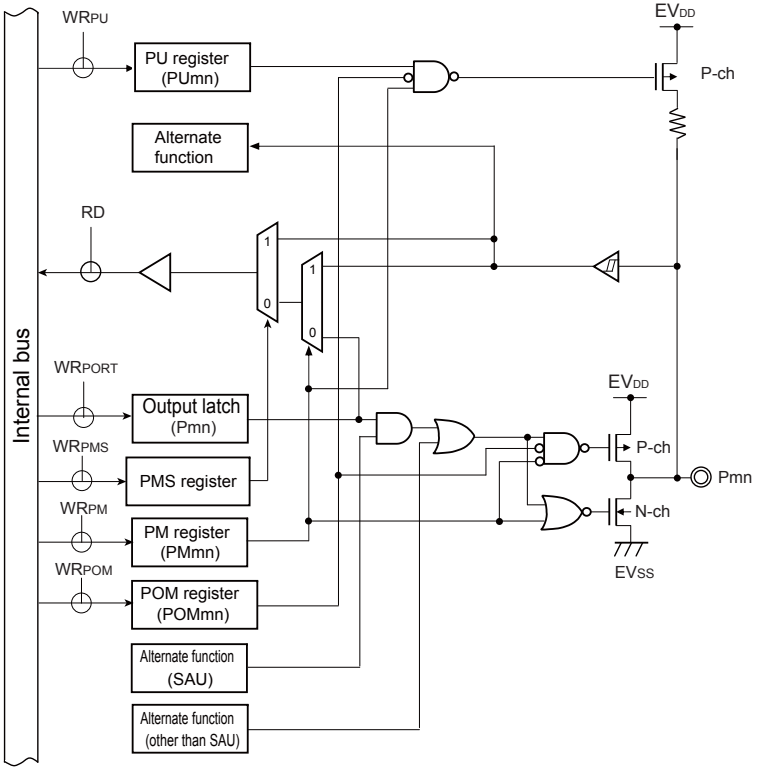



**Remarks 1.** For alternate functions, see **2.1 Port Function**.

**2.** SAU: Serial array unit

**New:**

Figure 2-7. Pin Block Diagram for Pin Type 7-1-4



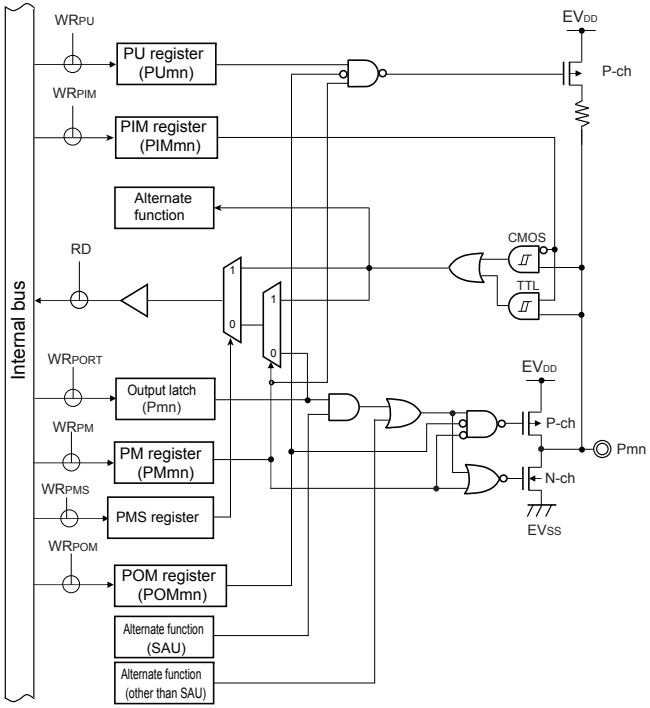

**Caution** A through current may flow through if the pin is in the intermediate potential, because the input buffer is also turned on when the pin is in N-ch open-drain output mode by port output mode register (POMx).

**Remarks 1.** For alternate functions, see **2.1 Port Function**.

**2.** SAU: Serial array unit.

**9. 2.4 Block Diagrams of Pins Figure 2-9. Pin Block Diagram for Pin Type 8-1-4(Page 34)**

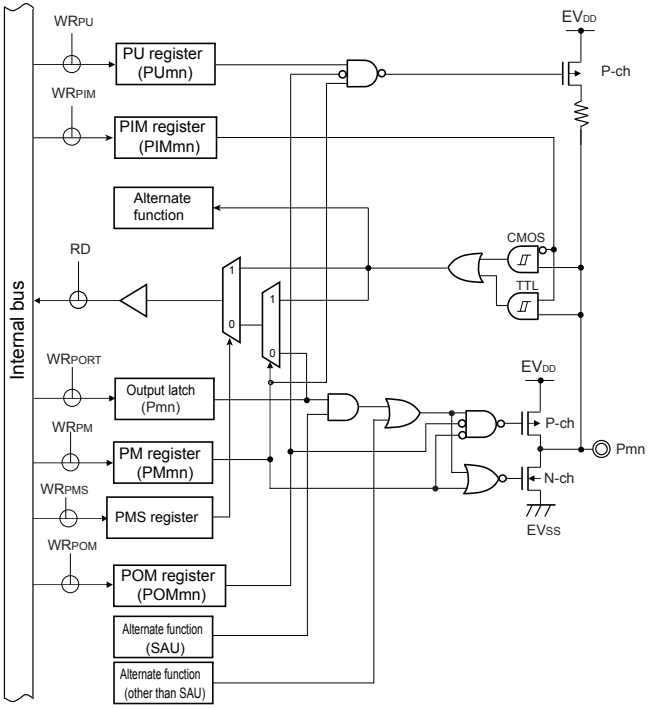
**Old:**




**Remarks 1.** For alternate functions, see **2.1 Port Function**.

**2.** SAU: Serial array unit

**New:**




**Caution 1** A through current may flow through if the pin is in the intermediate potential, because the input buffer is also turned on when the pin is in N-ch open-drain output mode by port output mode register (POMx).

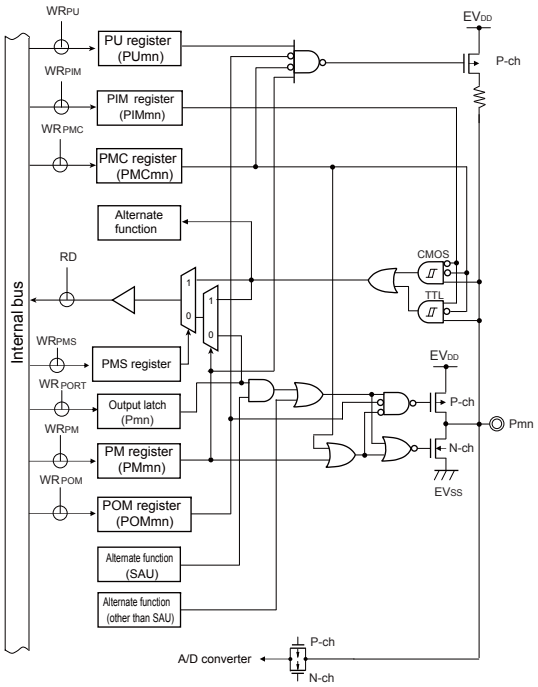
**Caution 2** Because of TTL input buffer structure, if the port input mode register (PIMx) is set in TTL input buffer, a through current may flow through in the case of high level input. It is recommended to input a low level to prevent a through current.

**Remarks 1.** For alternate functions, see **2.1 Port Function**.

**2.** SAU: Serial array unit

## 10. 2.4 Block Diagrams of Pins Figure 2-10. Pin Block Diagram for Pin Type 8-3-4(Page 35)

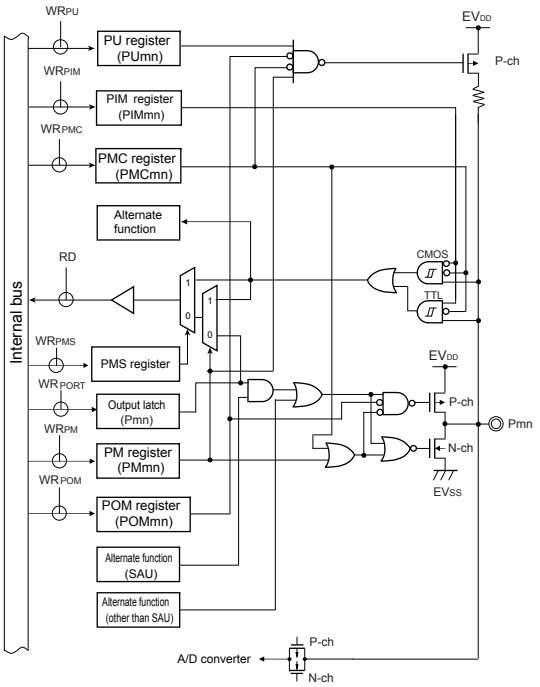
**Old:**




**Remarks 1.** For alternate functions, see **2.1 Port Function**.

**2.** SAU: Serial array unit

**New:**




**Caution 1** A through current may flow through if the pin is in the intermediate potential, because the input buffer is also turned on when the pin is in N-ch open-drain output mode by port output mode register (POMx).

**Caution 2** Because of TTL input buffer structure, if the port input mode register (PIMx) is set in TTL input buffer, a through current may flow through in the case of high level input. It is recommended to input a low level to prevent a through current.

**Remarks 1.** For alternate functions, see **2.1 Port Function**.

**2.** SAU: Serial array unit

## 11. 3.2.5 Extended special function registers (2nd SFRs: 2nd Special Function Registers) (Page 66)

### Incorrect:

**Table 3-6. Extended SFR (2nd SFR) List (5/8)**

| Address | Special Function Register (SFR) Name | Symbol | | R/W | Manipulable Bit Range | | | After Reset |
|---|---|---|---|---|---|---|---|---|
| | | | | | 1-bit | 8-bit | 16-bit | |
| (omitted) | | | | | | | | |
| F0414H | CFIFO port register | CFIFOML | CFIFOM | R/W | – | √ | √ | 00H |
| F0415H | | – | | | – | – | | 00H |
| F0418H | D0FIFO port register | D0FIFOML | D0FIFOM | R/W | – | √ | √ | 00H |
| F0419H | | – | | | – | – | | 00H |
| F041CH | D1FIFO port register | D1FIFOML | D1FIFOM | R/W | – | √ | √ | 00H |
| F041DH | | – | | | – | – | | 00H |
| F0420H | CFIFO port selection register | CFIFOSEL | | R/W | – | – | √ | 0000H |
| F0421H | | | | | | | | |
| F0422H | CFIFO port control register | CFIFOCTR | | R/W | – | – | √ | 0000H |
| F0423H | | | | | | | | |
| F0428H | D0FIFO port selection register | D0FIFOSEL | | R/W | – | – | √ | 0000H |
| F0429H | | | | | | | | |
| **F042CH** | **D0FIFO port control register** | **D0FIFOCTR** | | **R/W** | – | – | √ | **0000H** |
| **F042DH** | | | | | | | | |
| **F042EH** | **D1FIFO port selection register** | **D1FIFOSEL** | | **R/W** | – | – | √ | **0000H** |
| **F042FH** | | | | | | | | |

### Correct:

**Table 3-6. Extended SFR (2nd SFR) List (5/8)**

| Address | Special Function Register (SFR) Name | Symbol | | R/W | Manipulable Bit Range | | | After Reset |
|---|---|---|---|---|---|---|---|---|
| | | | | | 1-bit | 8-bit | 16-bit | |
| (omitted) | | | | | | | | |
| F0414H | CFIFO port register | CFIFOML | CFIFOM | R/W | – | √ | √ | 00H |
| F0415H | | – | | | – | – | | 00H |
| F0418H | D0FIFO port register | D0FIFOML | D0FIFOM | R/W | – | √ | √ | 00H |
| F0419H | | – | | | – | – | | 00H |
| F041CH | D1FIFO port register | D1FIFOML | D1FIFOM | R/W | – | √ | √ | 00H |
| F041DH | | – | | | – | – | | 00H |
| F0420H | CFIFO port selection register | CFIFOSEL | | R/W | – | – | √ | 0000H |
| F0421H | | | | | | | | |
| F0422H | CFIFO port control register | CFIFOCTR | | R/W | – | – | √ | 0000H |
| F0423H | | | | | | | | |
| F0428H | D0FIFO port selection register | D0FIFOSEL | | R/W | – | – | √ | 0000H |
| F0429H | | | | | | | | |
| F042AH | D0FIFO port control register | D0FIFOCTR | | R/W | – | – | √ | 0000H |
| F042BH | | | | | | | | |
| F042CH | D1FIFO port selection register | D1FIFOSEL | | R/W | – | – | √ | 0000H |
| F042DH | | | | | | | | |
| F042EH | D1FIFO port control register | D1FIFOCTR | | R/W | – | – | √ | 0000H |
| F042FH | | | | | | | | |