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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A099A/E	Rev.	1.00
Title	Changes to description of Complementary PWM Mode of MTU2/MTU2a/MTU3		Information Category	Technical Notification		
Applicable Product	RX62N Group, RX621 Group, RX62T Group, RX62G Group, RX630 Group, RX63T Group, RX63N Group, RX631 Group, RX210 Group, RX21A Group, RX220 Group RX111 Group	Lot No. All lots	Reference Document	User's Manual: Hardware for applicable products (see the table at the bottom)		

This document describes changes to description of Complementary PWM Mode of MTU2/MTU2a/MTU3.

Page and section numbers are based on the RX630 Group. Refer to the table on the last page for the corresponding page and section numbers in the other groups.

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The third paragraph of (j) Method for Generating PWM Output in Complementary PWM Mode is corrected as follows

Before change

The positive-phase and negative-phase signals are turned off on compare matches with the value of the counter (MTU3.TCNT), and are turned on compare matches with the MTU4.TCNT counter plus a delay of the dead time.

After change

The positive-phase and negative-phase turn-off timing is generated by a compare match with the counter indicated by a solid line, and the turn-on timing is generated by a compare match with the counter indicated by a dotted line, which operates with a delay equal to the dead time behind the counter indicated by a solid line.

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The seventh paragraph of (j) Method for Generating PWM Output in Complementary PWM Mode is corrected as follows

Before change

Similarly, in the example in Figure 22.48, compare match a' with new data in the temporary register occurs before compare match c, but until compare match c, which turns off the positive phase, other compare matches are ignored. As a result, the negative phase is not turned on.

After change

Similarly, in the example in Figure 22.48, turning off the negative phase has priority due to the occurrence of compare match a' (negative-phase off timing) before compare match d (negative-phase on timing). As a result, the negative phase is not turned on.

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Correct a ‘Figure 22.46 Example of Waveform Output in Complementary PWM Mode (1)’.

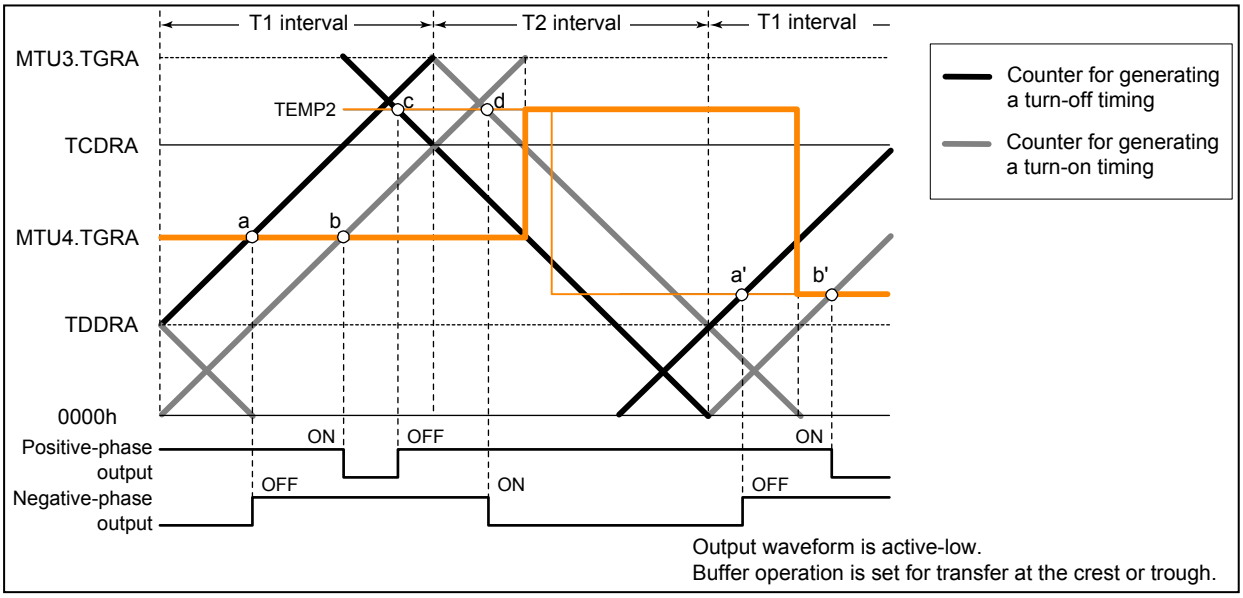

Figure 22.46 Example of Waveform Output in Complementary PWM Mode (1)

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Correct a ‘Figure 22.47 Example of Waveform Output in Complementary PWM Mode (2)’.

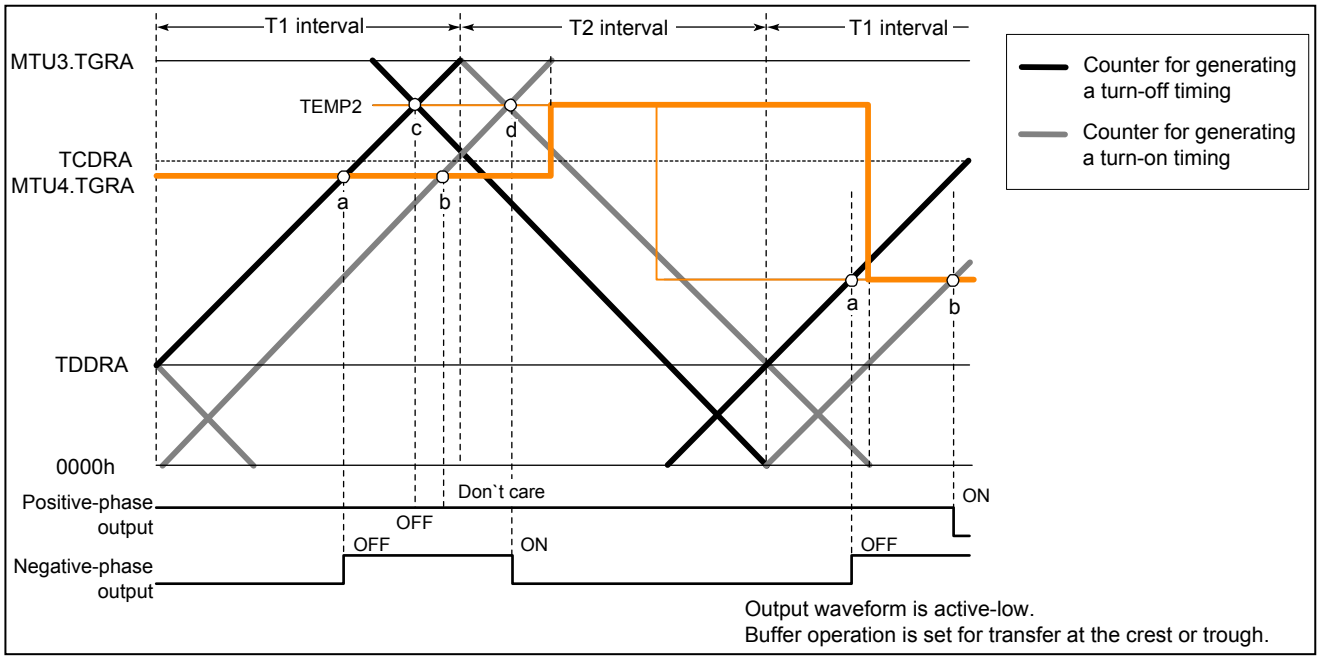

Figure 22.47 Example of Waveform Output in Complementary PWM Mode (2)

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Correct a ‘Figure 22.48 Example of Waveform Output in Complementary PWM Mode (3)’.

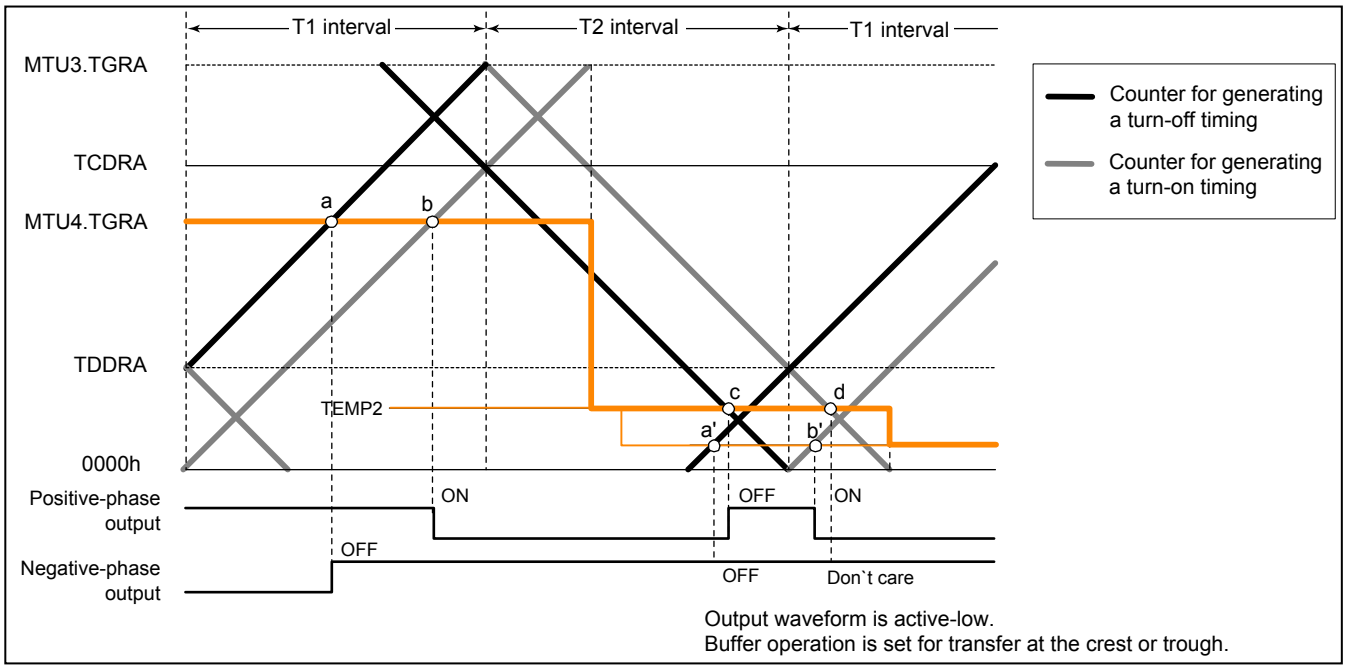

Figure 22.48 Example of Waveform Output in Complementary PWM Mode (3)

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Correct a ‘Figure 22.49 Example of 0% and 100% Waveform Output in Complementary PWM Mode (1)’.

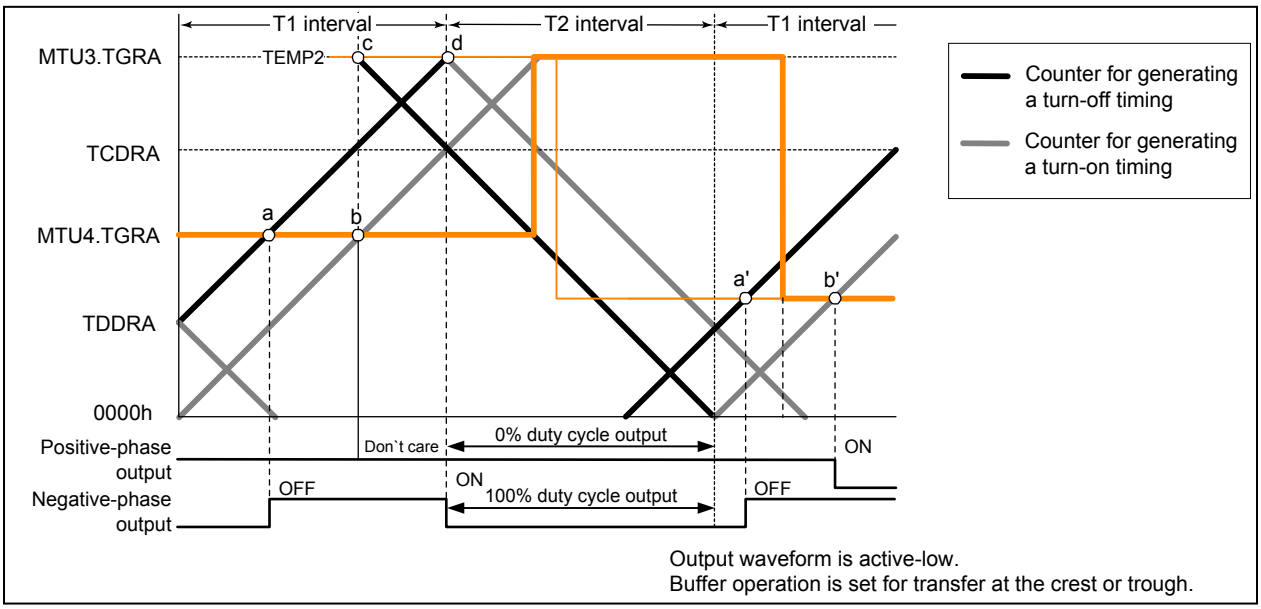

Figure 22.49 Example of 0% and 100% Waveform Output in Complementary PWM Mode (1)

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Correct a ‘Figure 22.50 Example of 0% and 100% Waveform Output in Complementary PWM Mode (2)’.

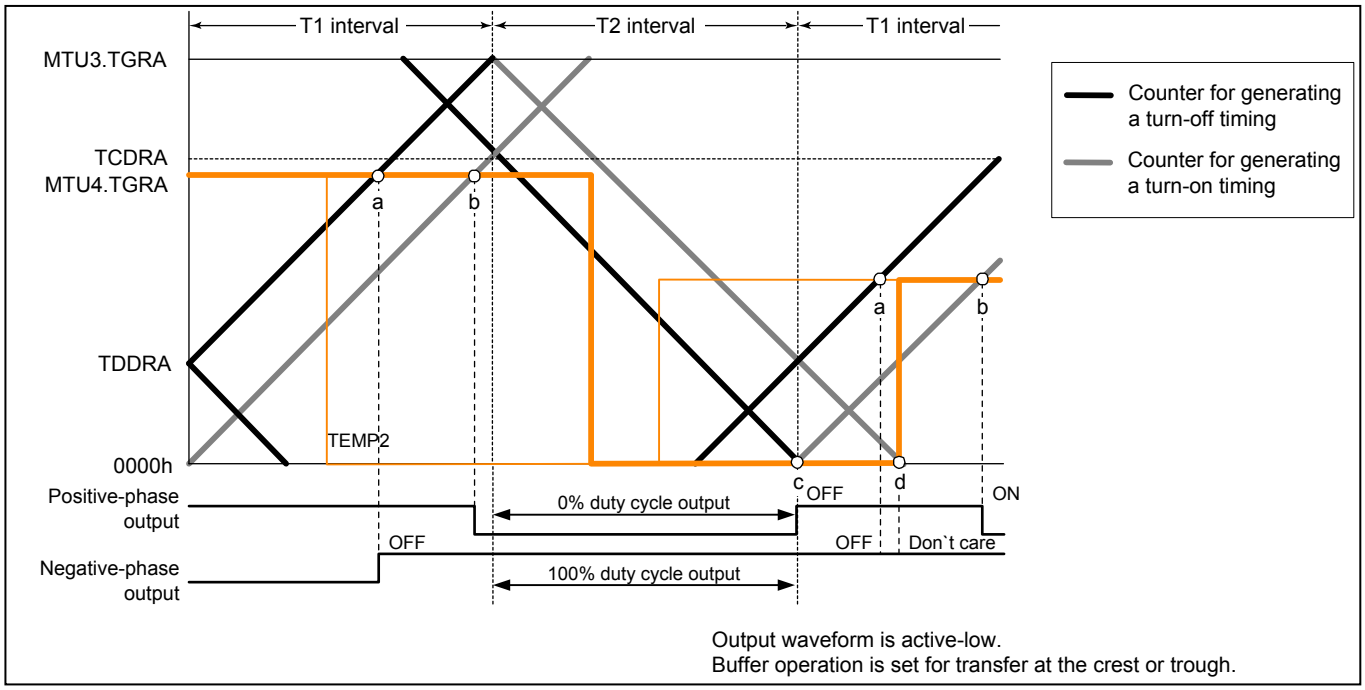

Figure 22.50 Example of 0% and 100% Waveform Output in Complementary PWM Mode (2)

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Correct a ‘Figure 22.51 Example of 0% and 100% Waveform Output in Complementary PWM Mode (3)’.

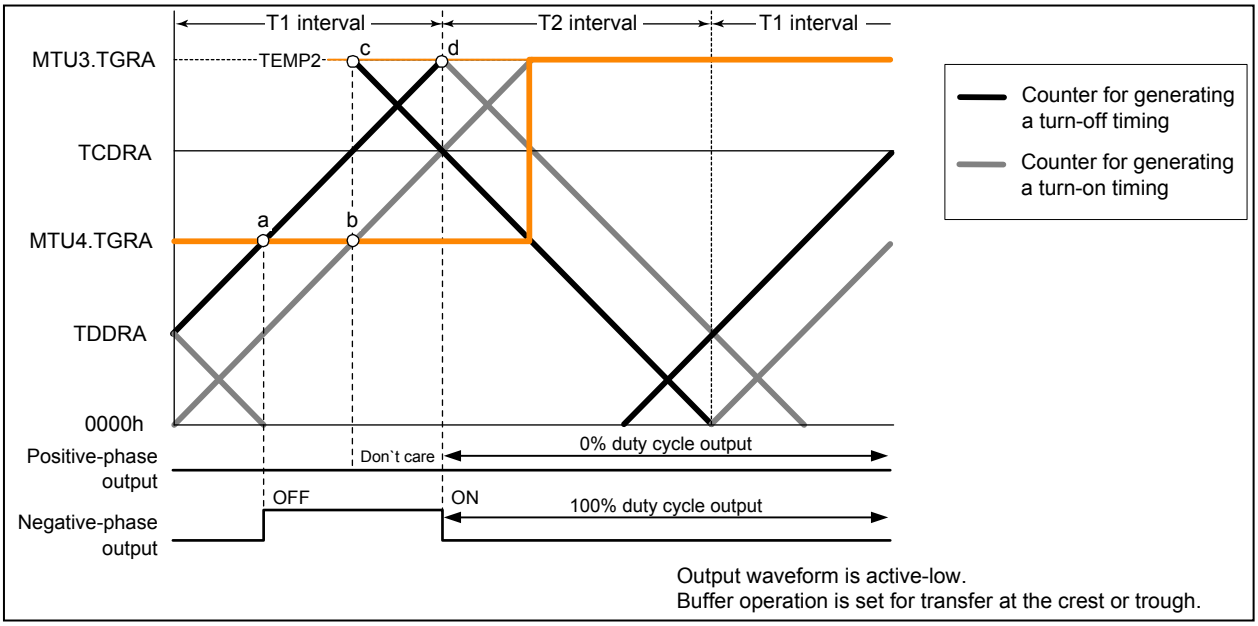

Figure 22.51 Example of 0% and 100% Waveform Output in Complementary PWM Mode (3)

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Correct a ‘Figure 22.52 Example of 0% and 100% Waveform Output in Complementary PWM Mode (4)’.

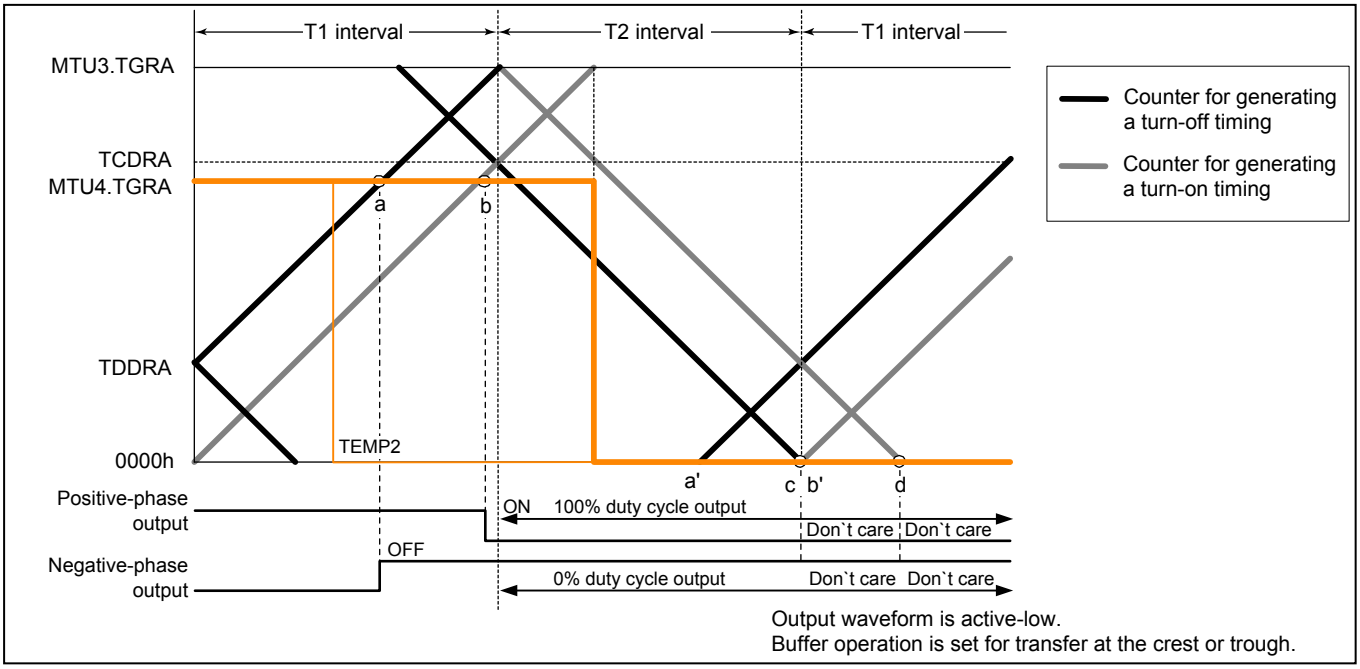

Figure 22.52 Example of 0% and 100% Waveform Output in Complementary PWM Mode (4)

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Correct a ‘Figure 22.53 Example of 0% and 100% Waveform Output in Complementary PWM Mode (5)’.

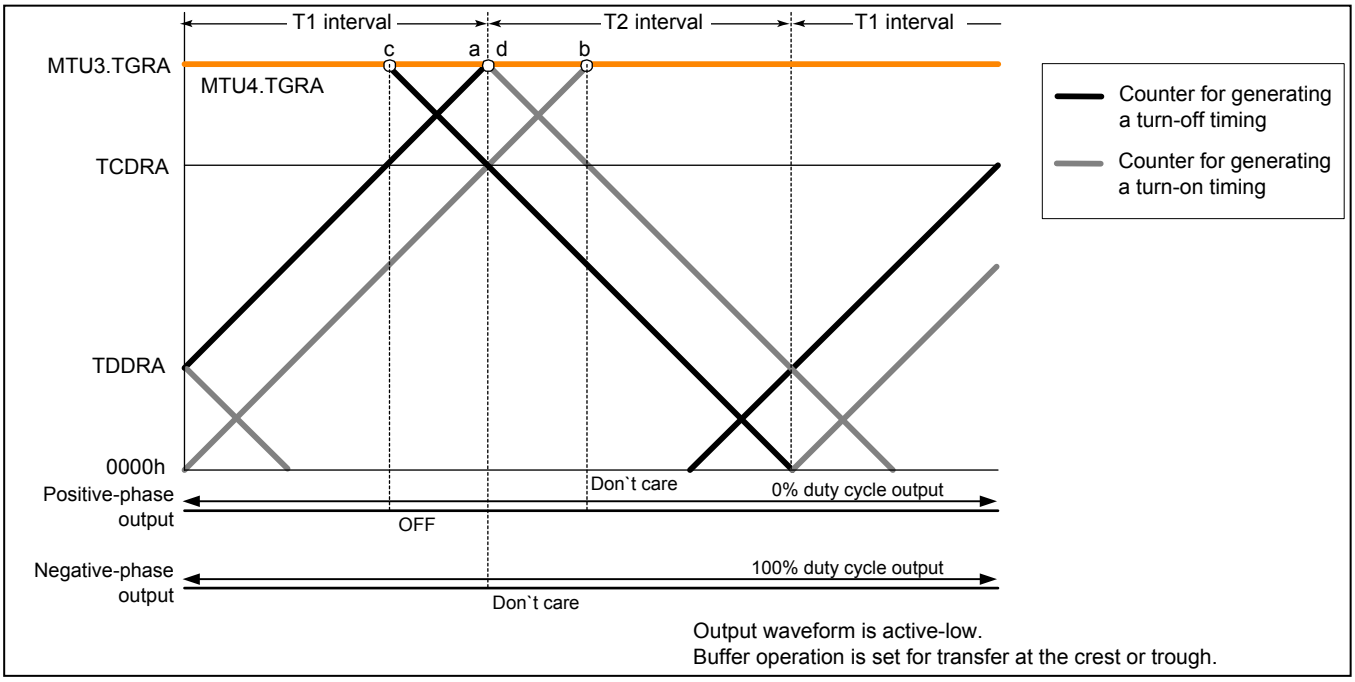

Figure 22.53 Example of 0% and 100% Waveform Output in Complementary PWM Mode (5)

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Correct a ‘Figure 22.71 Example of Operation when Buffer Transfer is Linked with Interrupt Skipping (BTE[1:0] = 10b)’.

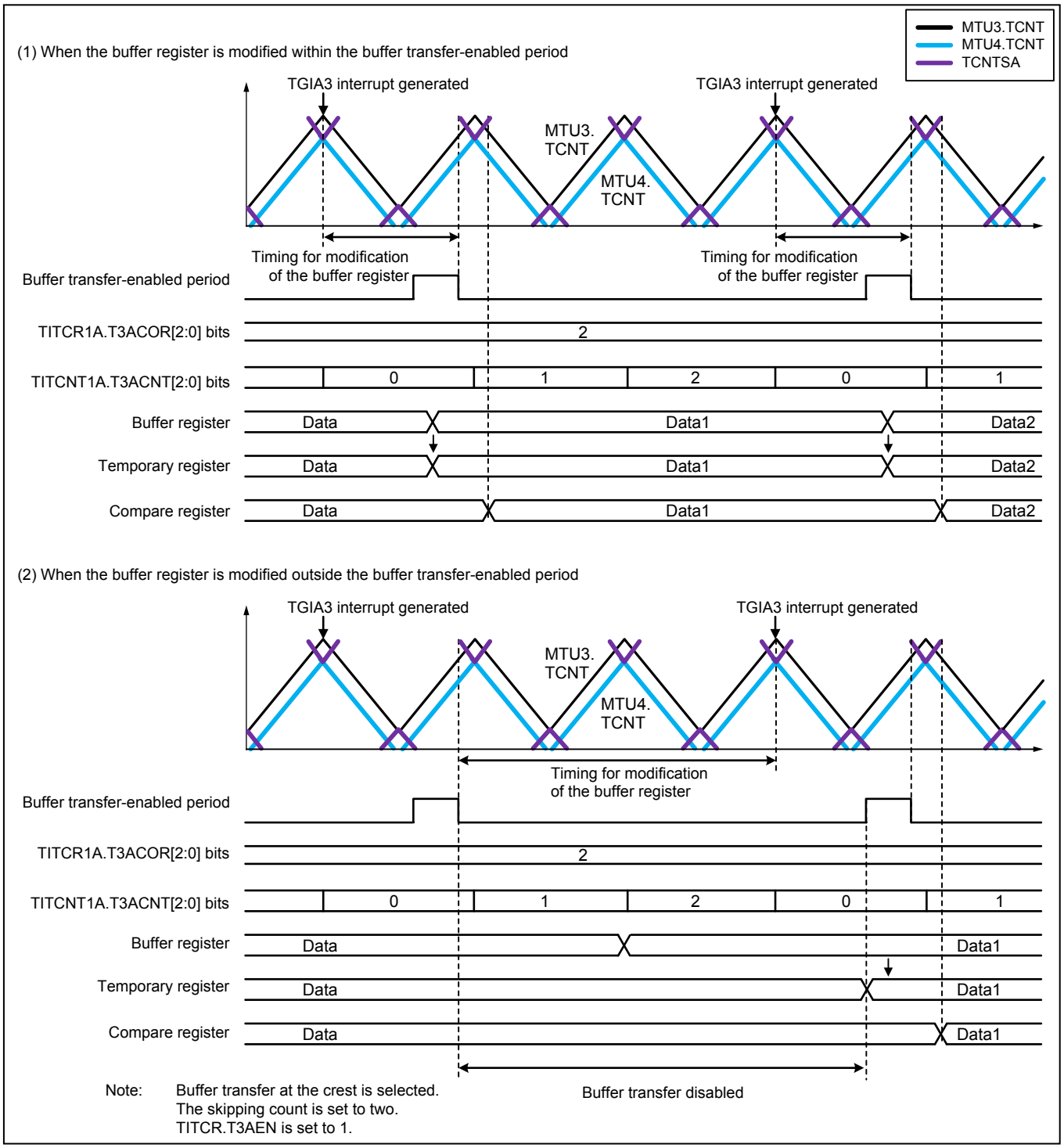

Figure 22.71 Example of Operation when Buffer Transfer is Linked with Interrupt Skipping (BTE[1:0] = 10b)

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Correct a ‘Figure 22.72 Relationship between Bits T3AEN and T4VEN in TITCR and Buffer Transfer-Enabled Period’.

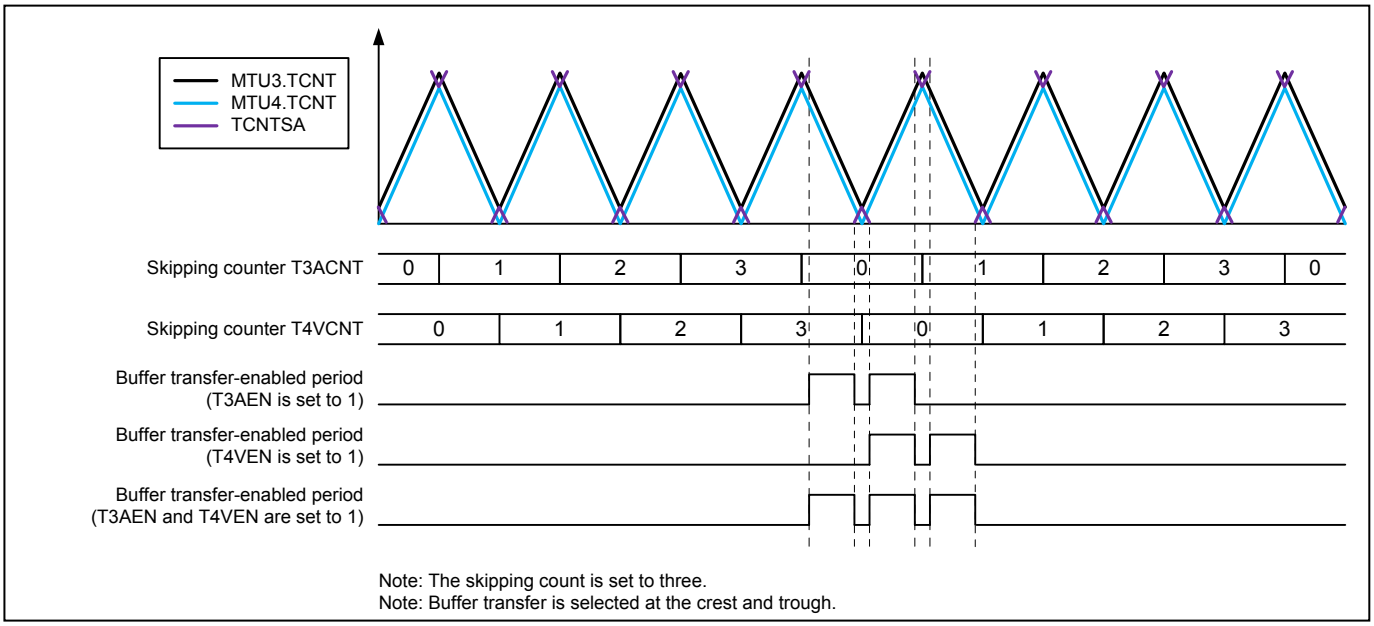

Figure 22.72 Relationship between Bits T3AEN and T4VEN in TITCR and Buffer Transfer-Enabled Period

■Target products and Reference

Series	Group	Title	Rev.	Document No.
RX600	RX62N, RX621	RX62N group, RX621 group User’s Manual, Hardware	1.30	R01UH0033EJ0130
	RX62T, RX62G	RX62T group, RX62G group User’s Manual, Hardware	2.00	R01UH0034EJ0200
	RX630	RX630 group User’s Manual, Hardware	1.60	R01UH0040EJ0160
	RX63N, RX631	RX63N group, RX631 group User’s Manual, Hardware	1.80	R01UH0041EJ0180
	RX63T	RX63T group User’s Manual, Hardware	2.10	R01UH0238EJ0210
RX200	RX210	RX210 group User’s Manual, Hardware	1.50	R01UH0037EJ0150
	RX21A	RX21A group User’s Manual, Hardware	1.00	R01UH0251EJ0100
	RX220	RX220 group User’s Manual, Hardware	1.10	R01UH0292EJ0110
RX100	RX111	RX111 group User’s Manual, Hardware	1.10	R01UH0365EJ0110

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RX600	RX62N, RX621	The third paragraph of (j) Method for Generating PWM Output in Complementary PWM Mode	Not applicable
		The seventh paragraph of (j) Method for Generating PWM Output in Complementary PWM Mode	Page 979 of 2020
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		Figure 18.48 Example of Waveform Output in Complementary PWM Mode (2) (Unit 0)	Page 980 of 2020

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		Figure 18.53 Example of 0% and 100% Waveform Output in Complementary PWM Mode (4) (Unit 0)	Page 983 of 2020
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		Figure 18.73 Relationship between Bits T3AEN and T4VEN in TITCR and Buffer Transfer-Enabled Period (Unit 0)	Page 999 of 2020
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		Figure 16.54 Example of 0% and 100% Waveform Output in Complementary PWM Mode (MTU3 and MTU4) (5)	Page 668 of 1489
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		Figure 16.82 Relationship between Bits T3AEN and T4VEN in TITCR and Buffer Transfer-Enabled Period	Page 625 of 1489
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	RX63T	The third paragraph of (j) Method for Generating PWM Output in Complementary PWM Mode	Page 683 of 1851
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		Figure 22.81 Example of Operation when Buffer Transfer is Linked with Interrupt Skipping (BTE[1:0] = 10b)	Page 706 of 1851
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