Date: Aug. 8, 2017

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RL*-A083A/E	Rev.	1.00
Title	Addition of the unused internal pin setting to User's manual		Information Category	Technical Notification		
Applicable Product	R5F11AGGANB, R5F11AGGDNB, R5F11AGHANB, R5F11AGHDNB, R5F11AGJANB, R5F11AGJDNB, RY7011A0000DZ00	Lot No. ALL	Reference Document	RL78/G1D User's Manual: Hardware Rev.1.20 R01UH0515EJ0120 (Dec, 2016)		

By treating the unused internal pins added in this technical notification, it is possible to reduce the leakage current about 100uA (It converges almost 0uA in about 1 second.). It is equivalent to the maximum 13.9 nAh@3V in the current time product.

The following unused internal pins explanations are added to RL78/G1D User's Manual: Hardware.

P24-P27, P44-P47, P56, P57, P64-P67, P80-P87, P100-P102, P110, P111, P142-P145, P150-P156

The hardware user's manual for above applicable products will be revised accordingly.

Previous revision: Bold with underline; After revision: Gray hatched

1. Append to 2.3 Initial Settings of Unused Internal Pins of MCU

Previous revision

P04, P17, P31, P41 to P43, P50 to P55, P62, P63, P73, P141, P146

After revision

P04, P17, P24-P27, P31, P41-P47, P50-P57, P62- P67, P73, P80-P87, P100-P102, P110, P111, P141-P146, P150-P156

2. Append to Table 5-1 in 5.2 Port Configuration.

Previous revision

able 5-1. Port Configuration

Item	Configuration
Control registers	Port mode registers (PM0 to **PM7, PM12, PM14**) Port registers (P0 to **P7, P12 to P14**) Pull-up resistor option registers (PU0, PU1, PU3, PU4, PU12, PU14) Port input mode registers (PIM0, PIM1) Port output mode registers (POM0, POM1) Port mode control registers (PMC0, PMC12, and PMC14) A/D port configuration register (ADPC) Peripheral I/O redirection register (PIOR) Global digital input disable register (GDIDIS)
Port	Total: 32 (CMOS I/O: 26, CMOS input: 5, CMOS output: 1)
Pull-up resistor	Total: 16

After revision

able 5-1. Port Configuration

Item	Configuration
Control registers	Port mode registers (PM0 to PM8, PM10 to PM12, PM14, PM15) Port registers (P0 to P8, P10 to P15) Pull-up resistor option registers (PU0, PU1, PU3, PU4, PU12, PU14) Port input mode registers (PIM0, PIM1) Port output mode registers (POM0, POM1) Port mode control registers (PMC0, PMC12, and PMC14) A/D port configuration register (ADPC) Peripheral I/O redirection register (PIOR) Global digital input disable register (GDIDIS)
Port	Total: 32 (CMOS I/O: 26, CMOS input: 5, CMOS output: 1)
Pull-up resistor	Total: 16

3. Append to Table 5-3. in 5.3 Registers Controlling Port Function

Previous revision

Table 5-3. PMxx, Pxx, PUxx, PIMxx, POMxx, PMCxx registers and the bits (1/2)

Port		Bit name					
		PMxx register	Pxx register	PUxx register	PIMxx register	POMxx register	PMCxx register
Port 0	0	PM00	P00	PU00	–	POM00	–
	1	PM01	P01	PU01	PIM01	–	–
	2	PM02	P02	PU02	–	POM02	PMC02
	3	PM03	P03	PU03	PIM03	POM03	PMC03
	4	PM04Note	P04Note	–	–	–	–
	5	PM05Note	P05Note	–	–	–	–
	6	PM06Note	P06Note	–	–	–	–
Port 1	0	PM10	P10	PU10	PIM10	POM10	–
	1	PM11	P11	PU11	PIM11	POM11	–
	2	PM12	P12	PU12	–	POM12	–
	3	PM13	P13	PU13	PIM13	POM13	–
	4	PM14	P14	PU14	PIM14	POM14	–
	5	PM15	P15	PU15	PIM15	POM15	–
	6	PM16	P16	PU16	PIM16	–	–
	7	PM17Note	P17Note	–	–	–	–
Port 2	0	PM20	P20	–	–	–	–
	1	PM21	P21	–	–	–	–
	2	PM22	P22	–	–	–	–
	3	PM23	P23	–	–	–	–
Port 3	0	PM30	P30	PU30	–	–	–
	1	PM31Note	P31Note	–	–	–	–
Port 4	0	PM40	P40	PU40	–	–	–
	1	PM41Note	P41Note	–	–	–	–
	2	PM42Note	P42Note	–	–	–	–
	3	PM43Note	P43Note	–	–	–	–
Port 5	0	PM50Note	P50Note	–	–	–	–
	1	PM51Note	P51Note	–	–	–	–
	2	PM52Note	P52Note	–	–	–	–
	3	PM53Note	P53Note	–	–	–	–
	4	PM54Note	P54Note	–	–	–	–
	5	PM55Note	P55Note	–	–	–	–
Port 6	0	PM60	P60	–	–	–	–
	1	PM61	P61	–	–	–	–
	2	PM62Note	P62Note	–	–	–	–
	3	PM63Note	P63Note	–	–	–	–

Table 5-3. PMxx, Pxx, PUxx, PIMxx, POMxx, PMCxx registers and the bits (2/2)

Port		Bit name					
		PMxx register	Pxx register	PUxx register	PIMxx register	POMxx register	PMCxx register
Port 7	0	PM70[Note]	P70[Note]	–	–	–	–
	1	PM71[Note]	P71[Note]	–	–	–	–
	2	PM72[Note]	P72[Note]	–	–	–	–
	3	PM73[Note]	P73[Note]	–	–	–	–
	4	PM74[Note]	P74[Note]	–	–	–	–
	5	PM75[Note]	P75[Note]	–	–	–	–
	6	PM76[Note]	P76[Note]	–	–	–	–
	7	PM77[Note]	P77[Note]	–	–	–	–
Port 12	0	PM120	P120	PU120	–	–	PMC120
	1	–	P121	–	–	–	–
	2	–	P122	–	–	–	–
	3	–	P123	–	–	–	–
	4	–	P124	–	–	–	–
Port 13	0	–	P130	–	–	–	–
	7	–	P137	–	–	–	–
Port 14	0	PM140	P140	PU140	–	–	–
	1	PM141[Note]	P141[Note]	–	–	–	–
	6	PM146[Note]	P146[Note]	–	–	–	–
	7	PM147	P147	PU147	–	–	–

After revision

Table 5-3. PMxx, Pxx, PUxx, PIMxx, POMxx, PMCxx registers and the bits (1/2)

Port		Bit name					
		PMxx register	Pxx register	PUxx register	PIMxx register	POMxx register	PMCxx register
Port 0	0	PM00	P00	PU00	–	POM00	–
	1	PM01	P01	PU01	PIM01	–	–
	2	PM02	P02	PU02	–	POM02	PMC02
	3	PM03	P03	PU03	PIM03	POM03	PMC03
	4	PM04Note	P04Note	–	–	–	–
	5	PM05Note	P05Note	–	–	–	–
	6	PM06Note	P06Note	–	–	–	–
Port 1	0	PM10	P10	PU10	PIM10	POM10	–
	1	PM11	P11	PU11	PIM11	POM11	–
	2	PM12	P12	PU12	–	POM12	–
	3	PM13	P13	PU13	PIM13	POM13	–
	4	PM14	P14	PU14	PIM14	POM14	–
	5	PM15	P15	PU15	PIM15	POM15	–
	6	PM16	P16	PU16	PIM16	–	–
	7	PM17Note	P17Note	–	–	–	–
Port 2	0	PM20	P20	–	–	–	–
	1	PM21	P21	–	–	–	–
	2	PM22	P22	–	–	–	–
	3	PM23	P23	–	–	–	–
	4	PM24Note	P24Note	–	–	–	–
	5	PM25Note	P25Note	–	–	–	–
	6	PM26Note	P26Note	–	–	–	–
	7	PM27Note	P27Note	–	–	–	–
Port 3	0	PM30	P30	PU30	–	–	–
	1	PM31Note	P31Note	–	–	–	–
Port 4	0	PM40	P40	PU40	–	–	–
	1	PM41Note	P41Note	–	–	–	–
	2	PM42Note	P42Note	–	–	–	–
	3	PM43Note	P43Note	–	–	–	–
	4	PM44Note	P44Note	–	–	–	–
	5	PM45Note	P45Note	–	–	–	–
	6	PM46Note	P46Note	–	–	–	–
	7	PM47Note	P47Note	–	–	–	–
Port 5	0	PM50Note	P50Note	–	–	–	–
	1	PM51Note	P51Note	–	–	–	–
	2	PM52Note	P52Note	–	–	–	–
	3	PM53Note	P53Note	–	–	–	–
	4	PM54Note	P54Note	–	–	–	–
	5	PM55Note	P55Note	–	–	–	–
	6	PM56Note	P56Note	–	–	–	–
	7	PM57Note	P57Note	–	–	–	–

Port		Bit name					
		PMxx register	Pxx register	PUxx register	PIMxx register	POMxx register	PMCxx register
Port 6	0	PM60	P60	–	–	–	–
	1	PM61	P61	–	–	–	–
	2	PM62Note	P62Note	–	–	–	–
	3	PM63Note	P63Note	–	–	–	–
	4	PM64Note	P64Note	–	–	–	–
	5	PM65Note	P65Note	–	–	–	–
	6	PM66Note	P66Note	–	–	–	–
	7	PM67Note	P67Note	–	–	–	–

Table 5-3. PMxx, Pxx, PUxx, PIMxx, POMxx, PMCxx registers and the bits (2/2)

Port		Bit name					
		PMxx register	Pxx register	PUxx register	PIMxx register	POMxx register	PMCxx register
Port 7	0	PM70Note	P70Note	–	–	–	–
	1	PM71Note	P71Note	–	–	–	–
	2	PM72Note	P72Note	–	–	–	–
	3	PM73Note	P73Note	–	–	–	–
	4	PM74Note	P74Note	–	–	–	–
	5	PM75Note	P75Note	–	–	–	–
	6	PM76Note	P76Note	–	–	–	–
	7	PM77Note	P77Note	–	–	–	–
Port 8	0	PM80Note	P80Note	–	–	–	–
	1	PM81Note	P81Note	–	–	–	–
	2	PM82Note	P82Note	–	–	–	–
	3	PM83Note	P83Note	–	–	–	–
	4	PM84Note	P84Note	–	–	–	–
	5	PM85Note	P85Note	–	–	–	–
	6	PM86Note	P86Note	–	–	–	–
	7	PM87Note	P87Note	–	–	–	–
Port 10	0	PM100Note	P100Note	–	–	–	–
	1	PM101Note	P101Note	–	–	–	–
	2	PM102Note	P102Note	–	–	–	–
Port 11	0	PM110Note	P110Note	–	–	–	–
	1	PM111Note	P111Note	–	–	–	–
Port 12	0	PM120	P120	PU120	–	–	PMC120
	1	–	P121	–	–	–	–
	2	–	P122	–	–	–	–
	3	–	P123	–	–	–	–
	4	–	P124	–	–	–	–
Port 13	0	–	P130	–	–	–	–
	7	–	P137	–	–	–	–

Port		Bit name					
		PMxx register	Pxx register	PUxx register	PIMxx register	POMxx register	PMCxx register
Port 14	0	PM140	P140	PU140	–	–	–
	1	PM141Note	P141Note	–	–	–	–
	2	PM142Note	P142Note	–	–	–	–
	3	PM143Note	P143Note	–	–	–	–
	4	PM144Note	P144Note	–	–	–	–
	5	PM145Note	P145Note	–	–	–	–
	6	PM146Note	P146Note	–	–	–	–
	7	PM147	P147	PU147	–	–	–
Port 15	0	PM150Note	P150Note	–	–	–	–
	1	PM151Note	P151Note	–	–	–	–
	2	PM152Note	P152Note	–	–	–	–
	3	PM153Note	P153Note	–	–	–	–
	4	PM154Note	P154Note	–	–	–	–
	5	PM155Note	P155Note	–	–	–	–
	6	PM156Note	P156Note	–	–	–	–
	7	PM157Note	P157Note	–	–	–	–

Note For controlling internal pins. For details, see CHAPTER 2.

4. Append to Figure 5-1. In 5.3.1 Port mode registers (PMxx)

Previous revision

Address: FFF22H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM2	1	1	1	1	PM23	PM22	PM21	PM20

Address: FFF24H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM4	1	1	1	1	PM43Note 2	PM42Note 2	PM41Note 2	PM40

Address: FFF25H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM5	1	1	PM55Note 2	PM54Note 2	PM53Note 2	PM52Note 2	PM51Note 2	PM50Note 2

Address: FFF26H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM6	1	1	1	1	PM63Note 2	PM62Note 2	PM61	PM60

Address: FFF2EH After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM14	PM147	PM146Note 2	1	1	1	1	PM141Note 2	PM140

After revision

Address: FFF22H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM2	PM27Note 5	PM26Note 5	PM25Note 5	PM24Note 5	PM23	PM22	PM21	PM20

Address: FFF24H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM4	PM47Note 2	PM46Note 2	PM45Note 2	PM44Note 2	PM43Note 2	PM42Note 2	PM41Note 2	PM40

Address: FFF25H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM5	PM57Note 2	PM56Note 2	PM55Note 2	PM54Note 2	PM53Note 2	PM52Note 2	PM51Note 2	PM50Note 2

Address: FFF26H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM6	PM67Note 2	PM66Note 2	PM65Note 2	PM64Note 2	PM63Note 2	PM62Note 2	PM61	PM60

Address: FFF28H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM8	PM87Note 2	PM86Note 2	PM85Note 2	PM84Note 2	PM83Note 2	PM82Note 2	PM81Note 2	PM80Note 2

Address: FFF2AH After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM10	1	1	1	1	1	PM102Note 2	PM101Note 2	PM100Note 2

Address: FFF2BH After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM11	1	1	1	1	1	1	PM111Note 2	PM110Note 2

Address: FFF2EH After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM14	PM147	PM146Note 2	PM145Note 2	PM144Note 2	PM143Note 2	PM142Note 2	PM141Note 2	PM140

Address: FFF2FH After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM15	1	PM156Note5	PM155Note5	PM154Note5	PM153Note5	PM152Note5	PM151Note5	PM150Note5

Notes 2. These internal pins must be set to output mode after reset release by software by setting 0 to the port register and port mode register.

5. In case of to set ADPC other than the reset value (00H), it must be to set to output mode by setting 0 to the port register and port mode register by software.

5. Append to Figure 5-2. in 5.3.2 Port registers (Pxx)

Previous revision

P2	0	0	0	0	P23	P22	P21	P20	FFF02H	00H (output latch)	R/W
P4	0	0	0	0	P43Note 3	P42Note 3	P41Note 3	P40	FFF04H	00H (output latch)	R/W
P5	0	0	P55Note 3	P54Note 3	P53Note 3	P52Note 3	P51Note 3	P50Note 3	FFF05H	00H (output latch)	R/W
P6	0	0	0	0	P63Note 3	P62Note 3	0	0	FFF06H	00H (output latch)	R/W
P14	P147	P146Note 3	0	0	0	0	P141Note 3	P140	FFF0EH	00H (output latch)	R/W

After revision

P2	P27Note5	P26Note5	P25Note5	P24Note5	P23	P22	P21	P20	FFF02H	00H (output latch)	R/W
P4	P47Note 3	P46Note 3	P45Note 3	P44Note 3	P43Note 3	P42Note 3	P41Note 3	P40	FFF04H	00H (output latch)	R/W
P5	P57Note 3	P56Note 3	P55Note 3	P54Note 3	P53Note 3	P52Note 3	P51Note 3	P50Note 3	FFF05H	00H (output latch)	R/W
P6	P67Note 3	P66Note 3	P65Note 3	P64Note 3	P63Note 3	P62Note 3	P61	P60	FFF06H	00H (output latch)	R/W
P8	P87Note 3	P86Note 3	P85Note 3	P84Note 3	P83Note 3	P82Note 3	P81Note 3	P80Note 3	FFF08H	00H (output latch)	R/W
P10	0	0	0	0	0	P102Note 3	P101Note 3	P100Note 3	FFF0AH	00H (output latch)	R/W
P11	0	0	0	0	0	0	P111Note 3	P110Note 3	FFF0BH	00H (output latch)	R/W
P14	P147	P146Note 3	P145Note 3	P144Note 3	P143Note 3	P142Note 3	P141Note 3	P140	FFF0EH	00H (output latch)	R/W
P15	0	P156Note5	P155Note5	P154Note5	P153Note5	P152Note5	P151Note5	P150Note5	FFF0FH	00H (output latch)	R/W

Notes 3. These internal pins must be set to output mode after reset release by software by setting 0 to the port register and port mode register.

5. In case of to set ADPC other than the reset value (00H), it must be to set to output mode by setting 0 to the port register and port mode register by software.

6. Correction to Figure 5-7. in 5.3.7 A/D port configuration register (ADPC)

Previous revision

Address: F0076H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC	0	0	0	0	ADPC3	ADPC2	ADPC1	ADPC0

ADPC3	ADPC2	ADPC1	ADPC0	Analog input (A)/digital I/O (D) switching			
				ANI3/P23	ANI2/P22	ANI1/P21	ANI0/P20
0	0	0	0	A	A	A	A
0	0	0	1	D	D	D	D
0	0	1	0	D	D	D	A
0	0	1	1	D	D	A	A
0	1	0	0	D	A	A	A
0	1	1	0	A	A	A	A
0	1	1	1	A	A	A	A
1	0	0	0	A	A	A	A
1	0	0	1	A	A	A	A
1	0	1	0	A	A	A	A
1	0	1	1	A	A	A	A
1	1	0	0	A	A	A	A
1	1	0	1	A	A	A	A
1	1	1	0	A	A	A	A
1	1	1	1	A	A	A	A
Other than above				Setting prohibited			

After revision

Address: F0076H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC	0	0	0	0	ADPC3	ADPC2	ADPC1	ADPC0

ADPC3	ADPC2	ADPC1	ADPC0	Analog input (A)/digital I/O (D) switching			
				ANI3/P23	ANI2/P22	ANI1/P21	ANI0/P20
0	0	0	0	A	A	A	A
0	0	0	1	D	D	D	D
0	0	1	0	D	D	D	A
0	0	1	1	D	D	A	A
0	1	0	0	D	A	A	A
0	1	1	0	A	A	A	A
0	1	1	1	A	A	A	A
Other than above				Setting prohibited			

Appendix: About software processing of additional unused internal pins

The additional unused internal pins need to set for output mode by the port mode register.

In that case, note that the target port mode register differs when A/D port configuration register (ADPC) is used with reset value (00H) or when it is used otherwise. (Refer to **Note 5** in the above number 4.)

How to set the unused internal pins is as follows.

Add the setting shown in [Example of software processing code] to the following source code of Bluetooth Low Energy protocol stack Ver 1.20 or earlier and RL78/G1D beacon stack Ver 2.10 or earlier.

For Bluetooth Low Energy protocol stack:

Add to the end of plf_port_init function defined in the following file.

RL78_G1D/Project_Source/renesas/src/driver/plf/plf.c

For RL78/G1D beacon stack:

Add to the end of plf_init_port function defined in the following file.

RL78G1D_Beacon/Project_Source/application/src/driver/plf/plf.c

[Example of software processing code]

The code examples are shown when ADPC is used with the reset value (00H) or when it is used otherwise.

Incidentally, in the sample program attached to the Bluetooth Low Energy protocol stack and RL78/G1D beacon stack, ADPC is set to 01H. Therefore, if ADPC is not set by user program, add the software processing example which is shown as “Wen ADPC is not used with reset value” to the following part.

When ADPC is used with reset value

```
#define clear_sfr(sfr, mask)   (sfr &= (unsigned char)(mask))   /* SFR bit clear macro */
#if !defined(PM8)
#define PM8        (*(volatile __near unsigned char  *)0xFF28)
#endif
#if !defined(PM10)
#define PM10       (*(volatile __near unsigned char  *)0xFF2A)
#endif
#if !defined(PM11)
#define PM11       (*(volatile __near unsigned char  *)0xFF2B)
#endif
#if !defined(PM15)
#define PM15       (*(volatile __near unsigned char  *)0xFF2F)
#endif
clear_sfr(PM4, 0x0F);      /* clear PM44-PM47 */
clear_sfr(PM5, 0x3F);      /* clear PM56,PM57 */
clear_sfr(PM6, 0x0F);      /* clear PM64-PM67 */
clear_sfr(PM8, 0x00);      /* clear PM80-PM87 */
clear_sfr(PM10, 0xF8);     /* clear PM100-PM102 */
clear_sfr(PM11, 0xFC);     /* clear PM110,PM111 */
clear_sfr(PM14, 0xC3);     /* clear PM142-PM145 */
```

When ADPC is not used with reset value

```
#define clear_sfr(sfr, mask)   (sfr &= (unsigned char)(mask))   /* SFR bit clear macro */
#if !defined(PM8)
#define PM8        (*(volatile __near unsigned char  *)0xFF28)
#endif
#if !defined(PM10)
#define PM10       (*(volatile __near unsigned char  *)0xFF2A)
#endif
#if !defined(PM11)
#define PM11       (*(volatile __near unsigned char  *)0xFF2B)
#endif
#if !defined(PM15)
#define PM15       (*(volatile __near unsigned char  *)0xFF2F)
#endif
clear_sfr(PM4, 0x0F);       /* clear PM44-PM47 */
clear_sfr(PM5, 0x3F);       /* clear PM56,PM57 */
clear_sfr(PM6, 0x0F);       /* clear PM64-PM67 */
clear_sfr(PM8, 0x00);       /* clear PM80-PM87 */
clear_sfr(PM10, 0xF8);      /* clear PM100-PM102 */
clear_sfr(PM11, 0xFC);      /* clear PM110,PM111 */
clear_sfr(PM14, 0xC3);      /* clear PM142-PM145 */
clear_sfr(PM2, 0x0F);       /* clear PM24-PM27 */
clear_sfr(PM15, 0x80);      /* clear PM150-PM156 */
```