Rev.12.00
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R0E521000EPB00 Release Notes - Read this before using this product -

Renesas Solutions Corp.

Thank you for purchasing the R0E521000EPB00 emulation probe for the Renesas PC7501. This document contains the information necessary for using this product. Be sure to read this before using the product.

Introduction

The R0E521000EPB00 is an emulation probe for the R8C Family of Renesas 16-bit MCUs.

- Emulation probe: R0E521000EPB00
  This is an emulation probe (board) for the R8C Family used by connecting to the PC7501 emulator main unit.

Setup Guide

	For details, refer to...
1. Check the contents	>> “Package Components” (right)
▼	
2. Register your R0E521000EPB00	>> R0E521000EPB00 User’s Manual “User Registration”
▼	
3. Setup hardware and turn on the emulator	>> R0E521000EPB00 User’s Manual “Chapter 2. Setup”
▼	
4. Startup the High-performance Embedded Workshop and the emulator debugger.	>> R0E521000EPB00 User’s Manual “Chapter 3. Usage”

Applicable MCU Groups

The R0E521000EPB00 is available for the R8C Family MCUs by using with the following converter boards.

Converter board	Applicable MCU Groups
R0E521134CFG00	: R8C/10, R8C/11, R8C/12, R8C/13
R0E521174CSJ00	: R8C/14, R8C/15, R8C/16, R8C/17, R8C/18, R8C/19, R8C/1A, R8C/1B, R8C/28, R8C/29
R0E521174CDB00	: R8C/14, R8C/15, R8C/16, R8C/17, R8C/18, R8C/19, R8C/1A, R8C/1B
R0E521237CFK00	: R8C/20, R8C/21, R8C/22, R8C/23
R0E521258CFJ00	: R8C/24, R8C/25
R0E521276CFG00	: R8C/26, R8C/27
R0E5212BACFG00	: R8C/2A, R8C/2B
R0E5212BACFK00	: R8C/2A, R8C/2B
R0E5212DACFK00	: R8C/2C, R8C/2D
R0E5212L4CFG00	: R8C/2K, R8C/2L

Package Components

Check to see if your product package contains all of the following items before using the product.

1	R0E521000EPB00 emulation probe	1
2	Oscillator circuit board OSC-3 (20MHz)	1
3	Oscillator circuit board OSC-2 (only J1 mounted)	1
4	R0E521000EPB00 Release Notes (English - this document / Japanese)	1/1
5	R0E521000EPB00 User’s Manual (English / Japanese)	1/1

If any of these items are missing or found faulty, please contact your local distributor.

For the Latest Information

Visit our website (URL below). Please use this website providing the latest information of Renesas tool products. Furthermore, the latest version of the included software (emulator debugger and C/C++ compiler package evaluation version) can be downloaded.

http://www.renesas.com/tools

To Contact Us

For technical information on the emulation probe R0E521000EPB00 and emulator debugger, contact us from the following URL.

http://www.renesas.com/inquiry

Notes on Using This Product

Before using this product, be sure to read the user's manual carefully. The following describes the precautions to be observed in common for all groups of the R8C Family microcomputers and those to be observed for each group. The functions that cannot be debugged with this product should please be debugged and evaluated with the on-chip debugging emulator E8a or the actual MCU.

(1) R8C/10, /11, /12 and /13 Groups
- Note on the CPU rewrite mode
  Debugging in CPU rewrite mode where the Erase Suspend function is enabled (FMR40 = "1") cannot be executed. Furthermore, the Block Erase and Byte Program times during CPU rewrite differ with those of the actual MCU.

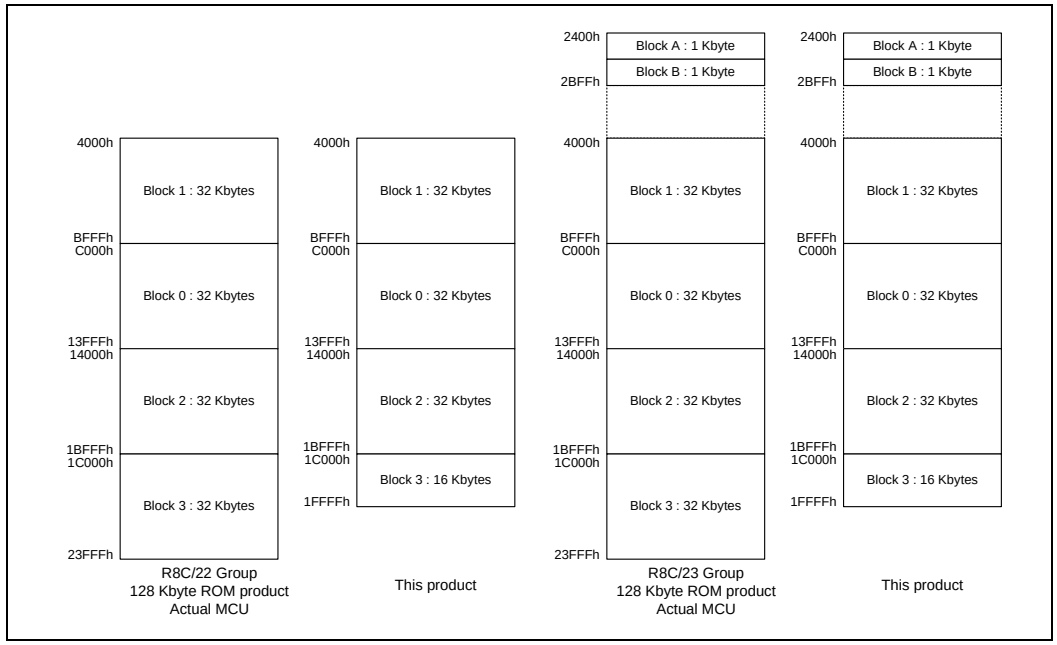
(2) R8C/14 and /15 groups
- Note on the CPU rewrite mode
  Debugging in CPU rewrite mode where the Erase Suspend function is enabled (FMR40 = "1") cannot be executed. Furthermore, the Block Erase and Byte Program times during CPU rewrite differ with those of the actual MCU.
- Note on changing the count source protection mode after reset select bit
  When you change the bit 7 (CSPROINI) of the Option Function Select Register (OFS at address 0FFFFh), by rewriting directly or downloading, the reset operation from the emulator should be done twice or more. Otherwise, the alteration may not be reflected.

(3) R8C/16 and /17 groups
- Note on the CPU rewrite mode
  Debugging in CPU rewrite mode where the Erase Suspend function is enabled (FMR40 = "1") cannot be executed. Furthermore, the Block Erase and Byte Program times during CPU rewrite differ with those of the actual MCU.
- Note on the stop condition detection flag
  When bit 3 (STOP) of the IIC Bus Status Register (ICSR at address 000BCh) is read out, its value is indeterminate.
- Note on changing the count source protection mode after reset select bit (CSPROINI)
  When you change the bit 7 (CSPROINI) of the Option Function Select Register (OFS at address 0FFFFh), by rewriting directly or downloading, the reset operation from the emulator should be done twice or more. Otherwise, the alteration may not be reflected.

(4) R8C/18, /19, /1A and /1B groups
- Note on changing the count source protection mode after reset select bit (CSPROINI)
  When you change the bit 7 (CSPROINI) of the Option Function Select Register (OFS at address 0FFFFh), by rewriting directly or downloading, the reset operation from the emulator should be done twice or more. Otherwise, the alteration may not be reflected.

(5) R8C/20, /21, /22 and /23 groups
- Note on the port XIN-XOUT switch bit (CM13)
  After changing the bit 3 (CM13) of the System Clock Control Register 1 (CM1 at address 00007h) to "1", do not set it to "0". Otherwise, the emulator cannot be operated normally.
- Note on changing the count source protection mode after reset select bit (CSPROINI)
  When you change the bit 7 (CSPROINI) of the Option Function Select Register (OFS at address 0FFFFh), by rewriting directly or downloading, the reset operation from the emulator should be done twice or more. Otherwise, the alteration may not be reflected.
- Note on access to the SFR area from the emulator debugger
  In the memory window, ASM watch window and script window of the emulator debugger, if you reference or modify the SFR area in word, all the areas will be accessed by byte except for some areas of the timer RD related register (00146h--0014Fh, 00156h--0015Fh).
  Note that the SFR area can be accessed from the user program, as specified in the program.
- Note on holding the error flags in serial interfaces
  The clear conditions of the overrun error flag (OER) when using the clock synchronous serial I/O mode and the clock asynchronous serial I/O (UART) mode, and the framing error flag (FER) and the parity error flag (PER) when using the clock asynchronous serial I/O (UART) mode are different form the actual MCU.
  For details, refer to the technical update below.
  http://documentation.renesas.com/eng/products/mpumcu/tu/tn16ca161ae.pdf

- Note on debugging the 128 Kbyte ROM product
  The maximum ROM capacity supported by this product is 112 Kbytes. Therefore, you cannot debug a program larger than 112 Kbytes. The following shows the Flash Memory Block Diagram for when using with this product, taking the R8C/22 and /23 groups as an example.



(6) R8C/24 and /25 groups
- Note on the port XCIN-XCOUT switch bit (CM04)
  After changing the bit 4 (CM04) of the System Clock Control Register 0 (CM0 at address 00006h) to “1” (XIN-XOUT pin), do not set it to “0” (I/O ports, P4_3, P4_4). Otherwise, the emulator cannot be operated normally.
- Note on the XCIN-XCOUT on-chip feedback resistor select bit (CM12)
  The functions associated with bit 2 (CM12) of System Clock Control Register 1 (CM1 at address 00007h) cannot be used. When writing to CM12, always be sure to write a “0”. This bit reads as “0” when read out.
- Note on the port XIN-XOUT switch bit (CM13)
  After changing the bit 3 (CM13) of the System Clock Control Register 1 (CM1 at address 00007h) to “1”, do not set it to “0”. Otherwise, the emulator cannot be operated normally.
- Note on voltage monitor 0 reset
  This product does not support voltage monitor 0 reset and Voltage Monitor 0 Circuit Control Register (VW0C at address 00038h).
  Therefore, do not access the Voltage Monitor 0 Circuit Control Register.
- Note on the voltage monitor 1 interrupt
  This product supports only voltage monitor 1 reset, and does not support the voltage monitor 1 interrupt. Therefore, when setting bit 0 (voltage monitor 1 interrupt/reset enable bit: VW1C0) of the Voltage Monitor 1 Circuit Control Register (VW1C at address 00036h) to “1”(= enable), always make sure that bit 6 (voltage monitor 1 circuit mode select bit: VW1C6) is also set to “1”(= voltage monitor 1 circuit reset mode).
- Note on the Port 2 Drive Capability Control Register (P2DRR)
  Be aware that the Port 2 Drive Capability Control Register (P2DRR at address 000F4h) in this product is subject to limitations that although the drive capability of the n-channel (Low side) output transistor can be increased, that of the p-channel (High side) output transistor cannot be increased.
- Note on the voltage detection 0 circuit start bit (LVD0ON)
  The function of bit 5 (LVD0ON) in the Option Function Select Register (OFS at address 0FFFFh) cannot be used. When writing to this register, always be sure to set LVD0ON to “1”.
- Note on changing the count source protection mode after reset select bit (CSPROINI)
  When you change the bit 7 (CSPROINI) of the Option Function Select Register (OFS at address 0FFFFh), by rewriting directly or downloading, the reset operation from the emulator should be done twice or more. Otherwise, the alteration may not be reflected.
- Note on access to the SFR area from the emulator debugger
  In the memory window, ASM watch window and script window of the emulator debugger, if you reference or modify the SFR area in word, all the areas will be accessed by byte except for some areas of the timer RD related register (00146h--0014Fh, 00156h--0015Fh).
  Note that the SFR area can be accessed from the user program, as specified in the program.
- Note on holding the error flags in serial interfaces
  The clear conditions of the overrun error flag (OER) when using the clock synchronous serial I/O mode and the clock asynchronous serial I/O (UART) mode, and the framing error flag (FER) and the parity error flag (PER) when using the clock asynchronous serial I/O (UART) mode are different form the actual MCU.
  For details, refer to the technical update below.
  http://documentation.renesas.com/eng/products/mpumcu/tu/tn16ca161ae.pdf
- Note on the High-Speed On-Chip Oscillator Control Register 4 (FRA4) and High-Speed On-Chip Oscillator Control Register 6 (FRA6)
  This product does not support High-Speed On-Chip Oscillator Control Register 4 (FRA4: address 00029h) and High-Speed On-Chip Oscillator Control Register 6 (FRA6: address 0002Bh). If you read FRA4 or FRA6 register, an undefined value is read in. Do not transfer the value to FRA1 register.
- Note on the High-Speed On-Chip Oscillator Control Register 7 (FRA7)
  This product does not support High-Speed On-Chip Oscillator Control Register 7 (FRA7: address 0002Ch). If you read FRA7 register, an undefined value is read in. Do not transfer the value to FRA1 register.

(7) R8C/26, /27, /28 and /29 Groups

- Note on the XCIN-XCOUT, XIN-XOUT on-chip feedback register select bit (CM12 and CM11)
  The functions associated with bits 2 and 1 (CM12 and CM11) of System Clock Control Register 1 (CM1 at address 00007h) cannot be used. When writing to CM12 and CM11, always be sure to write a “0”. This bit reads as “0” when read out.
- Note on the port XIN-XOUT switch bit (CM13)
  After changing the bit 3 (CM13) of the System Clock Control Register 1 (CM1 at address 00007h) to “1”, do not set it to “0”. Otherwise, the emulator cannot be operated normally.
- Note on using low-speed clock mode
  When using low-speed clock mode, always be sure to set the bit 3 (CM13) of the System Clock Control Register 1 (CM1 at address 00007h) to “1” (XIN-XOUT pin) before setting bit 2 (OCD2) of the Oscillation Stop Detection Register (OCD at address 0000Ch) to “0” (XIN clock selected).
- Note on XCIN clock source and selecting clock to the target MCU
  When using the internal clock as an XCIN clock source, built a desired oscillator circuit on the included OSC-2 oscillator circuit bare board and replace the oscillator circuit board on the emulator.
  Choose “Internal” to main-clock and sub-clock in the Init dialog box of emulator tab after starting up the emulator debugger. When using a clock on the user system, choose “External” to main-clock and sub-clock.
- Note on voltage monitor 0 reset
  This product does not support voltage monitor 0 reset and Voltage Monitor 0 Circuit Control Register (VW0C at address 00038h).
  Therefore, do not access the Voltage Monitor 0 Circuit Control Register.
- Note on the voltage monitor 1 interrupt
  This product supports only voltage monitor 1 reset, and does not support the voltage monitor 1 interrupt. Therefore, when setting bit 0 (voltage monitor 1 interrupt/reset enable bit: VW1C0) of the Voltage Monitor 1 Circuit Control Register (VW1C at address 00036h) to “1”(= enable), always make sure that bit 6 (voltage monitor 1 circuit mode select bit: VW1C6) is also set to “1”(= voltage monitor 1 circuit reset mode).
- Note on the Port 1 Drive Capability Control Register (P1DRR)
  Be aware that the Port 1 Drive Capability Control Register (P1DRR at address 000FEh) in this product is subject to limitations that although the drive capability of the n-channel (Low side) output transistor can be increased, that of the p-channel (High side) output transistor cannot be increased.
- Note on the voltage detection 0 circuit start bit (LVD0ON)
  The function of bit 5 (LVD0ON) in the Option Function Select Register (OFS at address 0FFFFh) cannot be used. When writing to this register, always be sure to set LVD0ON to “1”.
- Note on changing the count source protection mode after reset select bit (CSPROINI)
  When you change the bit 7 (CSPROINI) of the Option Function Select Register (OFS at address 0FFFFh), by rewriting directly or downloading, the reset operation from the emulator should be done twice or more. Otherwise, the alteration may not be reflected.
- Note on using the timer RA output pin (TRAO) function
  When using the port P3_7/TRAO/SSO/RXD1/(TXD1) pin as the TRAO pin function, set the bit4 (reserved bit) of the Pin Select Register 2 (PINSR2: address 000F6h) to “1” before using it. If you read out this register, “1” is read out after setting the bit to “1”.
- Note on access to the SFR area from the emulator debugger
  In the memory window, ASM watch window and script window of the emulator debugger, if you reference or modify the SFR area in word, all the areas will be accessed by byte except for some areas of the timer RC related register (00126h--0012Fh).
  Note that the SFR area can be accessed from the user program, as specified in the program.
- Note on the bit2 of the Pin Select Register 1 (PINSR1)
  If you read out the bit2 (reserved bit) of the Pin Select Register 1 (PINSR1: address 000F5h), “0” is read out when resetting the MCU and “1” is read out when setting the bit2 to “1”. For the actual MCU, “0” is read out although “1” is set.
- Note on the bit5, bit2, bit1 and bit0 of the Pin Select Register 3 (PINSR3)
  Before using the timer RC or timer RE, be sure to set the bit5, bit2, bit1 and bit0 (reserved bits) of the Pin Select Register 3 (PINSR3: address 000F7h) to “1”. If you read out these reserved bits, “0” is read out when resetting the MCU and “1” is read out when setting these bits to “1”. For the actual MCU, “0” is read out although “1” is set.
- Note on holding the error flags in serial interfaces
  The clear conditions of the overrun error flag (OER) when using the clock synchronous serial I/O mode and the clock asynchronous serial I/O (UART) mode, and the framing error flag (FER) and the parity error flag (PER) when using the clock asynchronous serial I/O (UART) mode are different form the actual MCU.
  For details, refer to the technical update below.
  http://documentation.renesas.com/eng/products/mpumcu/tu/tn16ca161ae.pdf
- Note on the High-Speed On-Chip Oscillator Control Register 4 (FRA4) and High-Speed On-Chip Oscillator Control Register 6 (FRA6)
  This product does not support High-Speed On-Chip Oscillator Control Register 4 (FRA4: address 00029h) and High-Speed On-Chip Oscillator Control Register 6 (FRA6: address 0002Bh). If you read FRA4 or FRA6 register, an undefined value is read in. Do not transfer the value to FRA1 register.
- Note on the High-Speed On-Chip Oscillator Control Register 7 (FRA7)
  This product does not support High-Speed On-Chip Oscillator Control Register 7 (FRA7: address 0002Ch). If you read FRA7 register, an undefined value is read in. Do not transfer the value to FRA1 register.
- Note on the Port Mode Register (PMR)
  The hardware manual says, 'If you write to the bit2 of the Port Mode Register (PMR: address 000F8h), write “0”. When reading the value, “0” is read out.' However, with this product, be sure to write “1” to the bit2 of the port mode register. When reading the value, “1” is read out.

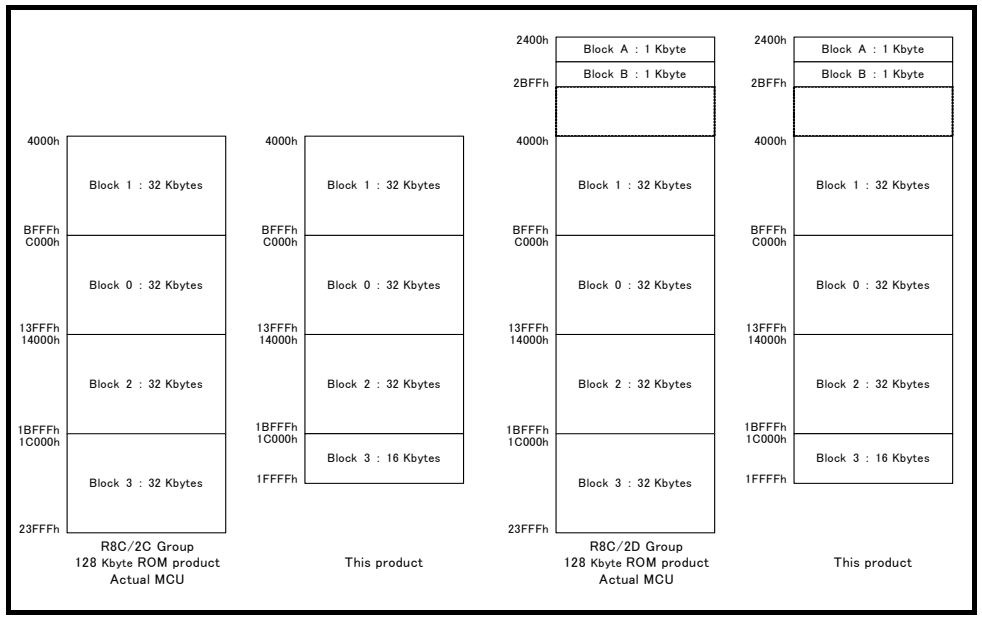
(8) R8C/2A, /2B, /2C, /2D Groups

- Note on the port XCIN-XCOUT switch bit (CM04)
  After changing the bit 4 (CM04) of the System Clock Control Register 0 (CM0 at address 00006h) to “1” (XCIN-XCOUT pin), do not set it to “0” (I/O ports, P4_3, P4_4). Otherwise, the emulator cannot be operated normally.
- Note on the XCIN-XCOUT on-chip feedback resistor select bit (CM12)
  The functions associated with bit 2 (CM12) of System Clock Control Register 1 (CM1 at address 00007h) cannot be used. When writing to CM12, always be sure to write a “0”. This bit reads as “0” when read out.
- Note on the port XIN-XOUT switch bit (CM13)
  After changing the bit 3 (CM13) of the System Clock Control Register 1 (CM1 at address 00007h) to “1”, do not set it to “0”. Otherwise, the emulator cannot be operated normally.
- Note on the Module Standby Control Register (MSTCR)
  This product does not support the module standby control register (MSTCR: 00008h). Therefore each function of IIC bus, timer RD and timer RC cannot be stopped.
- Note on the Emulator specified High-Speed On-Chip Oscillator Control Register 0 (EMFRA0), 2 (EMFRA2)
  This product has the emulator specified high-speed on-chip oscillator control register 0 (EMFRA0 at address 00223h) and the emulator specified high-speed on-chip oscillator control register 2 (EMFRA2 at address 00225h). When rewriting the high-speed on-chip oscillator control register 0 (FRA0 at address 00023h), write in EMFRA0 register. And when rewriting the high-speed on-chip oscillator control register 2 (FRA2 at address 00025h), write same value in EMFRA2 register. Note that the bit assignment and R/W condition of both EMFRA0 register and EMFRA2 register are the same with the ones of FRA0 register and FRA2 register.
- Note on the High-Speed On-Chip Oscillator Control Register 1 (FRA1)
  Do not change the high-speed on-chip oscillator control register 1 (FRA1 at address 00024h) while using this product. If FRA1 register is changed, some parts of functions cannot be operated normally.
- Note on the High-Speed On-Chip Oscillator Control Register 6 (FRA6)
  This product does not support High-Speed On-Chip Oscillator Control Register 6 (FRA6: address 0002Bh). If you read FRA6 register, an undefined value is read in. Do not transfer the value to FRA1 register.
- Note on the High-Speed On-Chip Oscillator Control Register 7 (FRA7)
  This product does not support High-Speed On-Chip Oscillator Control Register 7 (FRA7: address 0002Ch). If you read FRA7 register, an undefined value is read in. Do not transfer the value to FRA1 register.
- Note on the voltage monitor 0 reset
  This product does not support the voltage monitor 0 reset and the voltage monitor 0 circuit control register (VW0C at address 00038h).
  Therefore, does not access the voltage monitor 0 circuit control register.
- Note on the voltage monitor 1 interrupt
  This product supports only voltage monitor 1 reset, and does not support the voltage monitor 1 interrupt. Therefore, when setting bit 0 (voltage monitor 1 interrupt/reset enable bit: VW1C0) of the voltage monitor 1 circuit control register (VW1C at address 00036h) to “1”(= enable), always make sure that bit 6 (voltage monitor 1 circuit mode select bit: VW1C6) is also set to “1”(= voltage monitor 1 circuit reset mode).
- Note on the Port P2 Drive Capacity Control Register (P2DRR)
  Be aware that the Port P2 drive capacity control register (P2DRR at address 000F4h) in this product is subject to limitations that although the drive capability of the n-channel (Low side) output transistor can be increased, that of the p-channel (High side) output transistor cannot be increased.
- Note on the UART1 Function Select Register (U1SR)
  When writing to the bit0 and bit1 of the UART1 Function Select Register (U1SR: address 000F5h) while using this product, always be sure to write “1”. When reading the value, “1” is read out.
- Note on the voltage detection 0 circuit start bit (LVD0ON)
  The function of bit 5 (LVD0ON) in the option function select register (OFS at address 0FFFFh) cannot be used. When writing to this register, always be sure to set LVD0ON to “1”.
- Note on changing the count source protection mode after reset select bit (CSPROINI)
  When you change the bit 7 (CSPROINI) of the option function select register (OFS at address 0FFFFh), by rewriting directly in the memory window or downloading, the reset operation from the emulator debugger should be done twice or more. Otherwise, the alteration may not be reflected.
- Note on using the A/D conversion start trigger by Timer RD (complementary PWM mode)
  This product does not support the function of setting the bit 5 (A/D conversion trigger select bit: ADCAP) of the A/D control register 0 (ADC0N0 at address 002D6h) to “1” (starts at timer RD with complementary PWM mode). The usable A/D conversion trigger in this product is only software trigger which sets ADCAP bit to “0”.
- Note on using interrupts and changing an interrupt control register
  With the following registers, if an interrupt request corresponding to a register is generated while executing the AND, OR, BCLR and BSET instructions that change any bit other than the IR bit, the IR bit is not set to “1”(interrupt requested), and the interrupt request is ignored. This behavior is different from the actual MCU.
  Applicable registers:

Compare 1 Interrupt Control Register	CMP1IC
Timer RF Interrupt Control Register	TRFIC
Compare 0 Interrupt Control Register	CMP0IC
A/D Conversion Interrupt Control Register	ADIC
Capture Interrupt Control Register	CAPIC

- Note on access to the SFR area from the emulator debugger
  In the memory window, ASM watch window and script window of the emulator debugger, if you reference or modify the SFR area in word unit, all the areas will be accessed by byte except for some areas of the timer RC related registers (00126h--0012Fh).
  Note that the SFR area can be accessed from the user program, as specified in the program.

- Note on debugging the 128 Kbyte ROM products
  The maximum ROM capacity supported by this product is 112 Kbytes. You cannot debug a program larger than 112 Kbytes (20000h—23FFFh). The following shows the Flash Memory Block Diagram for when using with this product, taking the R8C/2C and /2D Groups as an example.



(9) R8C/2K, /2L Groups
- Note on the port XIN-XOUT switch bit (CM13)
  After changing the bit 3 (CM13) of the System Clock Control Register 1 (CM1 at address 00007h) to “1”, do not set it to “0”. Otherwise, the emulator cannot be operated normally.
- Note on the High-Speed On-Chip Oscillator Control Register 6 (FRA6)
  This product does not support High-Speed On-Chip Oscillator Control Register 6 (FRA6: address 0002Bh). If you read FRA6 register, an undefined value is read in. Do not transfer the value to FRA1 register.
- Note on the High-Speed On-Chip Oscillator Control Register 7 (FRA7)
  This product does not support High-Speed On-Chip Oscillator Control Register 7 (FRA7: address 0002Ch). If you read FRA7 register, an undefined value is read in. Do not transfer the value to FRA1 register.
- Note on the voltage monitor 0 reset
  This product does not support the voltage monitor 0 reset and the voltage monitor 0 circuit control register (VW0C at address 00038h).
  Therefore, do not access the voltage monitor 0 circuit control register.
- Note on the voltage monitor 1 interrupt
  This product supports only voltage monitor 1 reset, and does not support the voltage monitor 1 interrupt. Therefore, when setting bit 0 (voltage monitor 1 interrupt/reset enable bit: VW1C0) of the voltage monitor 1 circuit control register (VW1C at address 00036h) to “1”(= enable), always make sure that bit 6 (voltage monitor 1 circuit mode select bit: VW1C6) is also set to “1”(= voltage monitor 1 circuit reset mode).
- Note on the Port P2 Drive Capacity Control Register (P2DRR)
  Be aware that the Port P2 drive capacity control register (P2DRR at address 000F4h) in this product is subject to limitations that although the drive capability of the n-channel (Low side) output transistor can be increased, that of the p-channel (High side) output transistor cannot be increased.
- Note on the voltage detection 0 circuit start bit (LVD0ON)
  The function of bit 5 (LVD0ON) in the option function select register (OFS at address 0FFFFh) cannot be used. When writing to this register, always be sure to set LVD0ON to “1”.
- Note on changing the count source protection mode after reset select bit (CSPROINI)
  When you change the bit 7 (CSPROINI) of the option function select register (OFS at address 0FFFFh), by rewriting directly in the memory window or downloading, the reset operation from the emulator debugger should be done twice or more. Otherwise, the alteration may not be reflected.
- Note on access to the SFR area from the emulator debugger
  In the memory window, ASM watch window and script window of the emulator debugger, if you reference or modify the SFR area in word unit, all the areas will be accessed by byte except for some areas of the timer RC related registers (00126h--0012Fh).
  Note that the SFR area can be accessed from the user program, as specified in the program.