Sigma-Delta Calibration Technique

TB329
Rev.1.00
May 1995

Introduction

While the analog modulator is critically important in determining accuracy of a sigma delta ADC, digital calibration techniques are essential for reducing offset and gain errors, as well as improving linearity. Intersil sigma delta analog to digital converters use a unique three point calibration technique (patent pending) which minimizes offset error and supports unique gain correction factors for positive and negative voltages, thus improving linearity. The following is a brief description of how the calibration coefficients are generated and applied. In addition, range detection and data coding are discussed. This document applies to both the HI719X and HI718X family of sigma delta ADCs.

The block diagram of Figure 1 is a simplified sigma delta converter with emphasis on the calibration functions. The sigma delta modulator produces a 1-bit data stream that is digitally filtered. The one's density of this data stream within a given period of time provides a digital representation of the analog input at the modulator. The digital filter output is calibrated by subtracting offset and correcting for gain error. Over and under range conditions are checked before the calibrated data is coded and stored in memory.

Calibration Coefficient Generation

A complete calibration requires the calibration logic to record conversion results under three different input conditions. A "zero scale" input is used to eliminate offset error, a "positive full scale" input is used to generate a gain correction coefficient for positive input voltages and a "negative full scale" input is used to generate a gain correction coefficient for negative input voltages.

When generating calibration coefficients, the input to the modulator may come from an external system input to the device or it can be generated internally. System calibration coefficients are generated by using the system inputs to the converter. System calibration allows the user to correct both system component and converter offset and gain errors at one time. Self calibration coefficients are generated by internally configuring the inputs to the modulator while disconnecting the external system inputs. Self calibration compensates for the converters internal offset and gain errors. The HI719X and HI718X products support various calibration modes, including system and self calibration operations. See the specific product data sheet for details.

During offset calibration, the "zero scale" voltage is supplied to the input of the converter. After converting this input, the Offset Correction Register is updated with the digital filter output, which is the offset correction factor. The Offset Correction Register contains a two's complement number that can be positive or negative, depending on the offset correction required.

During positive gain calibration, the "positive full scale" voltage is supplied to the input of the converter. After completing a conversion, the Positive Gain Coefficient Register is updated with offset corrected data for this voltage. This data is a positive two's complement number which is used to calculate a gain correction factor for all positive input voltages.

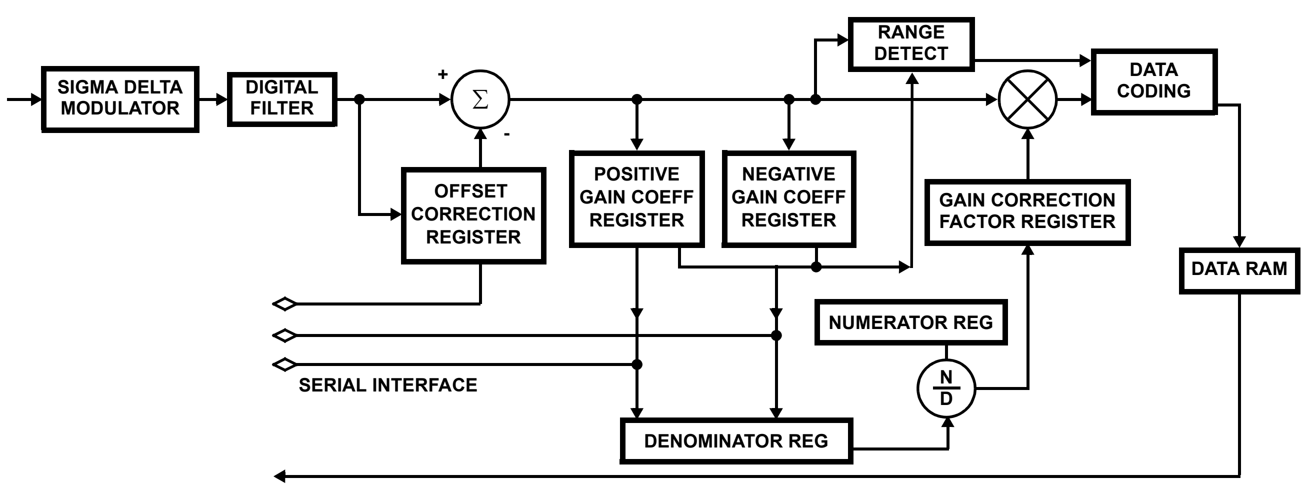

FIGURE 1. SIMPLIFIED CONVERTER BLOCK DIAGRAM

During negative gain calibration, the "negative full scale" voltage is supplied to the input of the converter. After completing a conversion, the Negative Gain Coefficient Register is updated with offset corrected data for this voltage. This data is a negative two's complement number which is used to calculate a gain correction factor for all negative input voltages.

The order of the gain coefficient generation is not important but the offset coefficient must be generated before either of the gain coefficients. For proper calibration, the gain coefficients must have offset error removed before storage in memory. The flow chart below describes a proper method for generating the converter calibration coefficients using the system inputs.

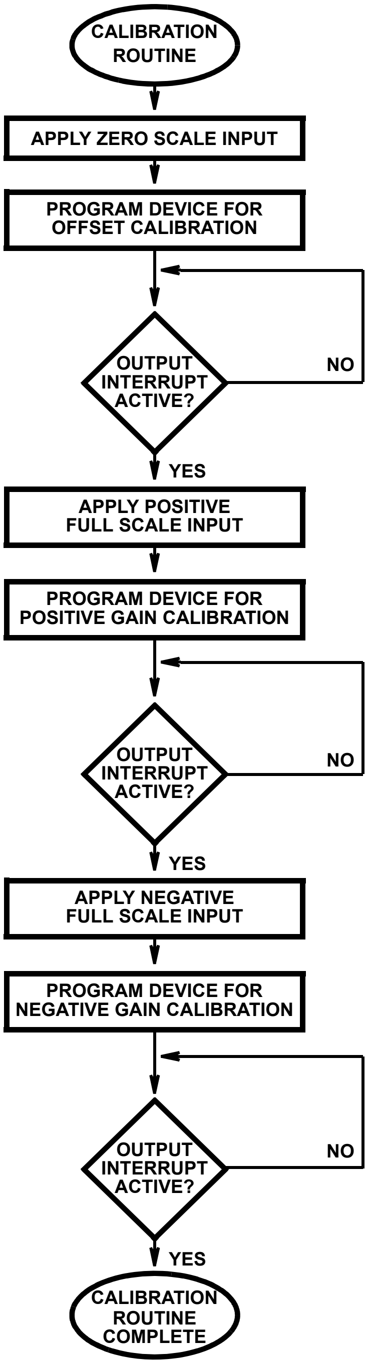

FIGURE 2.

Calibrating Conversion Results

In normal operating mode, every conversion is followed by a data calibration phase. Data calibration is as follows:

1. Offset is subtracted.
2. The polarity of the offset corrected data is determined and the proper gain correction factor is generated.
3. The offset calibrated data is multiplied by the gain correction factor generated in step two. This completes gain calibration.
4. The offset corrected data is checked for over or under range error before final coding (two's complement, offset binary or, in unipolar mode, binary).

The calibrated, coded data is stored in memory and the user is notified of a completed conversion via an output interrupt signal.

Offset Calibration

Offset Calibration is a simple two's complement subtraction. Each conversion has offset error removed by subtracting the contents of the Offset Correction Register from the digital filter output.

Gain Calibration

Gain calibration is a two step process. First, the proper gain correction factor is generated. Then this factor is multiplied by the offset corrected data, completing gain calibration.

The gain correction factor is generated via the divider (N/D) shown in Figure 1. After offset calibration has been completed, the converter determines which gain coefficient to use for generation of the gain correction factor. If the offset corrected data is positive, the positive gain coefficient is the denominator when determining the gain correction factor. If the offset corrected data is negative, the two's complement of the negative gain coefficient is the denominator when determining the gain correction factor.

The input span (numerator), used to generate the gain correction factor is different for bipolar versus unipolar mode. In unipolar mode the calibration logic determines the gain correction factor by dividing the total internal resolution of the converter (2^N) by the span between the zero scale and positive full scale points. In bipolar mode the gain factor is determined by dividing one half the total internal resolution (2^{N-1}) of the converter by the span between the zero scale (bipolar midscale) and ± full scale points.

In either unipolar or bipolar mode, the division result is the gain correction factor and is multiplied by the offset corrected filter output to calculate the proper digital output of the converter. The gain correction factor is not permanently stored but is generated for each conversion. The Gain Correction Factor Register is not accessible via the serial interface.

Range Detection

In addition to the calibration process, the converter detects over range above positive full scale and under range below minus full scale conditions. Over or under range detection affects the output data coding as described in the Data Coding section.

Over range detection is identical for both bipolar and unipolar operation. Over range is detected by comparing the offset corrected filter output to the positive gain coefficient. If the current offset corrected filter value is greater than the positive gain coefficient, an over range condition is detected.

In unipolar mode, under range is detected by sampling the sign bit of the offset calibrated data. If the sign bit is logic 1, signifying a negative voltage, an under range condition exists.

In bipolar mode, under range is detected by comparing the offset corrected filter output to the negative gain coefficient. If the current offset corrected filter value is less than the negative gain coefficient, an under range condition is detected.

Data Coding

The calibrated data can be obtained in one of various numerical codes depending on the bipolar/unipolar mode bit and the two's complement coding bit. In bipolar mode, if the two's complement bit is true, the output is two's complement. In bipolar mode, offset binary coding is used when the two's complement coding bit is not true. In unipolar mode, only binary coding is available and the two's complement coding bit is a don't care.

The output coding tables for the HI719X 24-bit family of products is shown below. V_{ZS} represents the applied zero scale input during system calibration or is AGND if internal calibration was performed. V_{PFS} represents the applied positive full scale input during system calibration or is V_{REF} if internal calibration was performed. V_{NFS} represents the applied negative full scale input during system calibration or is $-V_{REF}$ if internal calibration was performed.

TABLE 1. BIPOLAR MODE OUTPUT CODES 24-BIT

INPUT VOLTAGE	TWO'S COMPLEMENT CODE	OFFSET BINARY CODE
>(V_{PFS} - 1.5 LSB)	7FFFFF	FFFFFF
V_{PFS} - 1.5 LSB	7FFFFF/7FFFFE	FFFFFF/FFFFFE
V_{ZS} - 0.5 LSB	000000/FFFFFF	800000/7FFFFF
V_{NFS} + 0.5 LSB	800001/800000	000001/000000
<(V_{NFS} + 0.5 LSB)	800000	000000

TABLE 2. UNIPOLAR MODE DATA OUTPUT CODES 24-BIT

INPUT VOLTAGE	BINARY CODE
>(V_{PFS} - 1.5 LSB)	FFFFFF
V_{PFS} - 1.5 LSB	FFFFFF/FFFFFE
V_{PFS}/2 - 0.5 LSB	800000/7FFFFF
V_{ZS} + .5 LSB	000001/000000
<(V_{ZS} + 0.5 LSB)	000000

When the range detection logic determines an over range, the converter output will clamp at the >(V_{PFS} - 1.5 LSB) output as described in Table 1 or 2. When the range detection logic determines an under range, the converter output will clamp at the <(V_{NFS} + 0.5 LSB) output described in Table 1 or the <(V_{ZS} + 0.5 LSB) output described in Table 2.

Additional Notes

The calibration logic can be effectively bypassed by writing the Offset Correction Register to 000000 (hex) and the Gain Coefficient registers to 800000 (hex). This forces zero offset correction and a gain correction factor of 1.

The Offset Correction Register and the two Gain Coefficient registers are read/write accessible via the device serial interface.

The HI719X and HI718X products support an ability to ignore the negative gain coefficient when generating the gain correction factor. Each product has the ability to use only the positive gain coefficient when determining the gain correction factor. This feature is not recommended, but has been included to maintain compatibility with industry standard converters. In unipolar mode the negative gain coefficient is not used and does not require generation.

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338

Colophon 7.0