LLDRAM-Ⅲ 『RMHE41A364AGBG』

Exact Match Search Solution

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This document is an overview of Exact Match Search Solution using Renesas Low-Latency-DRAM『LLDRAM-Ⅲ』

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1. Exact Match Search Solution

1.1 Introduction

In recent years, network-virtualization is evolving by new technology such as SDN『Software-Defined Networking』 and NFV『Network Functions Virtualization』. To realize SDN, Openflow® specification is constantly being updated with new functions. Data-plane hardware such as router or switch is requested to implement above new functions. Although NFV data-plane functions can be implemented by software using microprocessors, network system performance may suffer due to slow software processing. Figure-1 shows one of the solution to achieve both flexible functionality and high performance. Network equipment by FPGA enables the implementation of new programmable functions and the execution of high speed packet processing at same time.

On the other hand one of the crucial bottlenecks of data-plane hardware is packet header search speed. Network equipment search for the information corresponding to packet header from search database and then transfer the received packet to destination host by executing packet processing according to search result information. Search database on network equipment is becoming more large scale because of the increasing network traffic and the requirement of more complex search table for security applications, etc. Large scale search databases from thousands to hundreds of thousands of entries are hard for FPGA devices to search at high search rate. Therefore special off-load search engine chip is often used for these solutions.

Exact Match Search Solution using『LLDRAM-Ⅲ』is a search-engine to upgrade search performance for network system implemented by FPGA. Instead of using special off-load search engine, this solution uses a combination of Search IP implemented in FPGA and LLDRAM-Ⅲfor database storage. LLDRAM-Ⅲ is low-latency DRAM developed by Renesas for network applications.

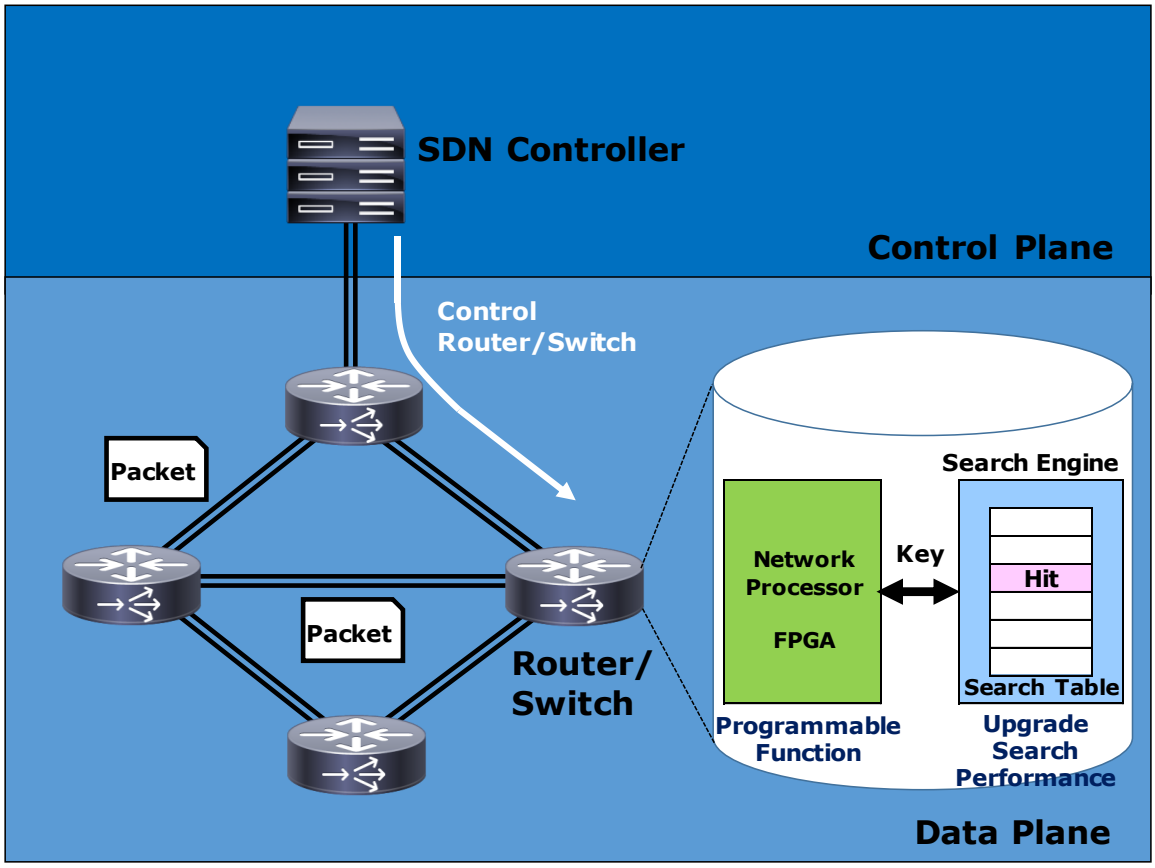


Figure 1 Network equipment implemented by FPGA

1.2 Packet Header Search for 100Gbit Network Traffic

Packet Header Search application using DRAM technology typically extracts the search key from the packet by user-logic in FPGA. This key information is then applied to the search-table in memory chip such as the example shown in figure-2. FPGA receives packets from multiple host-computers connected to the network at random and each packet has a unique packet header. As a result, Search IP receives a random search key from the user logic and perform random accesses to the attached memory chip to search the entry corresponding to the key. This means the key performance of Search IP using DRAM technology is highly dependent on random access performance of the DRAM memory.

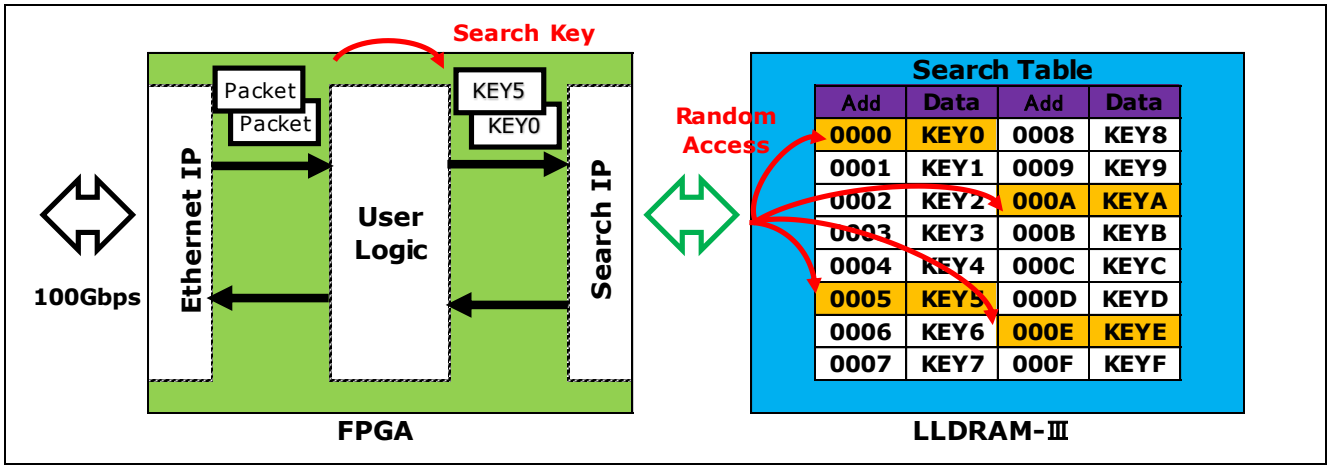


Figure 2 Bottleneck of search performance on Search solution using DRAM technology

Renesas Low-Latency DRAM 『LLDRAM-Ⅲ』 allows 400M access per second at random access .This is 4 times faster than DDR3 SDRAM such as figure-3. Exact Match Search Solution use LLDRAM-Ⅲ with newly developed search IP is optimized for LLDRAM-Ⅲ to further improve DRAM random access bottleneck.

It enables 100Gpbs traffic class packet header search for 1 million entry search table with max 2W power consumption.

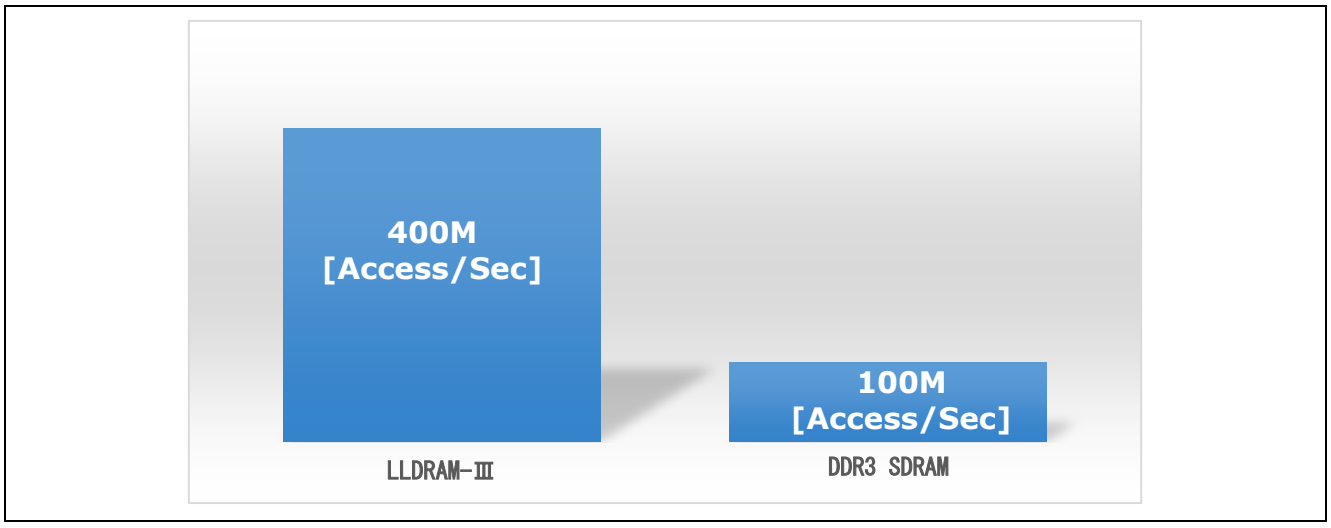


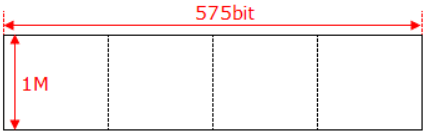
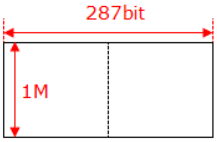
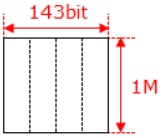
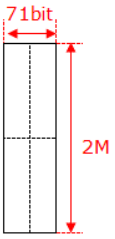
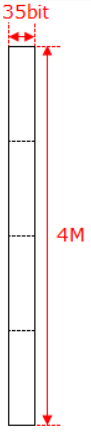
Figure 3 LLDRAM-Ⅲ Random Access performance

1.3 Search Table Configuration

LLDRAM-Ⅲ is 1.1Gbit high density DRAM and enables the configuration of bigger search tables. 5 types of search table configurations are available such as figure-4. Customer can select the most suitable configuration based on search key width and table entries requirements. When implementing Exact-Match IP RTL netlist to FPGA,3-type netlist is available according to search key length. (Type-3: ①575bit / Type-2: ②287bit / Type-1: ③143bit)

If Type-1 is selected, 2-type table configurations are available additionally by setting internal register. (④71bit / ⑤35bit)

Due to the low power consumption of under 2W for LLDRAM-III, Exact Match Search solution is suitable for large scale search table applications.

Netlist Type	Address Mode(*)	Table Dencity	Table Configration Image
Type-3	3'b001	575-bit x 1M-Entry	
Type-2	3'b001	287-bit x 1M-Entry	
Type-1	3'b001	143-bit x 1M-Entry	
	3'b010	71-bit X 2M-Entry	
	3'b100	35-bit X 4M-Entry	

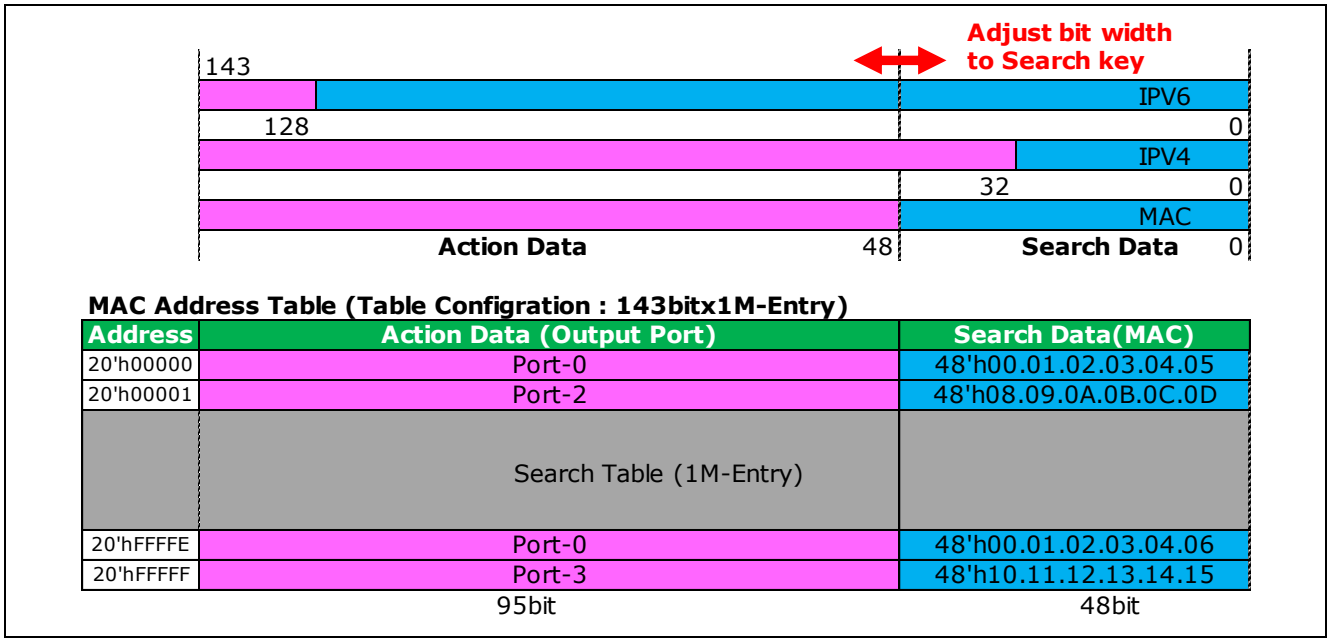
(*) Internal Register Data

Figure 4 Available search table configurations

1.4 Search Key Width

Within a search table, the width of the data bit field that are compared with the search key (defined as Search Data in figure-5) can be flexibly assigned in LLDRAM-Ⅲ. Search Data can be adjusted to 32bit for IPV4 address Search and 48bits for MAC address Search as an example.

On the other hand, Extra bits (defined as Action Data in figure-5) can be used to store action data. Action data indicates action which should be execute when search result is hit. For example LSB48bit data assigned to search data for MAC address search and the remaining 95bits can be assigned to action data under 143bit x 1M-entry table configuration shown as figure-5.



MAC Address Table (Table Configration : 143bitx1M-Entry)

Address	Action Data (Output Port)	Search Data(MAC)
20'h00000	Port-0	48'h00.01.02.03.04.05
20'h00001	Port-2	48'h08.09.0A.0B.0C.0D
	Search Table (1M-Entry)	
20'hFFFFE	Port-0	48'h00.01.02.03.04.06
20'hFFFFF	Port-3	48'h10.11.12.13.14.15
	95bit	48bit

Figure 5 Adjusting Search Data Width to Search Key

If Search Data is assigned to MAC address and Action data is assigned to port number to transfer the received packet such as figure-5, FPGA can receive port number as search result from LLDRAM-Ⅲ directly. FPGA can transfer the packet according to port number returned from LLDRAM-Ⅲ such as figure-6.

Conventional Search engine requires additional action memory to store action data.

If action data is stored into LLDRAM-Ⅲ, Exact Match Search Solution has the following advantages.

●Cost/Power consumption/PCB-area reduction by eliminating action memory

●FPGA resource reduction to control action memory (I/O-Pin and so on)

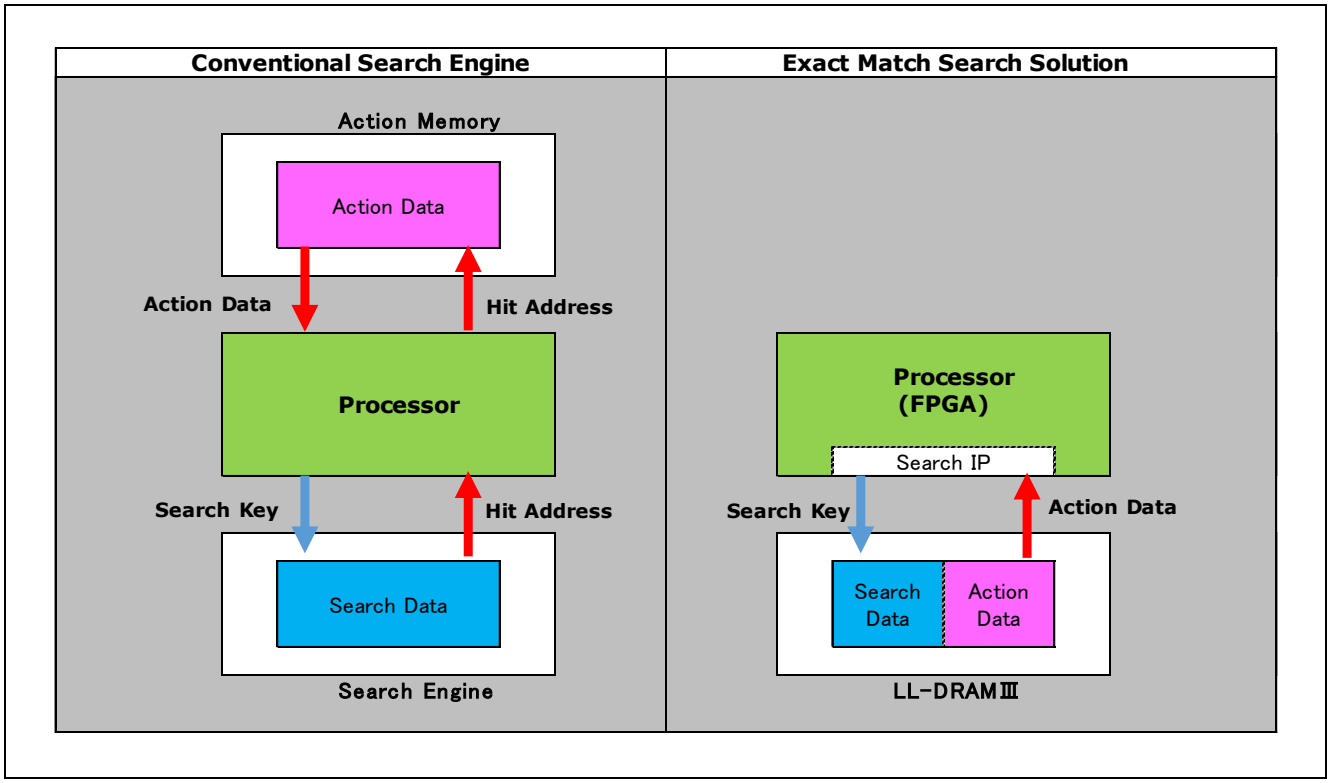


Figure 6 Action Data

1.5 Exact Match Search IP Block Diagram

Exact Match Search IP Block Diagram is described in figure-7. Exact Match Search IP implemented in FPGA consists of 2 modules. It controls LLDRAM-Ⅲ to execute search solution.

●Search Control IP Module

This module receives search-key or table maintenance command from user-logic designed by customer and executes search function or configures search-table according to commands.

●LLDRAM-ⅢControl IP Module

This module is User-IF module between LLDRAM-Ⅲ and Search Control IP Module. This module receives Write/Read command generated by Search Control IP Module and controls LLDRAM-Ⅲ.

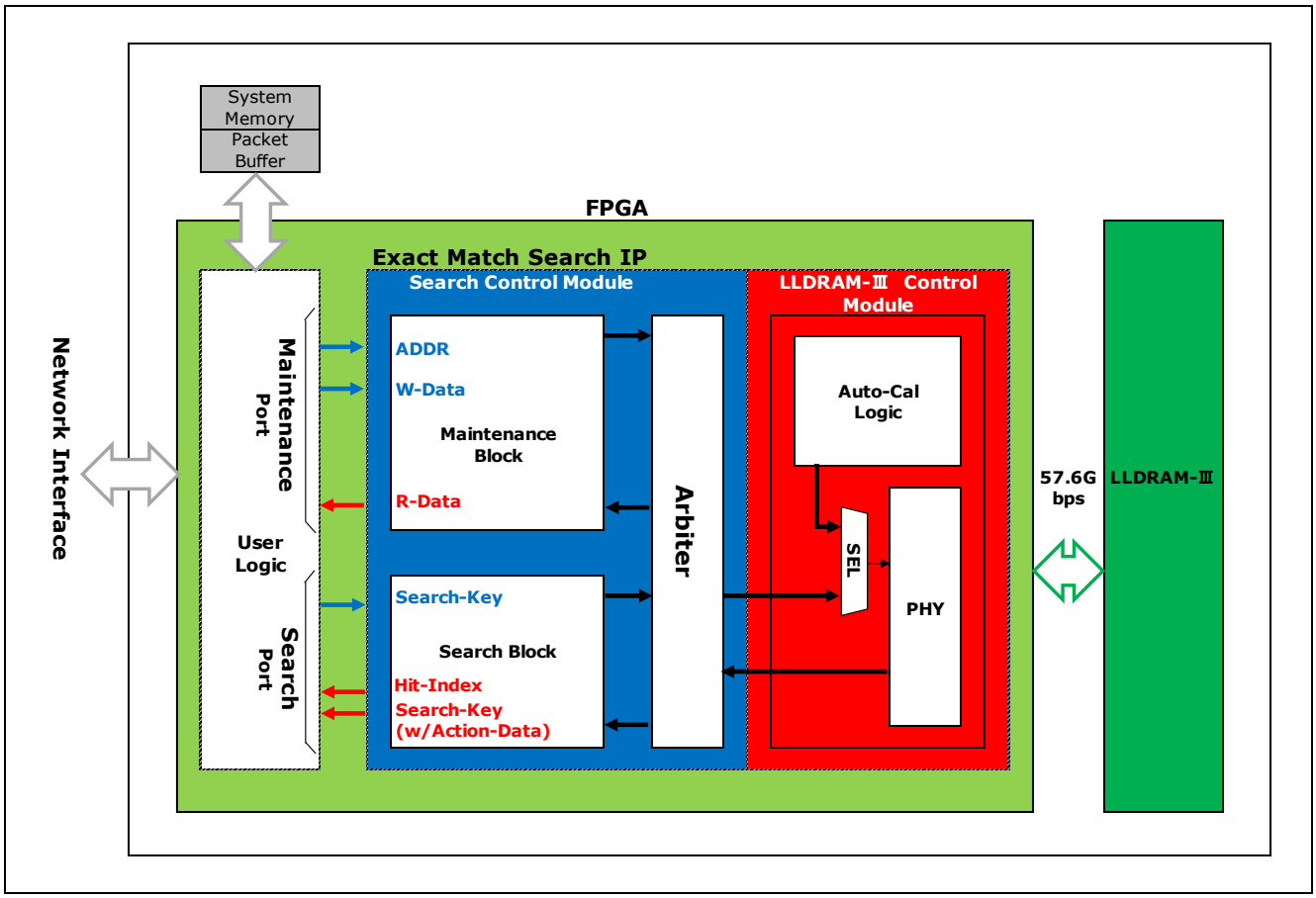


Figure 7 Exact Match Search IP Block Diagram

2. LLDRAM-Ⅲ Control IP

2.1 Memory Sub-System using LLDRAM-Ⅲ for Network System

LLDRAM-Ⅲ is a high-speed memory using 1.6Gbps DDR high-speed interface. Precise timing control is required to enable high-speed and stable data transfer between FPGA and LLDRAM-Ⅲ. LLDRAM-Ⅲ Control IP module implemented in Exact Match Search IP enables stable high-speed data transfer by auto-calibration to align Pin-skew.

LLDRAM-Ⅲ Control IP is used as User-IF IP between user-logic and LLDRAM-Ⅲ to configure memory sub-system. When LLDRAM-Ⅲ is used as packet buffer or statistic memory, network system performance will be vastly improved due to Low-Latency and High Random-Access Rate of LLDRAM-Ⅲ.

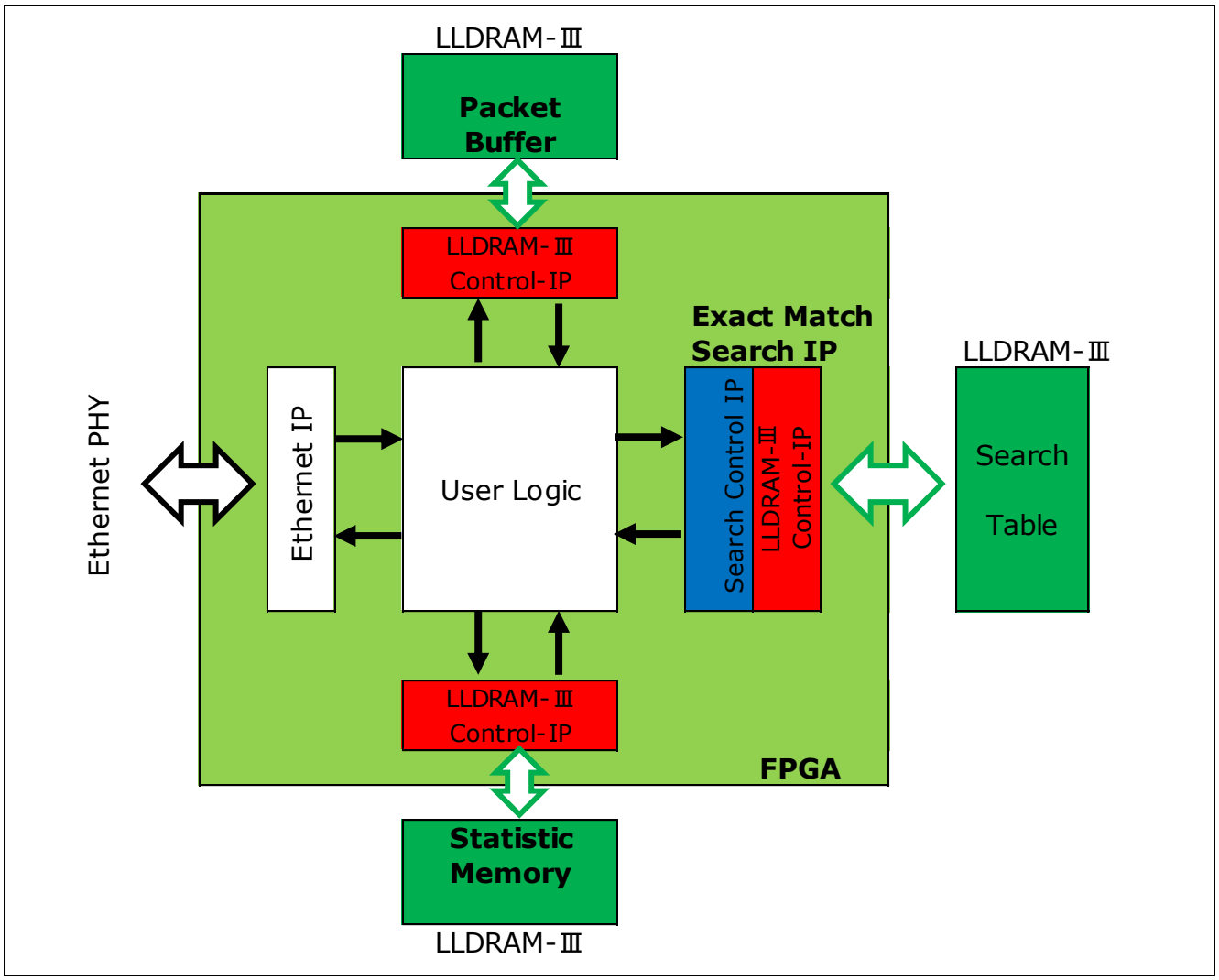


Figure 8 Example of Memory Sub-System using LLDRAM-Ⅲ for Network System

3. Development Support Tools

3.1 Reference design to execute Exact Match Search Solution

The development support tools consist of 1) a reference board with verified interoperability between the FPGA and LLDRAM-III, thereby saving time that would otherwise be needed for design and verification, 2) sample design including search IP, 3) a complete verification environment, and 4) a complete evaluation environment. These tools enable the user to begin FPGA subsystem design and network equipment design work in parallel which significantly reduces the development cycle time.

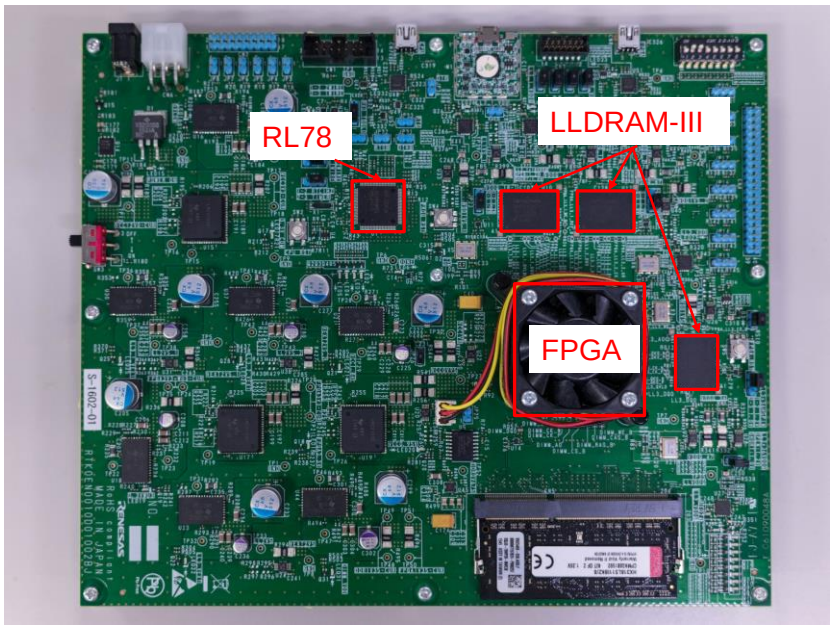


Figure 9 Reference Design Board

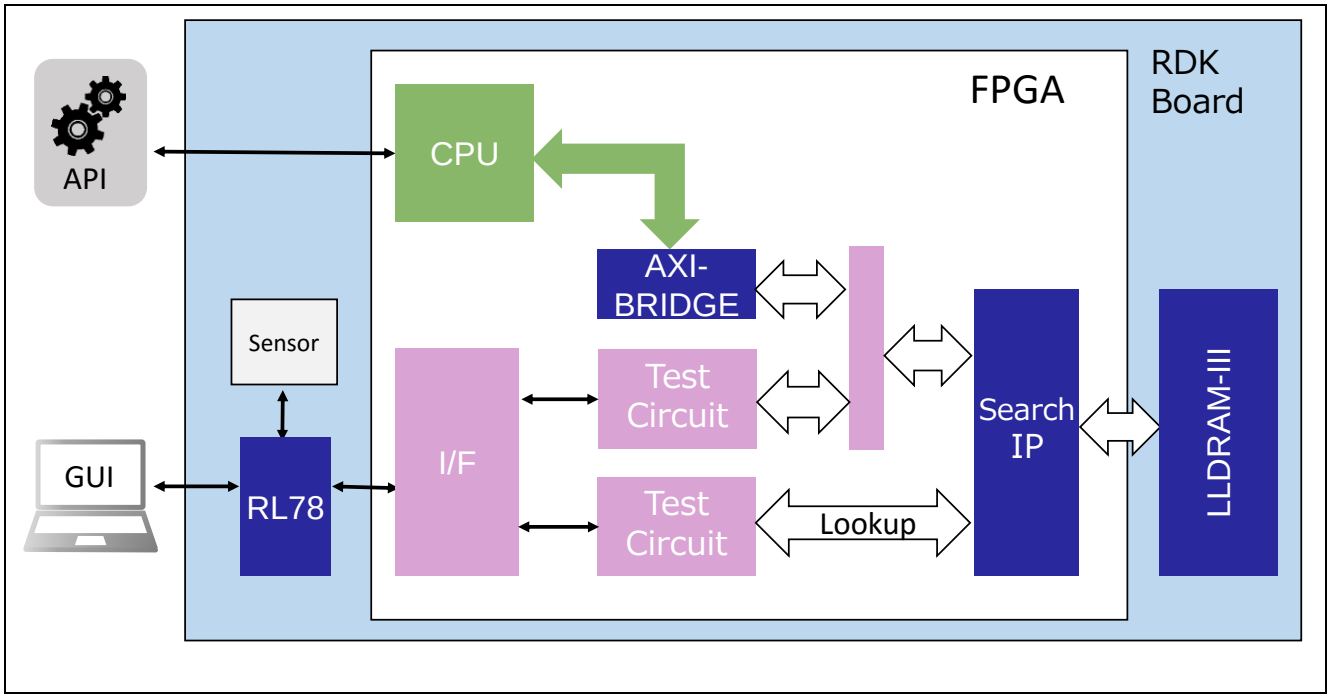


Figure 10 Reference Design Board Block Diagram

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Revision History

Rev.	Date	Description	
		Page	Summary
Rev. 1.00	2016.06.30		Rev.1.00 Issued
Rev. 2.00	2017.05.31	4	575bit/287bit search table configuration is added

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