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# High-Speed CMOS Logic IC HD74HC Series

## Precautions in System Design

In the system design, the problems to be considered are described in the following items:

### 1. Transfer Characteristics

Since the transfer characteristics of gate circuit varies with the number of working inputs, care must be taken to the noise margin. In the multiple input NOR gate, the P channel MOS is connected to $V_{CC}$ in series and the N channel MOS is connected to GND in parallel. In the NAND gate, the connection is reverse. The output voltage $V_{OUT}$ in the transition area becomes a value obtained by distributing the supply voltage at a split ratio according to the ON resistance of P channel MOS and N channel MOS. In the multiple input NOR and NAND gates, the fall of transfer characteristic, that is, $V_{IN}$ (voltage noise margin) that enters in the transition area changes according to the number of inputs as shown in Figure 1.

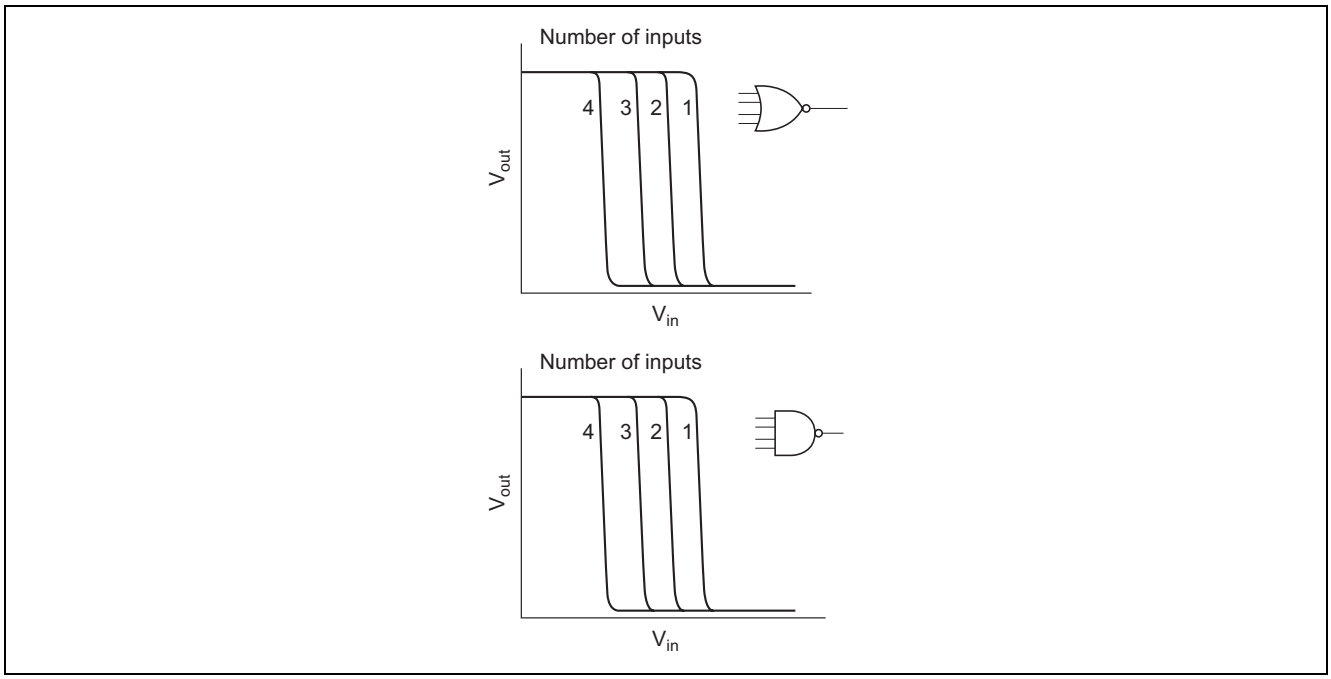


**Figure 1**

As seen from the above, it becomes clear that:

- In the NOR gate, "0" level noise margin $V_{NL}$ decreases, and "1" level noise margin $V_{NH}$ increases according to the number of working inputs.
- In the NAND gate, the noise margins are fully reversed.

### 2. Output Impedance

The output impedance of CMOS logic gate is influenced by the circuit configuration, the number of working inputs, logical state and supply voltage. There are two regions of output impedance depending on the operation:

- Constant impedance area in which P and N channel MOS' operate in the nonsaturated state.
- Constant current area in which P and N channel MOS' operate in the pinch-off state.

In designing a system including an interface circuit, the above must be considered.

### 3. Output Short-Circuit

Because no protective circuitry is provided to limit the output current, an output inadvertently shorted to $V_{CC}$ or GND on the HS-CMOS logic IC is limited to the current value determined by the pinch-off effect of the P-channel MOS and

N-channel MOS for the output. Notice that such output short-circuit current, if allowed to flow for a long time, could result in increased power dissipation or in a melted wire due to excessive current density through metallization or other performance failures. For operating stability and reliability, the maximum output current should remain within the maximum rating.

## 4. Unused Inputs

As shown in Figure 2, unused inputs must be:

(1) Directly connected to $V_{CC}$ for NAND gate circuits.
(2) Directly connected to GND for NOR gate circuits.
(3) Connected to $V_{CC}$ or GND through a proper resistor (10 kΩ or 100 kΩ.).

This is required because the extremely high input impedance of CMOS logic makes it subject to noise. This noise causes the output logic level to be unstable. Furthermore, in some cases, if a gate is not used or a flip-flop is not used, both p-channel MOS and n-channel MOS may conduct, causing $I_{CC}$ to flow.

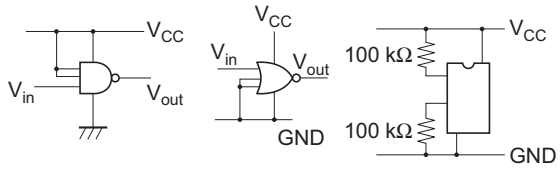


**Figure 2 Examples of Handling Unused Inputs**

## 5. Input Impedance

Since all the input protective diodes are biased reversely in the ordinary operations, the input impedance of CMOS logic IC is extremely high. When converted into a leak current, it is about several tens (pA) at a temperature of 25˚C or about one (nA) even at 100°C. Thus, the matching for operating the CMOS logic IC has only to be considered at a voltage level. In the actual interface to other IC's, however, remember that fan-out is limited according to a capacitance value because inputs measured in capacity.

## 6. Parallel Connection of Gate Circuits

If it is necessary to increase source or sinking current, the same type gate circuits can be connected in parallel as shown in Figure 3.

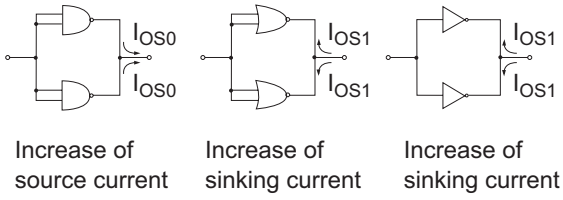


**Figure 3 Examples of Parallel Connection**

The switching speed improved at the same time. The source and sinking current capacities also increase in proportion to the number of inputs.

## 7. Wired OR Connection

The wired OR connection is unrecommendable and shall not be used in CMOS logic IC's. The reason is that if the two gate outputs are connected with A = B = 0 and C = D = 1 as shown in Figure 4, the output voltage is a value with which the supply voltage is divided by each of the resistance values of active P and N channel MOS', on an about half level ($V_{CC}$ - GND).

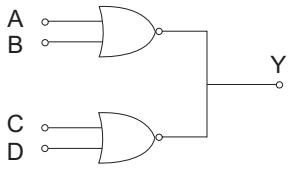


**Figure 4 Wired OR Connection**

## 8. Input Capacitance

In the CMOS logic IC, there is capacitance between the input and the GND. In addition to the major capacitance between the gate and the substrate, the capacitance of package, leads and input protection circuit are also included. The change input capacitance depending on the input voltage results mainly from the capacitance between the gate and the substrate. This input capacitance has an advantage of temporarily storing date in it by opening/closing the transmission gate. On the other hand, however, remember that the input capacitance may slow down switching speed of mutually connected gate and also may increase the power dissipation. The input capacitance is usually about 5 (pF) as specified in the standard.

## 9. Output Capacitance

The whole output capacitance of CMOS logic IC is the sum of the drain capacitance of output MOS and the external load capacitance. It may be considered that the former is about 10 (pF) per output. The propagation delay time increases linealy in proportion to the increase of external load capacitance as described previously. The power dissipation also increases according to it. Especially, be careful in attaching a large capacity of around 1 (1 μF) outside.

The peak current at the gate transition, as described previously, is limited by the output characteristics of P and N channel MOS'. In the buffer circuit, the peak current may increase (to 100 mA or more).

Pay sufficient attention to the fact that the rise of temperature in the chip may cause metal migration on the metal wiring layer. If the peak current for gate circuit is set to about 50 mA and the one for buffer circuit is set to about 100 mA, no consideration is required.

## 10. Features of 3-state Output Circuit

In a system that requires bus configuration, the 3-state output element is brought from the necessity to place unnecessary circuits in the high output impedance state through control input to operate necessary circuit selectively when tow or more circuit is connected to one bus line. Figure 5 shows the typical 3-state circuit. When the Disable input of control terminal is at "1" level, the output is at low impedance by the switch operation. When at "0" level, the output is at extremely high impedance of $10^4$ (MΩ) at a room temperature. Remember that the number of 3-state elements connectable to one bus line is limited by the switching speed and supply voltage.

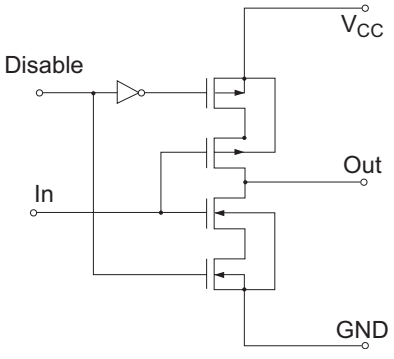


**Figure 5 3-state Output Circuit**

## 11. Static Power Dissipation

In the CMOS logic IC, the P channel MOS and N channel MOS are mutually connected each other. Therefore, either P channel or N channel is cut off in the input potential level static state. There is no path in which the current from the power supply flows. Actually, the reverse bias leak current in all the P-N junction in the chip including parasitic P-N

junction flows only. The supply current in this state is referred to as static current consumption, and the power dissipation as static power dissipation. The static current consumption is a total of leak currents, and its values are extremely small as listed in Table 1. Thus, the static current consumption is almost proportional to the supply voltage and increases exponentially in proportion to temperature.

**Table 1**

| Type | | $V_{CC}$ | Static Current Consumption $I_{CC}$(max) | |
|---|---|---|---|---|
| | | | +25°C | –40 to +85°C |
| HC series | SSI | 6.0 V | 1.0 µA | 10 µA |
| | FF | | 2.0 µA | 20 µA |
| | MSI | | 4.0 µA | 40 µA |
| HCT series | SSI | 5.5 V | 1.0 µA | 10 µA |
| | FF | | 2.0 µA | 20 µA |
| | MSI | | 4.0 µA | 40 µA |

## 12. Dynamic Power Dissipation

Assuming that the square pulse waves (tr = tf = 0) as shown in Figure 7 are applied to the input of the inverter shown in Figure 6, the output steps from “0” level to “1” level in response to the input fall from “1” level to “0” level.

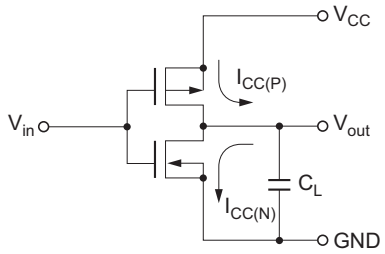


**Figure 6 Inverter circuit**

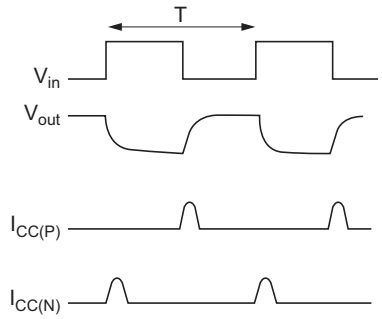


**Figure 7 Operating Voltage and current of inverter circuit**

Actually, $V_{OUT}$ is not converted into square waveforms. The reason is that the sum total $C_L$ of the outputs such as external load capacitance and drain capacitance are inverted by charging them from 0 to VCC. For charging, supply current $I_{CC(P)}$ flows through the active P channel MOS from $V_{CC}$. Contrary to this, when the input goes from “0” level to “1” level, $C_L$ discharges and $I_{CC(N)}$ flows into GND through the N channel MOS. The supply current caused by the charge/discharge is dynamic current dissipation, and the power dissipation is dynamic power dissipation. If the average power dissipation is taken as PT, it is obtained theoretically as follows:

The power dissipation when $I_{CC(P)}$ flows into the P channel MOS in Figure 6 is $I_{CC(P)}$ ($V_{CC} – V_{OUT}$). If an average is taken by the one cycle of input pulse, the average power dissipation $P_{TP}$ of P channel MOS is:

$$P_{TP} = \frac{1}{T}\int_0^T I_{CC\,(P)} \times (V_{CC} - V_{OUT})\,dt$$

$$I_{CC\,(P)} = C_L \times \frac{d\,(V_{CC} - V_{OUT})}{dt}$$

In the same manner, the average power dissipation of N channel MOS is:

$$P_{TN} = \frac{1}{T}\int_0^T I_{CC\,(N)} \times V_{OUT}\,dt$$

$$I_{CC\,(N)} = C_L \times \frac{d\,V_{OUT}}{dt}$$

Thus, the average dynamic power dissipation $P_T$ is:

$$P_T = P_{TP} + P_{TN}$$
$$= 1/T \bullet C_L \bullet V_{CC}^2$$
$$= f \bullet C_L \bullet V_{CC}^2$$

f : Input pulse frequency

It is clear that the dynamic power dissipation varies with the frequency, load capacitance and supply voltage.

Figure 8 shows the aspect.

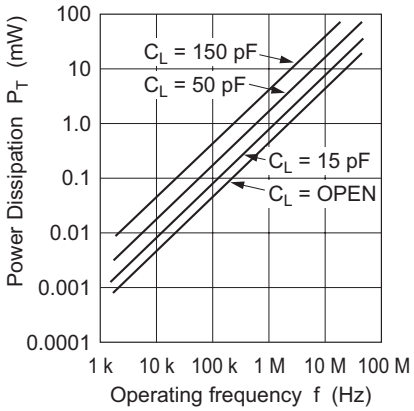


**Figure 8 Power Dissipation VS. Operating Frequency**

This relation shows a case where the square wave input with tr = tf = 0 is assumed. In an actual case, the input pulse is considered a trapezoidal waveform. Thus, remember that the transition state in which both P channel MOS and N channel MOS are simultaneously activate and DC current flows from $V_{CC}$ into GND during this time. If input is used at an intermediate level, such as crystal oscillator circuit and a linear amplifier, and if the circuits such as a differentiation circuit, an integration circuit and an oscillation circuit process gentle waveforms, pay attention to the increase of power dissipation.

## 13. Caution of Supply Voltage

To decouple noises, the capacitance of 0.01 to 0.1 (μF) should be attached externally between $V_{CC}$ and GND.

## 14. Caution of Fan-out

The number of fan-outs of CMOS logic IC is virtually unlimited in terms of DC. The reason is that the input current is the P-N junction leak current of input protection circuit at most and its value is actually approximate to 0 because the input is connected to the gate electrodes and insulated from the substrate.

Therefore, the number of fan-outs is not a problem in terms of DC. In AC, there is a slightly different circumstance. Since the input has a capacity of about 5 (pF), the output capacitance increases if the input is connected to the output. If the input capacitance is taken as 5 (pF), for example, the whole load capacitance $C_L$ (pF) at the time the number of fan-outs is n and load capacitance is $C_O$ (pF) is:

$C_L = 5 \bullet n + C_O$ (pF)

On the other hand, the propagation delay time increases in proportion to the output load capacitance $C_L$. The operating speed decreases according to the number of inputs (fan-outs) connected to the output. Therefore, remember that the number of fan-outs is fairly limited if a high-speed operation is required.

## 15. Cautions on Actual Operation

(1) The rise time and fall time of input waveforms should be 500 ns or less. Since the voltage gain is very high near the threshold, the slightest ripples on the input voltage may cause the output to produce a corresponding waveform, making the output operation unstable.

(2) The power line should be sufficiently filtered for the device. The input threshold voltage of the IC varies with the supply voltage. A ripple on the power line may change the input threshold, causing the same malfunction as noted in (1) above.

(3) Beware of a ringing (waveform distortion). Because the switching from “1” level to “0” level on vice versa is very fast, the load capacitance plus the wiring inductance may cause a ringing. Care should be taken to arrange the circuit configuration, PCB layout and wiring appropriately.

## Revision Record

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 1.00 | Jul.09.04 | — | First edition issued |
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