RAA223012

700V AC/DC Buck Regulator with Ultra-Low Standby Power

The RAA223012 is a universal input AC/DC switching buck regulator with ultra-low standby power that features a 700V integrated MOSFET capable of delivering up to 2.5W output power (Table 1). It supports output voltage as low as 3.3V.

The RAA223012 combines constant off-time control for heavy load and Pulse Frequency Modulation (PFM) for light-load operation. Constant off-time controls switching frequency above the audible frequency of approximately 50kHz. PFM eliminates any potential audible noises while offering superior light-load efficiency and ultra-low power consumption (<10mW at no load). Efficiency is achieved up to 75%. The built-in frequency dithering further reduces the EMI noise spectrum.

The RAA223012 also features input brownout protection that prevents input circuitry from the overcurrent at low input voltage, and hiccup protections for output fault conditions such as short-circuit, overload, and open feedback.

The RAA223012 is available in a small 5 Ld TSOT23 and 8 Ld SOIC packages.

Table 1. Maximum Output Current (Max. Ambient 85°C)

V_{OUT} (V)	$120V_{AC}$	$230V_{AC}$	$85V_{AC}$~$265V_{AC}$
24	100mA	100mA	100mA
12	140mA	140mA	140mA
5	185mA	195mA	170mA
3.3	190mA	190mA	190mA

Features

- Ultra low standby power (<10mW)
- No audible noise
- Low quiescent current (<100µA)
- Output voltage as low as 3.3V
- Low EMI with frequency dithering
- 5 Ld TSOT23 and 8 Ld SOIC package options
- Programmable PFM allows optimization of C_{OUT} for various standby power requirements
- Protection features: Short-Circuit Protection (SCP), Overload Protection (OLP), Open Feedback Protection, and Over-Temperature Protection (OTP).

Applications

- Home appliances
- Home automation, IoT, and sensors
- Metering and Industry control
- Bias power

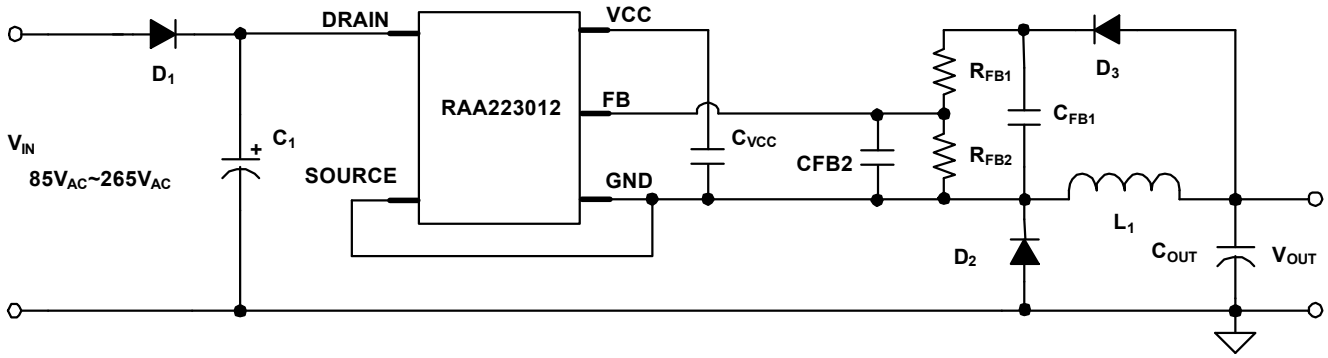


Figure 1. Typical RAA223012 Buck Application Circuit

Contents

1. Overview

1.1 Block Diagram

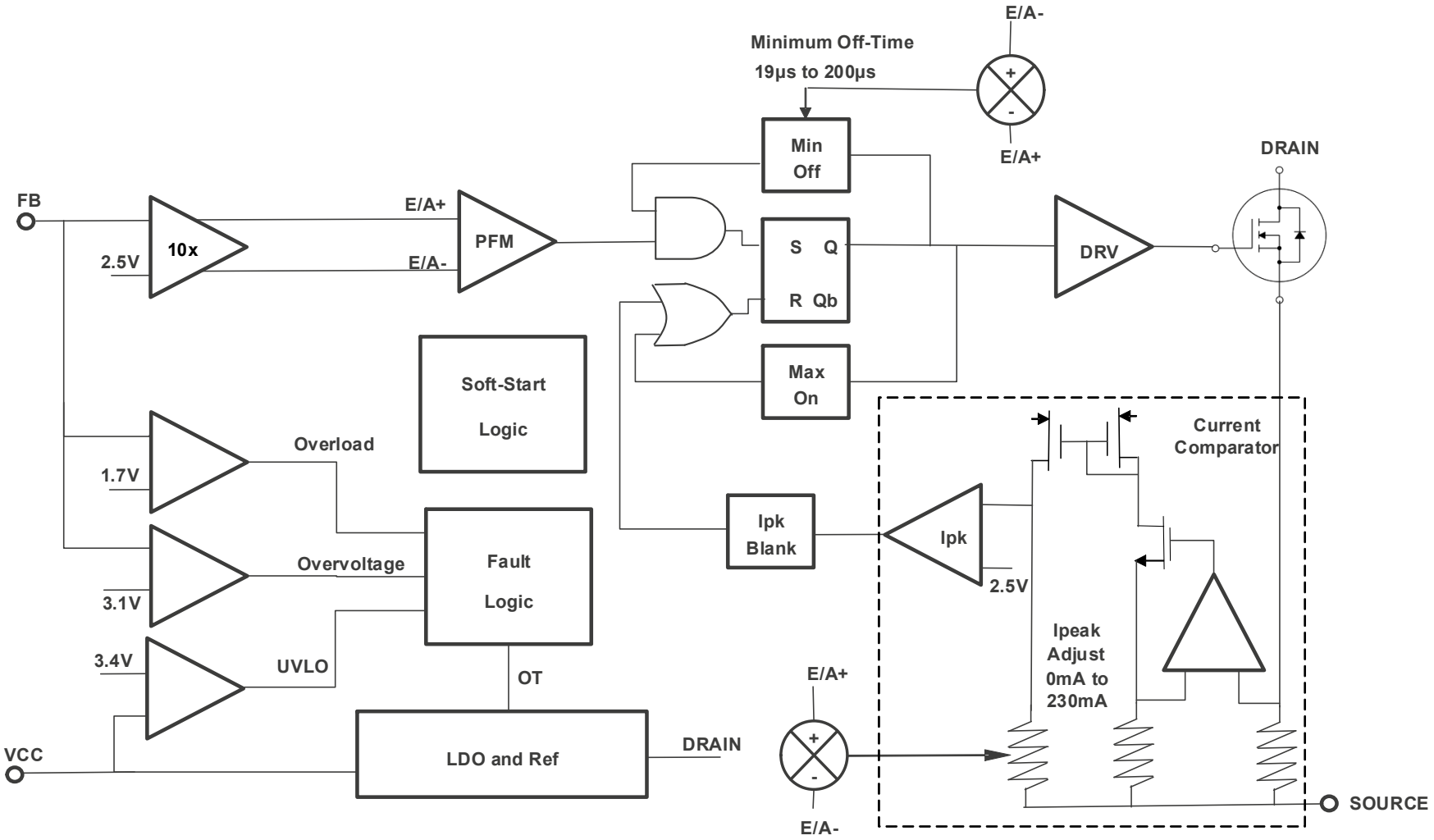
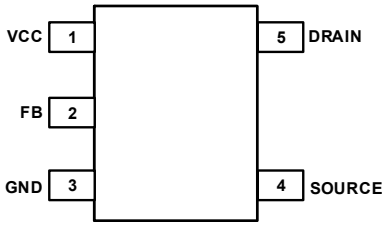


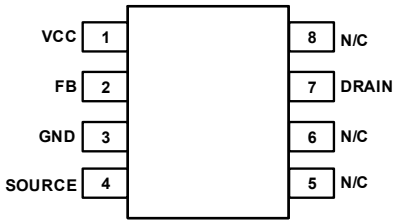
Figure 2. Block Diagram of RAA223012

2. Pin Information

2.1 Pin Assigments



5 Ld TSOT23
Top View



8 Ld SOIC
Top View

2.2 Pin Descriptions

Pin Number		Pin Name	Description
5 Ld TSOT23	8 Ld SOIC		
1	1	VCC	IC supply voltage
2	2	FB	Feedback pin, 2.5V ±4%
3	3	GND	IC ground, externally connected to the SOURCE pin
4	4	SOURCE	Internal power MOSFET source
5	7	DRAIN	Internal power MOSFET drain
	5, 6, 8	N/C	Not connected

3. Specifications

3.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty..

Parameter	Minimum	Maximum	Unit
VCC	-0.3	+6.5	V
VFB	-0.3	+6.5	V
DRAIN (to SOURCE)	- 0.3	700	V
Continuous Power Dissipation (T_A = +25°C)		1	W
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per JS-001-2017)	1.2		kV
Charged Device Model (Tested per JS-002-2014)	1		kV
Latch-Up (Tested per JESD78E; Class 2, Level A)	100		mA

3.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)[1]	θ_{JC} (°C/W)[2]
5 Ld TSOT23	80	71
8 Ld SOIC	86	57

1. θ_{JA} is measured on single layer 1oz evaluation PCB with 218mm^2 thermal copper connected to the SOURCE and DRAIN pins, in free air.
2. For θ_{JC}, the case temperature location is taken at the package top center.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature		+150	°C
Maximum Storage Temperature Range	-60	+150	°C
Pb-Free Reflow Profile	See TB493		

3.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Supply Voltage, V_{DRAIN}		375	V
Ambient Temperature	-40	+85	°C
Output Voltage	3.3		V

3.4 Electrical Specifications

Typical operating conditions at 25°C, V_{DRAIN} = 100V, V_{CC} = 5.6V, T_J = -40 to +125°C, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Startup and Power FET						
Internal V_{CC} Startup Current	I_{VCC_START}	V_{CC} = 4V,		1.6		mA
Drain Leakage Current	I_{D_LEAK}	V_{CC} = 0V, V_{DRAIN} = 375V, V_{FB} = 2.6V		1		µA
I_{DRAIN} Bias	I_{D_BIAS}	V_{CC} = 5.9V, V_{DRAIN} = 375V			5	µA
Power FET Breakdown Voltage	$V_{DS(BR)}$	T_J = 25°C	700			V
Power FET On-Resistance	$r_{DS(ON)}$	T_J = 25°C, V_{CC} = 5.8V, I_{DS} = 200mA		14.5	17	Ω
		T_J = 125°C		25	30	Ω
V_{CC} Supply						
V_{CC} Start (Rising)	V_{CC_START}		5.5	5.9	6.3	V
V_{CC} when Internal Regulator Off	V_{CC_OFF}		5.5	5.9	6.3	V
V_{CC} (Falling) Regulator On at Startup	V_{CC_ON}		5.2	5.55	5.9	V
Internal V_{CC} On/Off Hysteresis	V_{CC_HYS}		0.3	0.35	0.45	V
V_{CC} (Fallng) Regulator On after Startup	$V_{CC\_ON\_SS}$		4.25	4.5	4.8	V
V_{CC} Undervoltage Threshold (Falling)	V_{CC_UVLO}	IC stop switching	3.15	3.4	3.55	V
V_{CC} Shunt Regulator On (Rise)	V_{CC_SON}	External V_{CC} supply, internal shunt on		6.15	6.5	V
V_{CC} Shunt Regulator Off (Fall)	V_{CC_SOFF}			6.1	6.4	V

Typical operating conditions at 25°C, V_{DRAIN} = 100V, V_{CC} = 5.6V, T_J = -40 to +125°C, unless otherwise specified. **(Cont.)**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
V_{CC} Quiescent Current	I_{VCC_Q}	V_{FB} > 2.5V, no switching, V_{CC} = 5.6V		70	103	µA
V_{CC} Current During Switching	I_{VCC}	V_{FB} < 2.5V, switching frequency = 50kHz, D = 0.15, V_{CC} = V_{CC_ON} +0.1V		130	200	µA
V_{CC} Discharging Current Hiccup Timing	I_{QVCC3}	V_{CC} discharge current for timing of fault hiccup delay		19	30	µA
Current Sense						
Peak Current Limit	I_{PK}	V_{FB} < 2.5V, di/dt = 0.5A/µs, V_{CC} = 5.8V	260	335	400	mA
SCP Threshold	I_{SC_TH}			710		mA
Minimum Peak Current	I_{PKMIN}	di/di = 0.5A/µs, V_{CC} = 5.8V		150		mA
Leading Edge Blank Time	t_{LEB}		192	230		ns
Feedback						
Feedback Voltage	V_{FB}		2.4	2.5	2.63	V
Transconductance	GM	I_{PK} GM, V_{CC} = 5.8V		7		mS
Feedback Undervoltage Threshold	V_{FBUV}	V_{CC} = 5.7V	1.6	1.7	1.8	V
Feedback Threshold for Increased Off-Time	$V_{FB\_TOFFMIN}$	V_{CC} = 5.0V	0.67	0.84	0.98	V
Feedback Overvoltage	V_{FBOV}		2.75	3	3.3	V
Timing						
Minimum Off-Time	t_{OFF_MIN}	V_{CC} = 5.0V	15	19	24	µs
Maximum On-Time	t_{ON_MIN}	V_{CC} = 5.0V	12	15	18	µs
Minimum Off-Time in Short-Circuit	t_{OFFMIN_SC}	V_{CC} = 5.0V		200		µs
Hiccup Restart Delay	t_{HICC}	C_{VCC} = 1µF		100		ms
Startup Blanking Time, OLP Time	t_{OLP}	f_{SW} = 50kHz, V_{FB} < 1.7V, V_{CC} = 5.0V		1024		cycle
Thermal						
Over-Temperature Threshold	OTP_{TH}			150		°C
Over-Temperature Hysteresis	OTP_{HYS}			30		°C

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

4. Typical Characterization Graphs

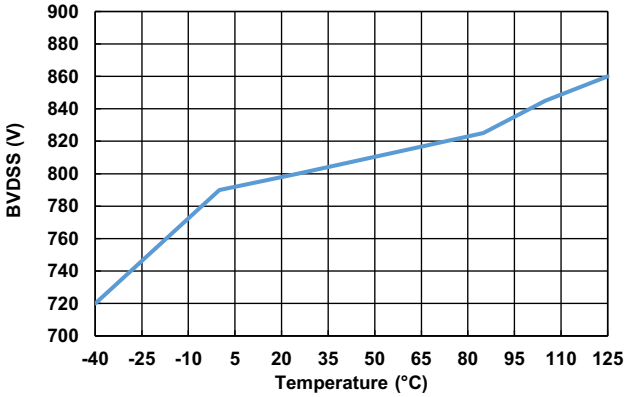


Figure 3. Breakdown Voltage vs Temperature

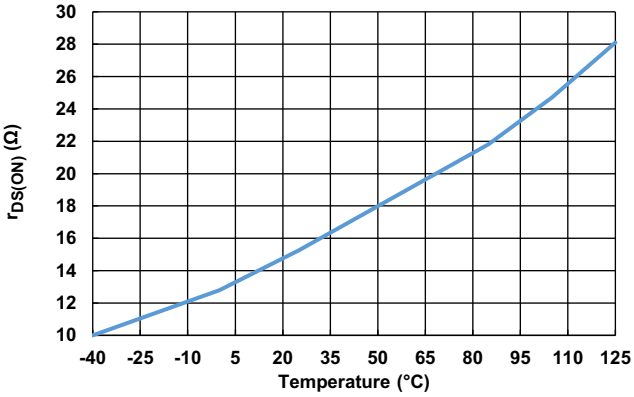


Figure 4. On-Resistance vs Temperature

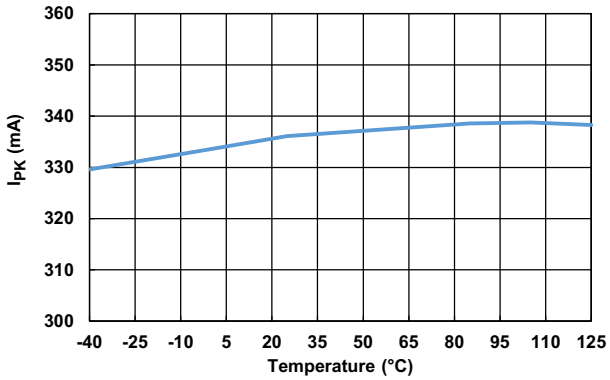


Figure 5. Peak Current Limit vs Temperature

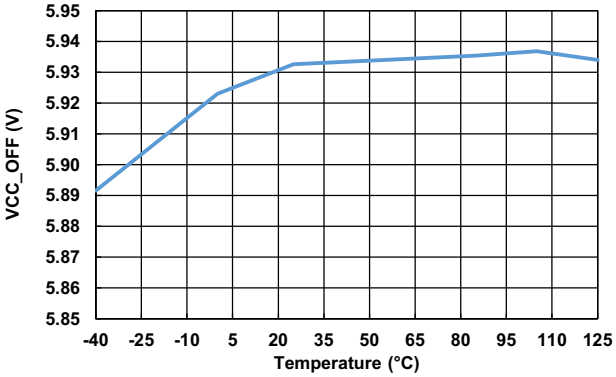


Figure 6. V_{CC} Start/Upper Limit vs Temperature

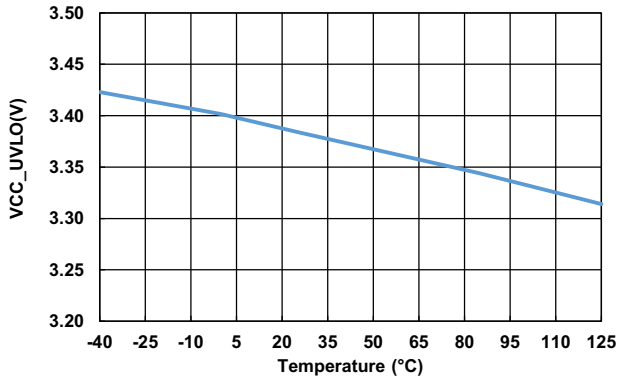


Figure 7. V_{CC} Undervoltage Threshold vs Temperature

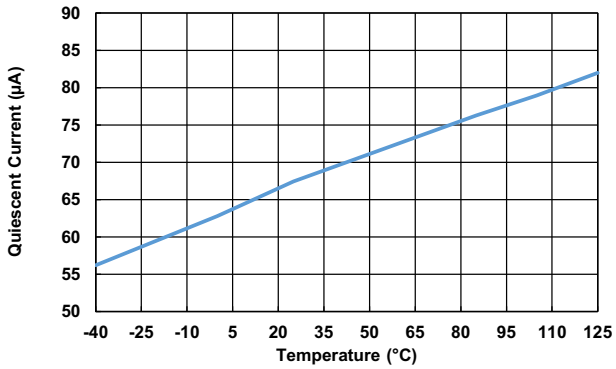


Figure 8. IC Quiescent Current vs temperature

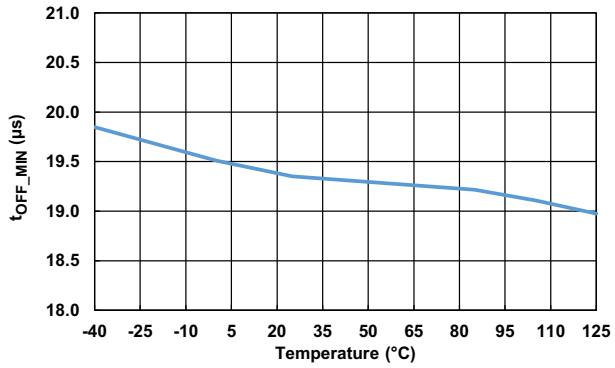


Figure 9. Minimum Off-Time vs Temperature

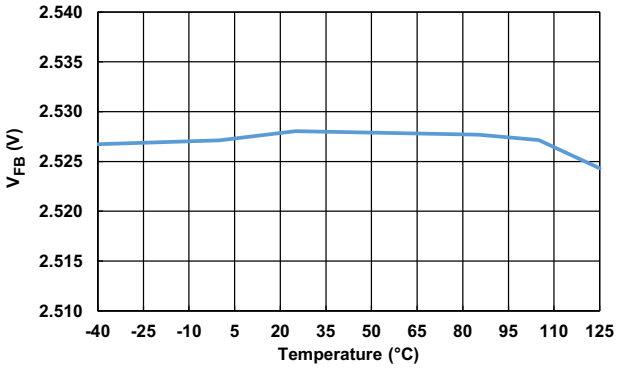


Figure 10. Feedback Voltage vs Temperature

V_{IN} = 230V_{AC}, V_{OUT} = 6.5V, I_{OUT} = 100mA, L = 680µH, Co = 100µF, T_A = 25°C)

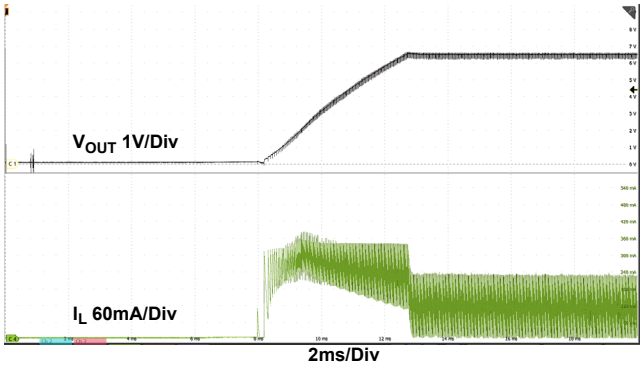


Figure 11. Startup

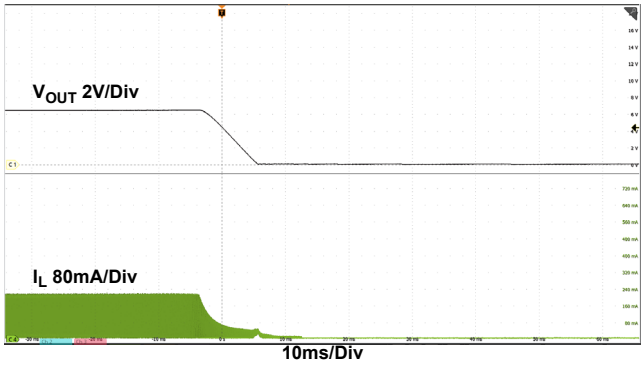


Figure 12. Shutdown

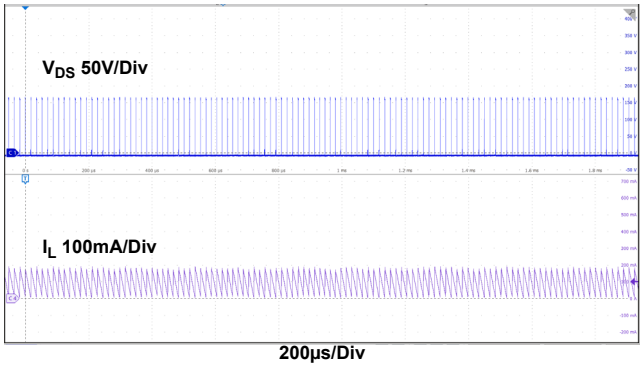


Figure 13. Full Load Operation

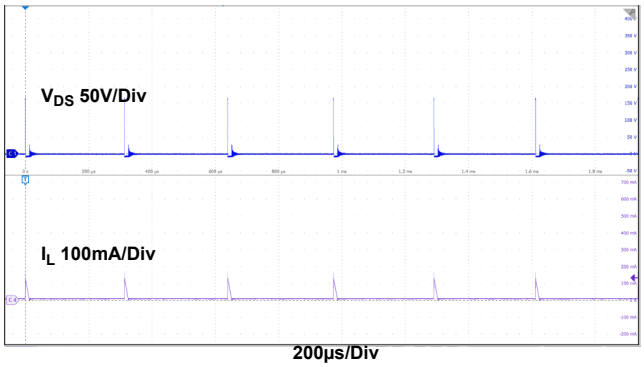


Figure 14. Light-Load Operation

V_{IN} = 230V_{AC}, V_{OUT} = 6.5V, I_{OUT} = 100mA, L = 680µH, Co = 100µF, T_A = 25°C) (Cont.)

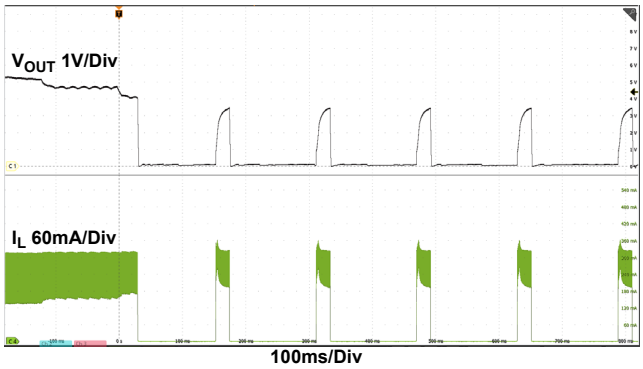


Figure 15. Overload protection

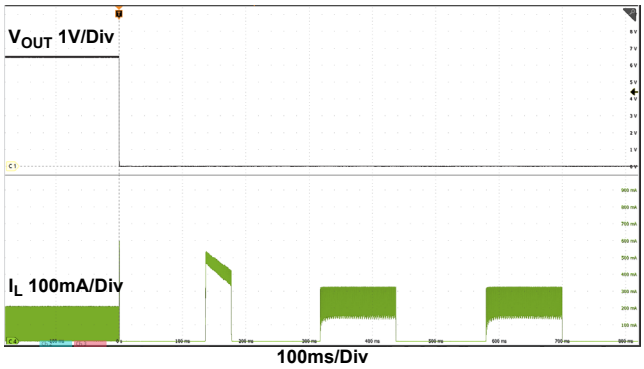


Figure 16. Short-Circuit Protection

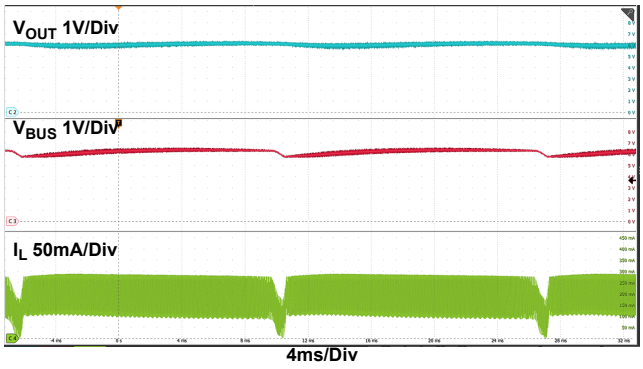


Figure 17. Input Brownout Protection

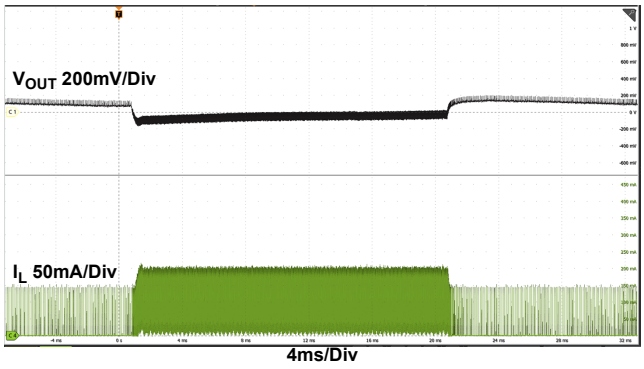


Figure 18. Load Transient (10mA to 100mA)

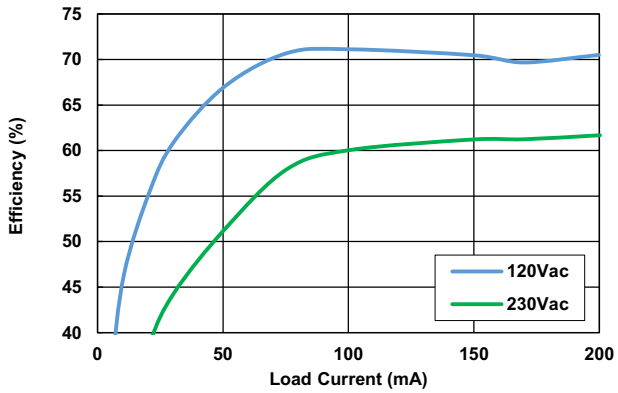


Figure 19. Efficiency (V_{OUT} = 6.5V)

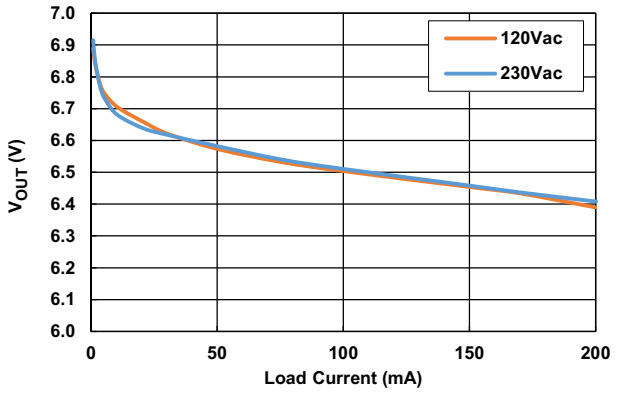


Figure 20. Load Regulation (V_{OUT} = 6.5V)

5. Detailed Description

The RAA223012 adopts the high-side float switching topology as Figure 1 shows. A floating VCC supplies IC operation. The output voltage is sensed on the FB pin from an RC sampling network connected to the output, and compared with the internal reference through an error amplifier that controls the peak current accordingly.

5.1 Constant Off-Time Mode

In heavy load, the power FET is turned on after a constant off-time. Because the on-time is comparably much smaller than the off-time, the IC operates with quasi-constant frequency. When the load current goes lower, the peak current becomes lower while still switching around 50kHz until it hits the minimum peak current limit. Because the switching frequency is always kept around 50kHz in the operation, no audible noises can be heard.

5.2 PFM Mode

When the load current decreases below a certain value (see, the peak current is kept at the minimum level, while the off-time is gradually increased to maintain the output regulation. As a result, the frequency reduces. The IC goes into Pulse Frequency Modulation (PFM) operation, as Figure 21 shows, so losses are reduced due to switching frequency reduction. During this mode, while the switching frequency is reduced below 1kHz at no load, the audible noise is minimized by keeping the peak current at the minimum level. In the meantime, due to the low IC biasing current and small peak current, the standby power can be achieved below 10mW. The above operation is illustrated in Figure 22 and Figure 23.

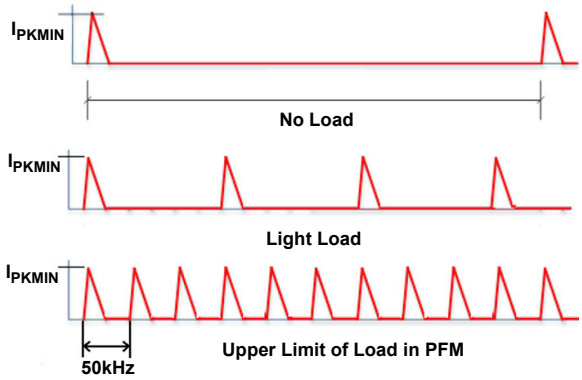


Figure 21. PFM Operation in Light Load

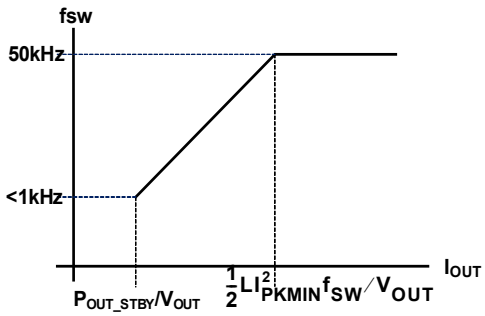


Figure 22. Switching Frequency vs I_{OUT}

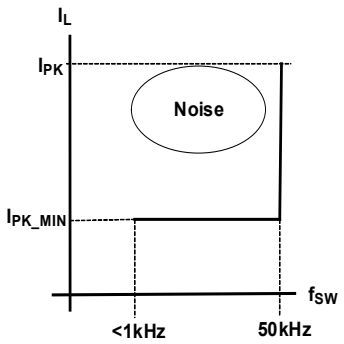


Figure 23. Peak Current vs Switching Current

5.3 Output Voltage Sampling

The RC sampling network samples the output voltage through a forward biased D3 when D2 is free-wheeling. When the D2 cathode goes high and D2 stops conducting current, the sampled voltage across C_{FB1} is discharged by R_{FB1} and R_{FB2}. In constant off-time operation, the FB pin voltage is slightly below the internal reference. The power FET is set on after a constant off-time. In PFM mode, when the sampled voltage on FB pin drops to internal

reference, the power FET is clocked on. In this way, the light-load switching is set by the C_{FB1}, R_{FB1}, and R_{FB2} for the corresponding load. Therefore, the required no-load standby power is achieved by choosing C_{FB1}, allowing you the flexibility to design your circuit for various standby power requirements. For detailed design guidance, see Feedback Capacitor (C_{FB1}) Selection.

5.4 Soft Start-Up

The RAA223012 starts up with the V_{CC} capacitor charged by an internal HV current source. When the V_{CC} reaches up to 5.9V, the IC begins switching, the internal HV current source is turned off, and a start-up timer begins. When V_{CC} drops below 5.5V, the HV current source is on again, which is determined by the actual IC supply current. During the start-up, the output voltage ramps up gradually, which is controlled by a variable off-time set by the feedback voltage. After the timer expires (start-up is finished), the HV current source is on again only when V_{CC} drops to 4.5V. When V_{OUT} is established, V_{CC} can be supplied by V_{OUT} (optional) to save power consumption for high efficiency and low standby power, see Figure 24.

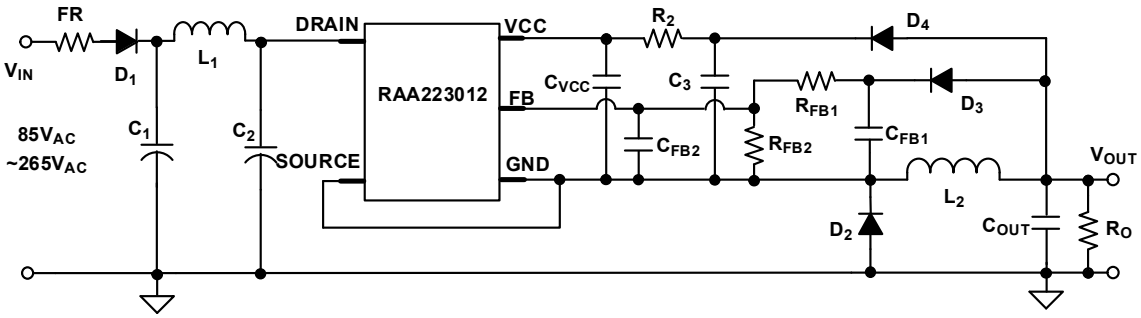


Figure 24. RAA223012 Low Standby Power Buck Regulator

Figure 25 shows the start-up diagram.

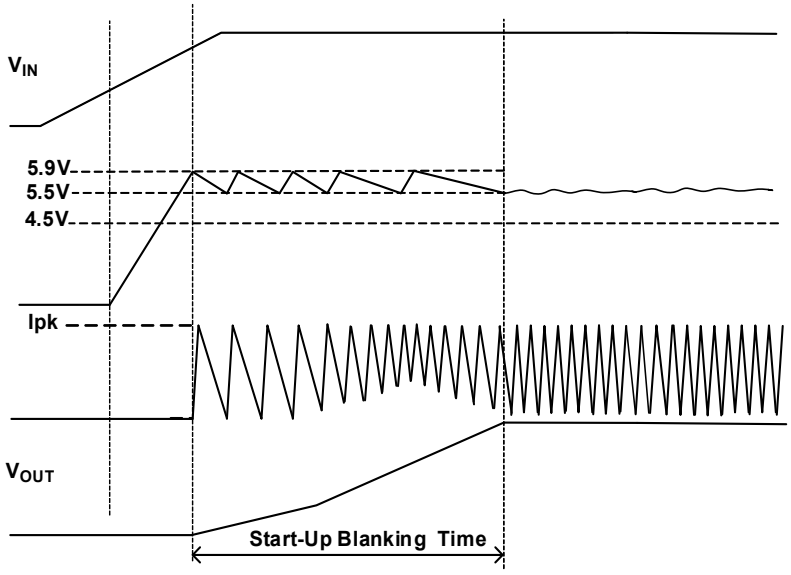


Figure 25. RAA223012 Start-Up Diagram

5.5 Overload Protection

With the fixed minimum off-time (when $V_{FB} \geq 0.84V$), the maximum load current that the RAA223012 allows is limited for a given output voltage and inductor, and therefore, is the maximum output power (<5W). However, when the output voltage continues to drop during the overload, the FET power losses increase and can cause potential IC overheating. Therefore, when V_{FB} reaches 1.7V an internal comparator is triggered and starts an Overload Protection (OLP) timer. When the timer is expired, the overload situation is identified, and the IC is shut off. V_{CC} is discharged by a 19µA internal current source to 3.4V, and charged up to 5.9V to resume switching (the interval without switching is the hiccup time). The overload protection time sequence is shown in Figure 26.

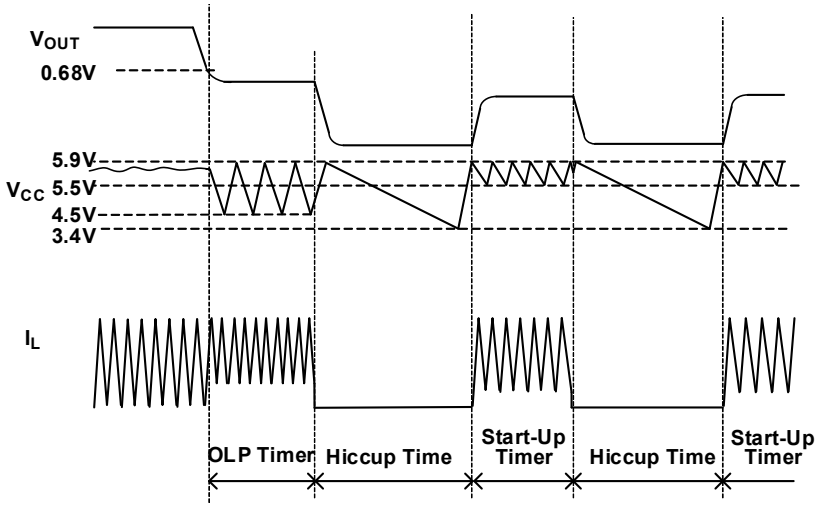


Figure 26. RAA223012 Overload Protection Diagram

5.6 Short-Circuit Protection

When the output is shorted, $V_{OUT} = 0$, V_{FB} drops to zero because of the feedback network, introducing a delay. Before V_{FB} drops to $V_{FB\_TOFFMIN}$, the RAA223012 operates with T_{ONMAX} and T_{OFFMIN}, which quickly builds up a high current ($>I_{PK}$) because the inductor peak current does not get reset. When the current reaches I_{SC_TH}, a timer is started. If the inductor current reaches I_{SC_TH} for four consecutive cycles, the RAA223012 determines that a short-circuit is present and immediately shuts off switching. The IC then quickly charges V_{CC} up to 5.9V and discharges it with a 19µA current source to 3.4V. When V_{CC} drops to 3.4V, a 1.6mA current source charges V_{CC} back to 5.9V where the IC resumes switching.

When the RAA223012 resumes switching, assuming V_{FB} drops to zero, the IC operates with the increased T_{OFFMIN_MAX} so the inductor current can fully reset below the maximum peak limit. The RAA223012 operates in CCM with the inductor peak current being limited at I_{PK}, with an average current around 240mA during the short. The part remains in hiccup mode until the short is removed. When the short is removed, V_{OUT} returns to normal. This procedure is shown in Figure 27.

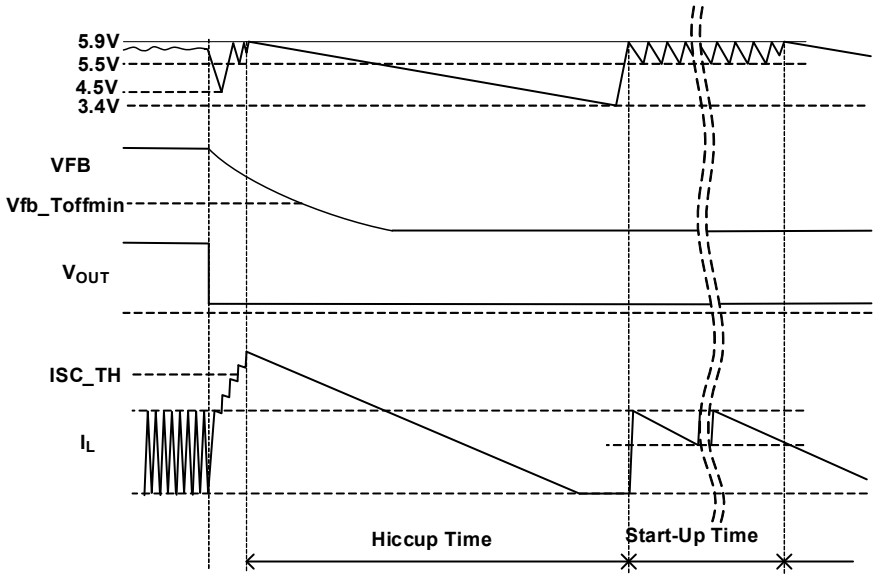


Figure 27. RAA223012 Short-Circuit Protection Diagram

6. Application Topologies

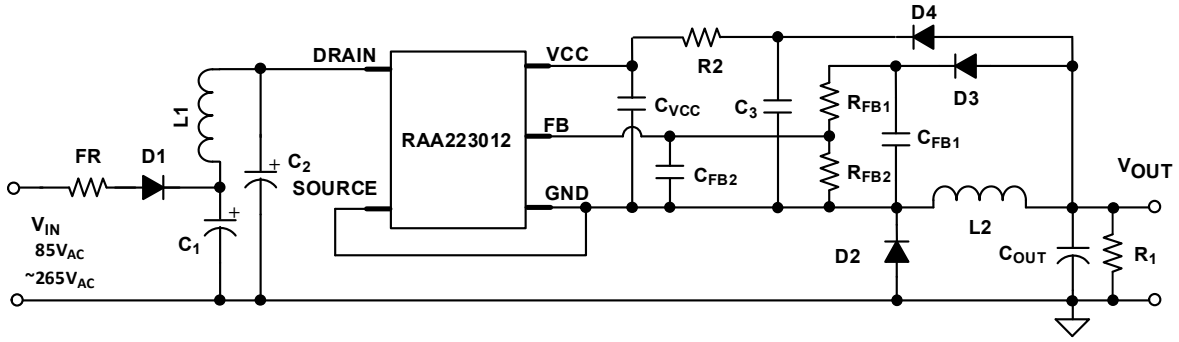


Figure 28. RAA223012 Buck with Enhanced Efficiency and Low Standby Power

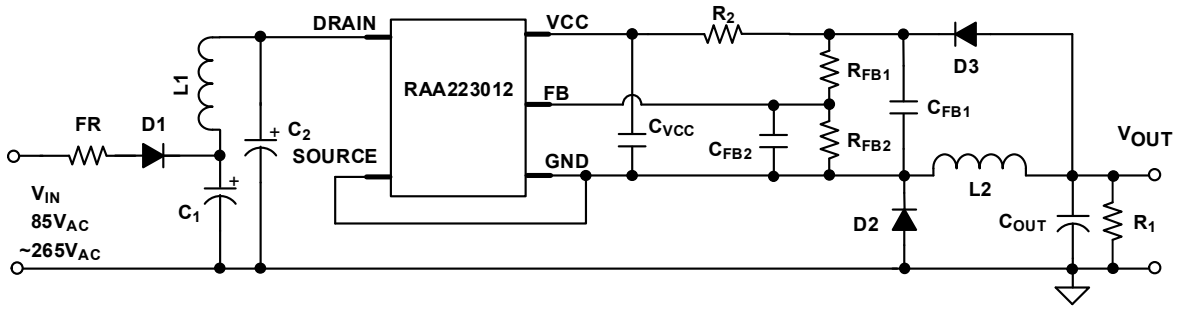


Figure 29. RAA223012 Buck with Enhanced Efficiency

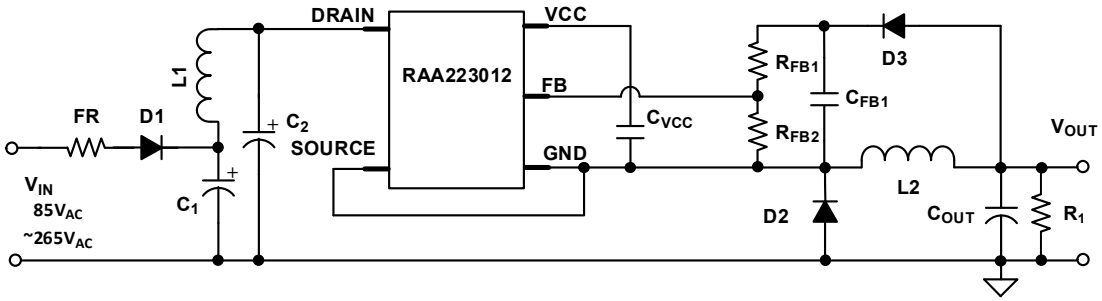


Figure 30. RAA223012 Buck with Low BOM Cost

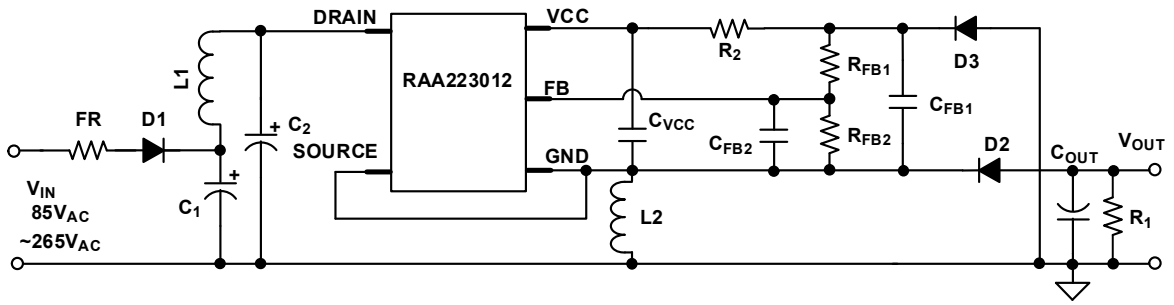


Figure 31. RAA223012 Buck/Boost

7. Design Guidance

7.1 Feedback Resistor Selection

The output voltage is set by the resistor divider of R_{FB1} and R_{FB2}. Because of the diode forward voltage mismatch between the feedback diode D3 and free-wheeling diode D2, an additional 0.4 offset is added in Equation 1 to calculate the resistor values of R_{FB1} and R_{FB2}.

(EQ. 1) $$\frac{R_{FB1}}{R_{FB2}} = \frac{V_{OUT} + 0.4}{V_{FB}} - 1$$

7.2 Output Inductor Selection

Because the buck regulator is designed with a constant off-time of 19µs at full load, design the output inductor according to Equation 2:

(EQ. 2) $$L \geq \frac{V_{OUT} T_{OFFMIN}}{2(I_{PK} - I_{O\_MAX})}$$

For example, if V_{OUT} = 6.5V, if I_{O_MAX} = 150mA, $L \geq \frac{6.5 \times 19 \times 10^{-6}}{2 \times (0.335 - 0.15)} = 333\mu H$ L is chosen with a fixed value 470µH.

7.3 Feedback Capacitor (C_{FB1}) Selection

The feedback capacitor, C_{FB1}, determines the pulse frequency at no load condition. The corresponding inductor current is shown in Figure 32.

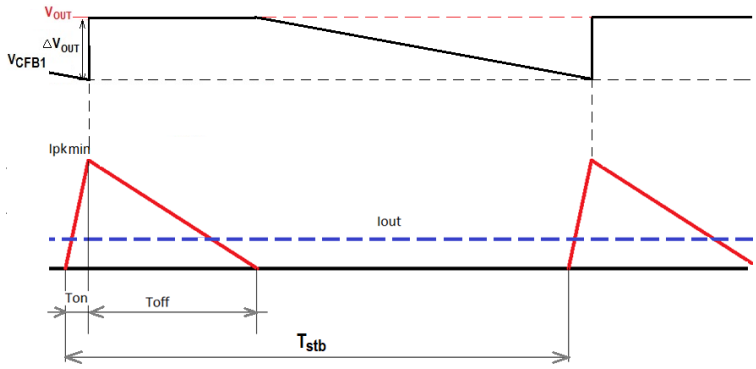


Figure 32. The Inductor Current at No Load Operation

The average output current is written as Equation 3.

(EQ. 3) $$I_{OUT\_MIN} = \frac{I_{PK\_MIN}(T_{ON} + T_{OFF})}{2T_{stb}}$$

Because $T_{ON} << T_{OFF}$, I_{OUT_MIN} can be written as:

$$\frac{I_{PK\_MIN}T_{OFF}}{2T_{stb}} = I_{OUT\_MIN} \quad \text{, where } T_{OFF} = \frac{LI_{PK\_MIN}}{V_{OUT}}$$

Therefore:

(EQ. 4) $$I_{OUT\_MIN} = \frac{L(I_{PK\_MIN})^2}{2V_{OUT}T_{stb}}$$

To have the required input standby power, P_{IN_STBY}, the power delivered to the output should satisfy Equation 5:

(EQ. 5) $$V_{OUT}I_{OUT\_MIN} = P_{IN\_STBY}\eta$$

where η is the light-load efficiency.

Replacing I_{OUTMIN} with Equation 4 gives you Equation 6:

(EQ. 6) $$V_{OUT}\left(\frac{L(I_{PK\_MIN})^2}{2V_{OUT}T_{stb}}\right) = P_{IN\_STBY}\eta$$

The required time interval T is calculated using Equation 7:

(EQ. 7) $$T_{stb} = \frac{L(I_{PK\_MIN})^2}{2P_{IN\_STBY}\eta}$$

Because the time interval T_{stb} is primarily determined by the sampling network discharging time, it is related to C_{FB1} in Equation 8:

(EQ. 8) $$C_{FB1} = \frac{V_{OUT}T_{stb}}{\Delta V_{OUT}(R_{FB1}+R_{FB2})}$$

where ΔV_{OUT} is the output voltage increase above the nominal V_{OUT} at no load.

From Equation 8, it can be seen that a bigger sampling capacitor leads to a smaller ΔV_{OUT}, but C_{FB1} can not be too big as it calls for a huge C_{OUT}. A small ΔV_{OUT} can cause erratic logic function of the internal PFM comparator in mode transition. Therefore, choose ΔV_{OUT} properly according to the highest V_{OUT} allowed in the applications. When ΔV_{OUT} is picked, C_{FB1} is calculated using Equation 8.

7.4 Output Capacitor Selection

The output capacitor does not only need to meet the requirement of output ripple voltage and load transient response, but also needs to ensure the slew rate of the output voltage is slower than the discharging rate of the

sampling capacitor, C_{FB1}, in a defined step load transient, as shown in the Figure 33. Therefore, C_{OUT} is first calculated according to V_{OUT} discharging by Equation 9.

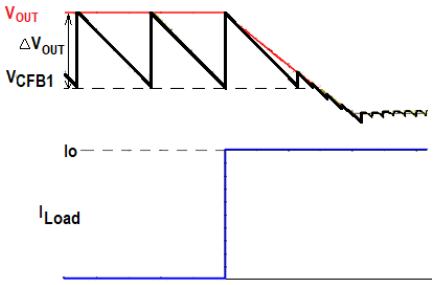


Figure 33. Output Capacitor Discharging at Step Load

(EQ. 9) $$C_{OUT} \geq \frac{C_{FB1}\Delta I_{OUT}(R_{FB1}+R_{FB2})}{V_{OUT}}$$

(EQ. 10) $$C_{OUT} \geq \frac{\Delta I_{OUT} T}{0.07 V_{OUT}}$$

where 7% voltage drop is used in this example.

7.5 Dummy Resistor Selection

At no load condition, the system standby power is determined by the IC quiescent current and the feedback resistor bleeding current. If the required standby power is not low, a dummy resistor can be added in parallel with the output capacitor to keep a no-load output voltage from getting too high. Its value is calculated using Equation 11.

(EQ. 11) $$R_O = \frac{V_{OUT}}{\left(\frac{P_{IN_{STBY}}\eta}{V_{OUT}} - I_q - \frac{VFB}{RFB2}\right)}, \text{where } \eta = 0.4$$

7.6 Power Capability

The maximum power the RAA223012 can deliver depends on the ambient temperature, output voltage, input voltage, and even PCB thermal design. In general, higher input voltage with lower ambient temperature allows a bit more power than low input voltage at higher ambient temperature. Also, it delivers more power at higher output voltage. Table 1 summarizes the maximum power the RAA223012 can deliver with ambient temperature up to 85°C. This table should be used as a reference and may vary because of the actual PCB thermal design.

7.7 PCB Layout Guidance

Proper layout is important to ensure a stable operation, good thermal behavior, EMI performance, and reliable operation for various operating environments. Pay attention to the following layout recommendations:

- Leave proper spacing between high voltage (maximum 400V) traces and low voltage traces (minimum1.4mm)
- Keep a small loop from the input filter capacitor to the IC, switching inductor, output capacitor, and to the ground of the input capacitor, and a small loop consisting of a switching inductor, output capacitor, and free-wheeling diode.
- Keep sufficient copper area on the IC drain and/or source pin (not less than 140mm^2 for 2W to 3W output power) for better thermal performance

- Keep the switching inductor away from the input EMI inductor to avoid noise coupling, especially when an unshielded switching inductor is used.
- Place the V_{CC} decoupling capacitor and FB pin decoupling capacitor close to the pins.

The PCB layout example is shown in Figure 34.

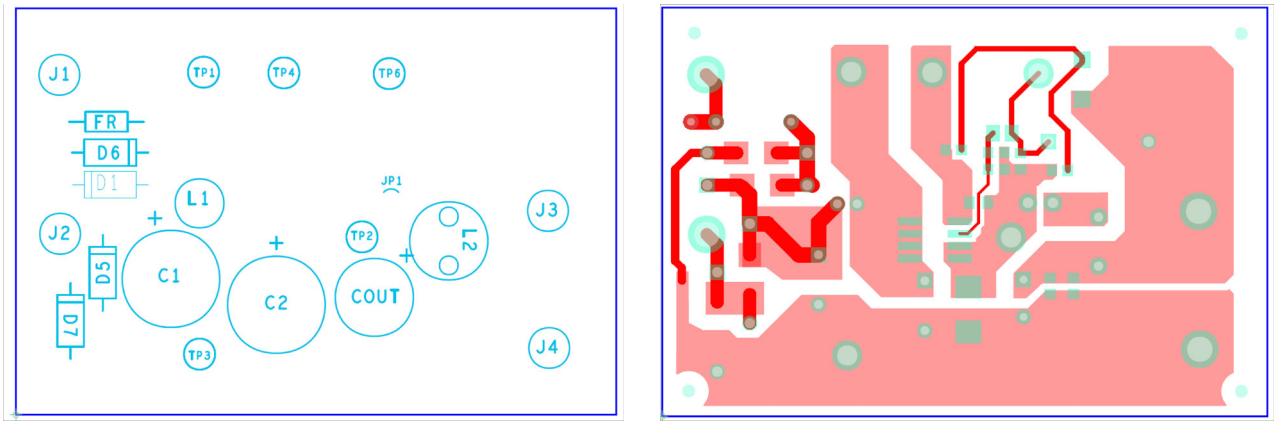


Figure 34. Example PCB Layout

8. EMI Performance

Conducted and Radiated EMI compliance for EN55022/CISPR22 (5V/150mA output)

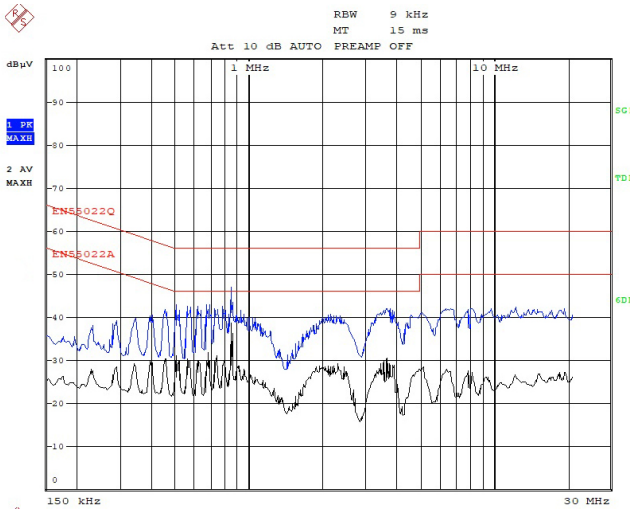


Figure 35. Line, $120V_{AC}$

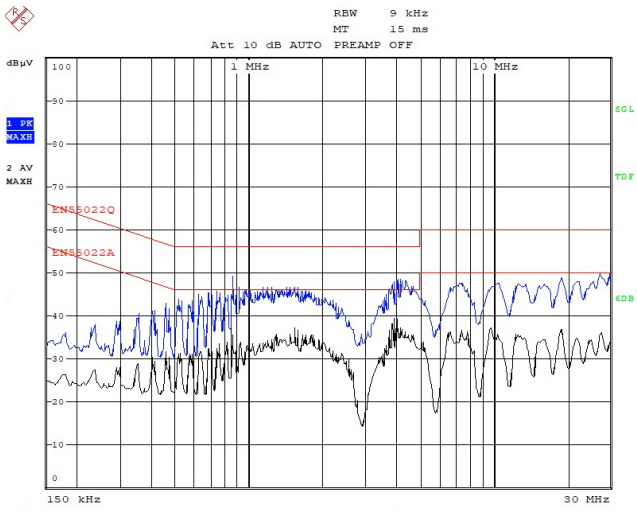


Figure 36. Line, $230V_{AC}$

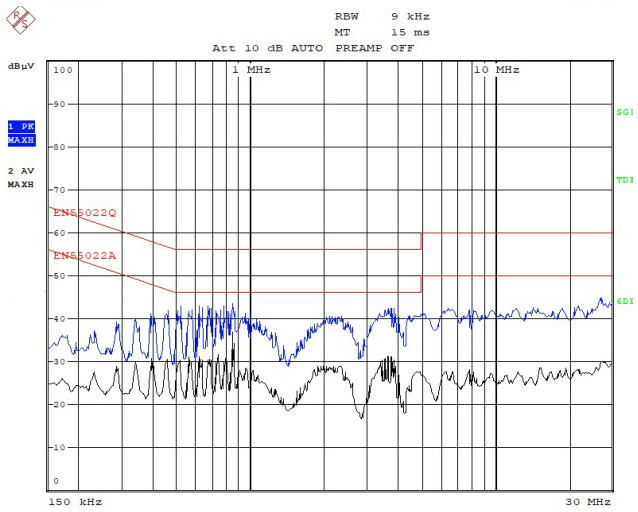


Figure 37. Neutral, $120V_{AC}$

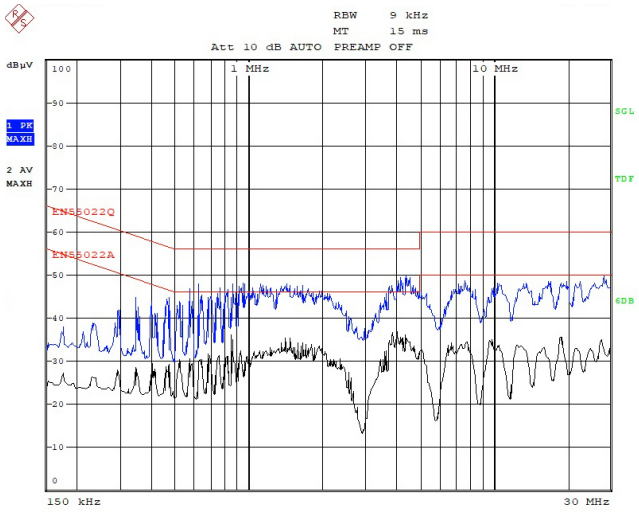


Figure 38. Neutral, $230V_{AC}$

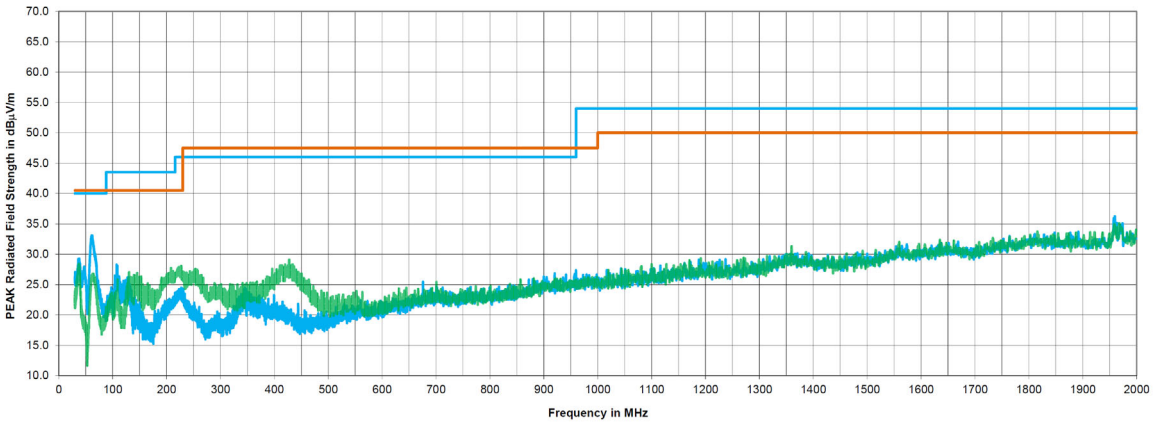


Figure 39. FCC Part15/CISPR22 Class B Radiated Emissions at 3 Meters, $120V_{AC}$, 60Hz (Peak Detector)

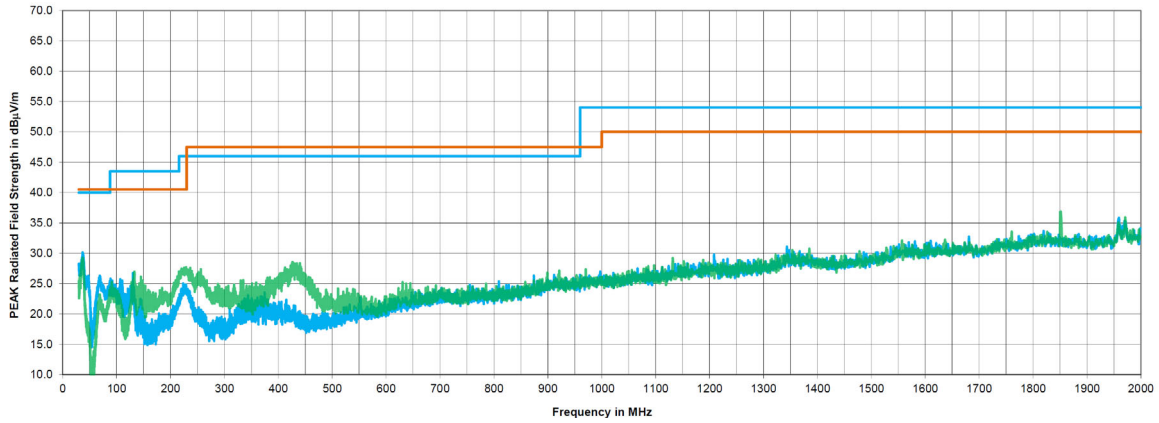
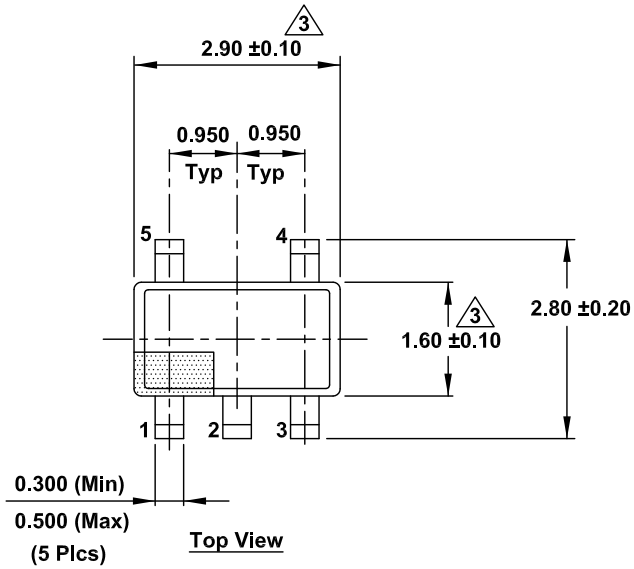


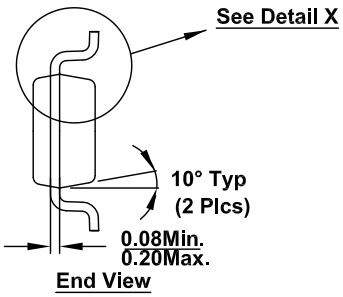
Figure 40. FCC Part15/CISPR22 Class B Radiated Emissions at 3 Meters, $230V_{AC}$, 50Hz (Peak Detector)

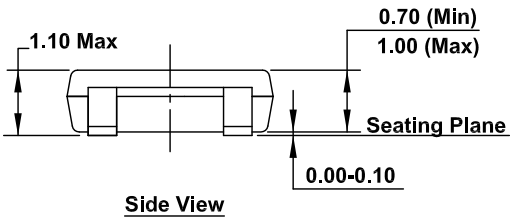
9. Package Outline Drawings

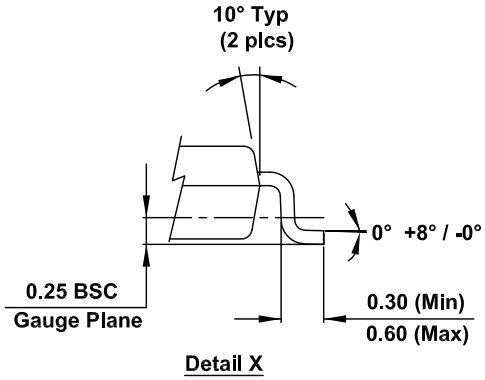
For the most recent package outline drawing, see P5.064B.

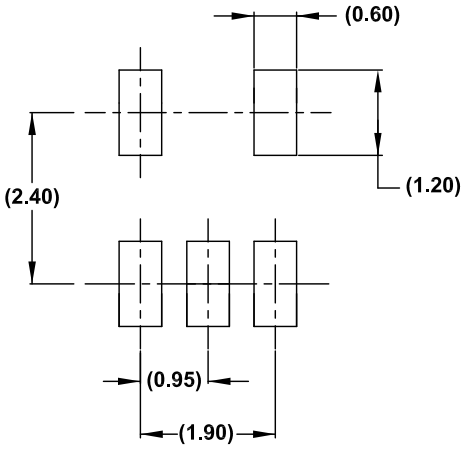
P5.064B
5 Lead Thin Small Outline Transistor (TSOT) Plastic Package
Rev 3, 2/2022











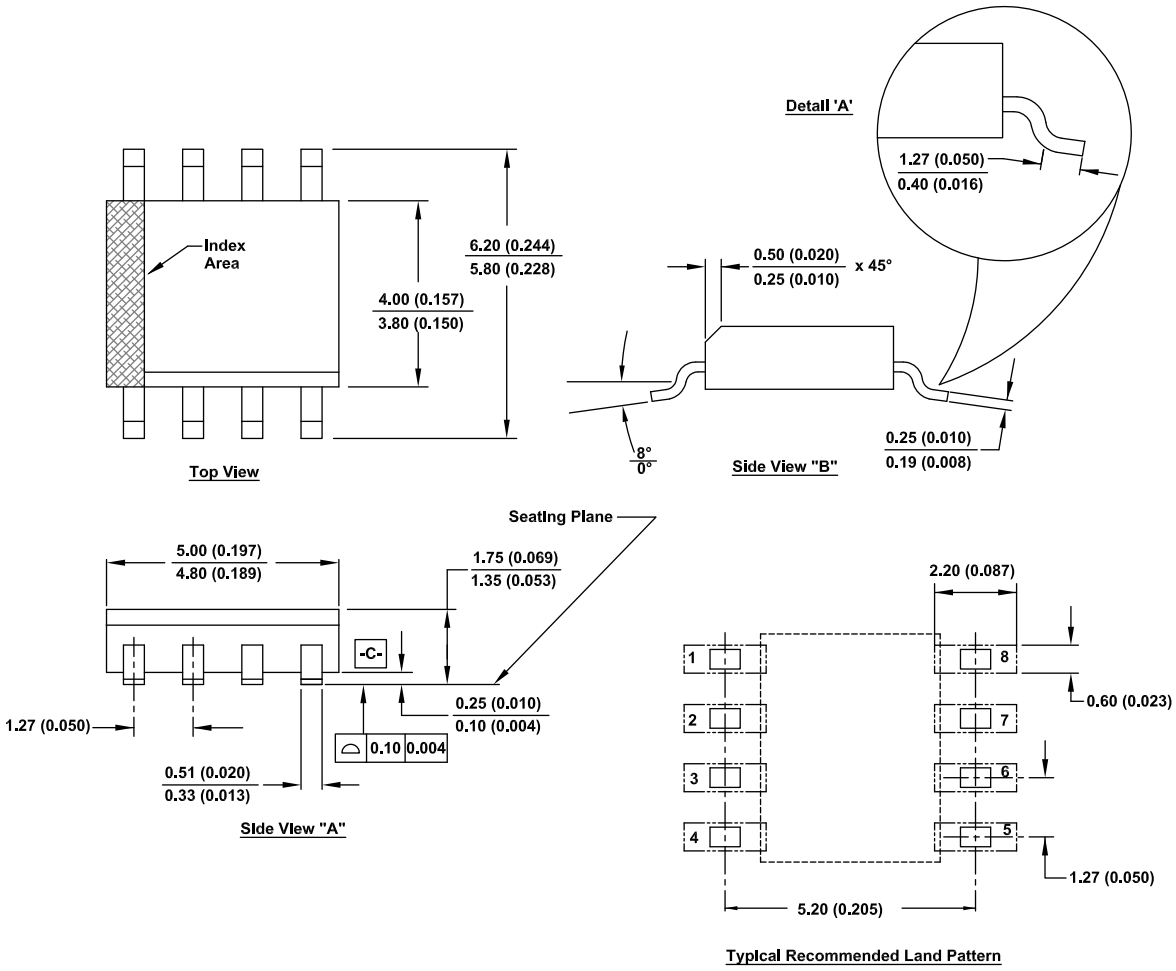
Typical Recommended Land Pattern

NOTE:

1. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
2. Die is facing up for mold. Die is facing down for trim/form, that is reverse trim/form.
3. Dimensions are exclusive of mold flash and gate burr.
4. The footlength measuring is based on the gauge plane method.
5. All specifications comply to JEDEC Spec MO193 Issue C.

For the most recent package outline drawing, see M8.15.

M8.15
8 Lead Narrow Body Small Outline Plastic Package
Rev 7, 9/2023



Notes:

1. Dimensioniong and tolerancing conform to ASME Y14.5M-1994.
2. Package length does not include mold flash, protrusion or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
7. Controlling dimension: MILLIMETER. Converted inch dimension are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

10. Ordering Information

Part Number[1][2]	Part Marking	Package Description (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[3]	Junction Temp Range
RAA2230124GSP#AA0	223012	8 LD SOIC	M8.15	Tube	-40 to +125°C
RAA2230124GSP#MA0				Reel, 250	
RAA2230124GSP#HA0				Reel, 2.5k	
RAA2230124GP3#NA0	012[4]	5 Ld TSOT23	P5.064B	Reel, 250	
RAA2230124GP3#JA0				Reel, 3k	
RTKA223012DR0010BU	Evaluation Board with RAA223012 in 8 LD SOIC package				
RTKA223012DR0020BU	Evaluation Board with RAA223012 in 5 Ld TSOT23 package				

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the RAA223012 device page. For more information about MSL, see TB363.
3. See TB347 for details about reel specifications.
4. The part marking is located on the bottom of the part.

Table 2. Key Differences between Family of Parts

Device	$r_{DS(ON)}$ (Ω)	I_{PK} (mA)	t_{OFF_MIN} (µs)	Package Options
RAA223011	14.5	520	32	8 Ld SOIC, 7 Ld SOIC, 5 Ld TSOT
RAA223012	14.5	335	19	8 Ld SOIC, 5 Ld TSOT
RAA223021	4	1100	23	7 Ld SOIC

11. Revision History

Rev.	Date	Description
3.02	Oct 10, 2023	Updated M8.15 POD to the latest revision (corrected typo).
3.01	Mar 3, 2022	Updated POD P5.064B to the latest revision, changes are as follows: ▪ Corrected pin numbering to align with datasheet and actual unit. ▪ In the End View, widened the lead thickness range to 0.08-0.2mm and removed Note 6.
3.00	Sep 2, 2021	Changed the Theta JC thermal value for the SOT23-5 package from 80 to 71.
2.00	Jun 3, 2021	Applied new template. Updated File Number to R16DS0139EU0200. Changed the SOIC Theta JA from 89 to 86. Changed TSOT23 Theta JC from 60 to 80. Updated Table 2. Updated POD M8.15 to latest revision: -Added the coplanarity specification.
1.01	Feb 25, 2021	Updated Figure 31.
1.00	Dec 16, 2020	Initial release

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use o any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:

www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.