RENESAS

µPC1251A

Single Power Supply Dual Operational Amplifiers

Datasheet

R03DS0117EJ0100 Rev.1.00 2017.12.25

Description

 μ PC1251A is dual operational amplifiers designed for single power supply operation. Main features include low-voltage operation, a common-mode input voltage that range from V⁻ (GND) level, an output from a V⁻ (GND) level that is determined by the output stage utilizing class C push-pull circuit with 50 μ A(TYP.) constant current, and low current consumption.

In addition, this amplifier supports both positive and negative power supply and can be used in various amplifier circuits.

µPC451A which is a quad type with the same circuit configuration is also available under this series of operational amplifiers.

Features

- AEC-Q100 Compliant
- Input Offset Voltage ±2 mV (TYP.)
- Input Offset Current ±5 nA (TYP.)
- Large Signal Voltage Gain 100000 (TYP.)
- Internal Frequency Compensation
- Output Short-Circuit Protection

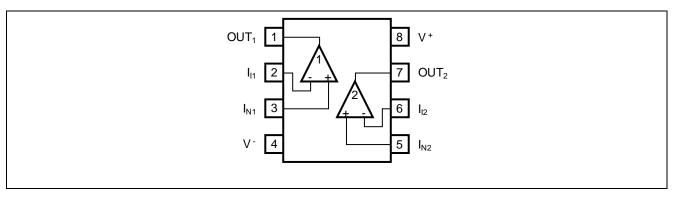
Product Lineup

| Package | Standard SOP | TSSOP | MSOP |
|-----------------------|--------------|-----------------|--|
| Part Name | µPC1251AG2 | µPC1251AGR | µPC1251AMP |
| Outline Comparison | Unit : mm | Unit : mm | Unit : mm |
| | 6.5 5.2 | 4.4 → 3.15 → | $\begin{array}{c c} 0.65 \\ \hline \\ 2.8 \\ \hline \\ \hline \\ + 2.9 \\ \hline \\ + 2.9 \\ \hline \end{array}$ |
| (Mounting Area Ratio) | (100 %) | (60 %) | (34 %) |

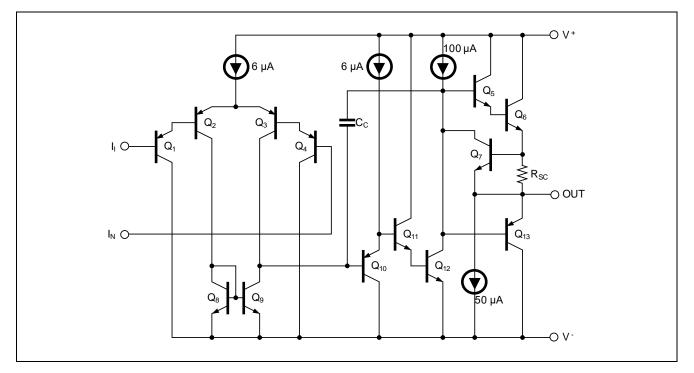
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Pin Configuration (Marking side)



EQUIVALENT CIRCUIT (1/2 Circuit)



ABSOLUTE MAXIMUM RATINGS

| | | | $(T_{A} = 25 \ ^{\circ}C$ |
|--------------------------------------|------------------|---|---------------------------|
| Parameter | Symbol | Ratings | Unit |
| Voltage between V+ and V- Note1 | V + - V - | -0.3 ~ +32 | V |
| Differential Input Voltage | VID | ±32 | V |
| Input Voltage Note 2 | VI | V ⁻ -0.3 ~ V ⁻ +32 | V |
| Output applied Voltage Note 3 | Vo | V ⁻ -0.3 ~ V ⁺ +0.3 | V |
| Total Power Dissipation Note4 | Ρτ | 440 | mW |
| Output Short Circuit Duration Note 5 | ts | Indefinite | S |
| Operating Ambient Temperature | TA | -40 ~ +125 | ۵° |
| Storage Temperature | T _{stg} | -55 ~ +150 | °C |

 $\ensuremath{\left[\ensuremath{\mathsf{Note}} \ensuremath{\right]} 1.$ Note that reverse connections of the power supply may damage the ICs

2. The input voltage is allowed to input without damage or destruction independent of the magnitude of V+. Either input signal is not allowed to go negative by more than 0.3 V. In addition, the input voltage that operates normally as an operational amplifier is within the Common Mode Input Voltage range of an electrical characteristic.

3. A range where input voltage can be applied to an output pin externally with no deterioration or damage to



the feature (characteristic). The input voltage can be applied regardless of the electric supply voltage. This specification which includes the transition state such as electric power ON/OFF must be kept.

4. This is the value when the glass epoxy substrate (size: 100 mm x 100 mm, thickness: 1 mm, 15% of the substrate area where only one side is copper foiled is filling wired) is mounted.

Note that restrictions will be made to the following conditions for each product, and the derating ratio depending on the operating ambient temperature.

 $\mu PC1251AG2$: Derate at -4.4 mW/°C when T_A $\,>\,$ 25 °C

(Junction – ambient thermal resistance $R_{th(J-A)} = 227^{\circ}C/W$)

 $\mu PC1251AGR$: Derate at -5.5 mW/°C when T_A ~>~69 °C

(Junction – ambient thermal resistance $R_{th(J-A)} = 183^{\circ}C/W$)

 $\mu PC1251AMP$: Derate at -4.8 mW/°C when T_A $\,>\,$ 58 °C

(Junction – ambient thermal resistance $R_{th(J-A)} = 208^{\circ}C/W$)

Short circuits from the output to V⁺ can cause destruction. (V⁺ ≤ +15V, for any one channel only) Pay careful attention to the total power dissipation by not exceeding the absolute maximum ratings, Note 4.

RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | MIN. | TYP. | MAX. | Unit |
|----------------------------------|--------|------|------|------|------|
| Power Supply Voltage (Split) | V ± | ±1.5 | | ±15 | V |
| Power Supply Voltage (V - = GND) | V + | +3 | | +30 | V |

ELECTRICAL CHARACTERISTICS

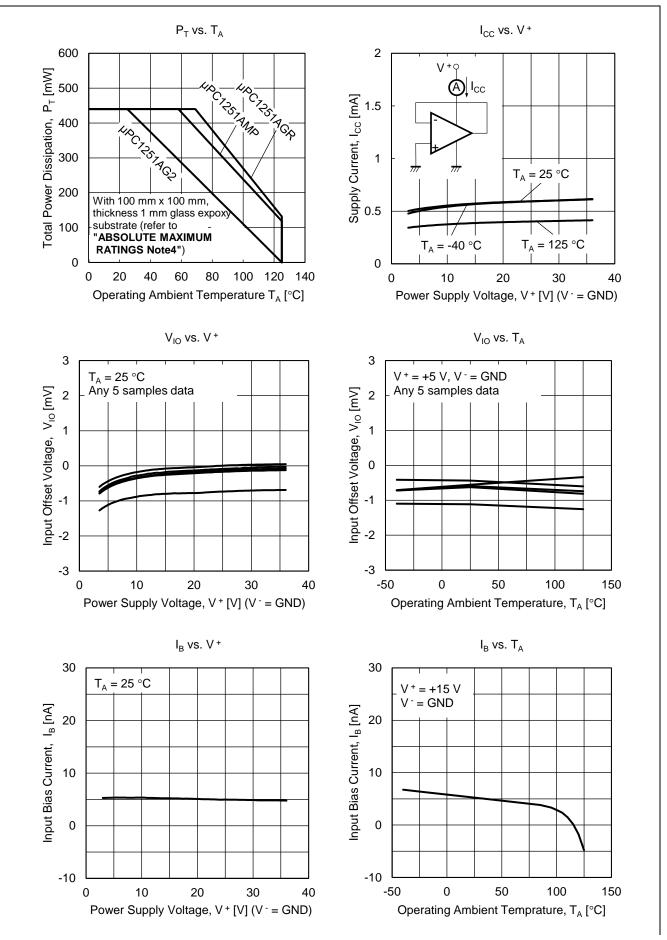
 $(T_A = 25 \text{ °C}, V^+ = +5 \text{ V}, V^- = \text{GND})$

| Parameter | Symbol | MIN. | TYP. | MAX. | Unit | Test Condition |
|------------------------------------|-----------------|-------|--------|--------|------|--|
| Input Offset Voltage | Vio | | ±2 | ±7 | mV | Rs = 0 Ω |
| Input Offset Current | l _{io} | | ±5 | ±50 | nA | |
| Input Bias Current Note 6 | IB | | 45 | 250 | nA | |
| Large Signal Voltage Gain | Av | 25000 | 100000 | | | $R_L \ge 2 k\Omega$ |
| Circuit Current Note 7 | Icc | | 0.7 | 1.2 | mA | R _L = ∞, I _O = 0 A |
| Common Mode Rejection Ratio | CMR | 65 | 70 | | dB | |
| Supply Voltage Rejection Ratio | SVR | 65 | 100 | | dB | |
| Output Voltage Swing | Vo | 0 | | V+-1.5 | V | $R_{\perp} = 2 k\Omega$ (connected to GND) |
| Common Mode Input Voltage Range | VICM | 0 | | V+-1.5 | V | |
| Output Source Current | IO SOURCE | 20 | 40 | | mA | $V_{IN(+)} = +1 V, V_{IN(-)} = 0 V$ |
| Output Sink Current | IO SINK1 | 10 | 20 | | mA | $V_{IN(-)} = +1 V, V_{IN(+)} = 0 V$ |
| | IO SINK2 | 12 | 50 | | μA | $V_{IN (-)} = +1 V, V_{IN (+)} = 0 V,$ $V_0 = 200 mV$ |
| Channel Separation | | | 120 | | dB | f = 1 ~ 20 kHz |

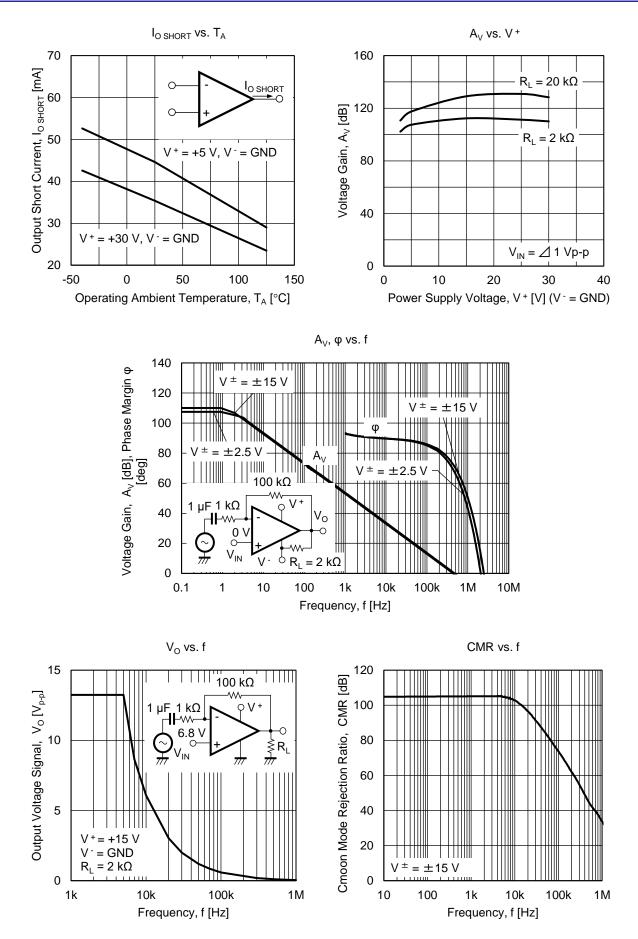
(Note) 6. The absolute value of the input bias current is small, thus the direction of the current flowing from the inside of the IC may be reversed due to variations in the product during high temperature.

7. This is a current that flows in the internal circuit. This current will flow irrespective of the channel used.

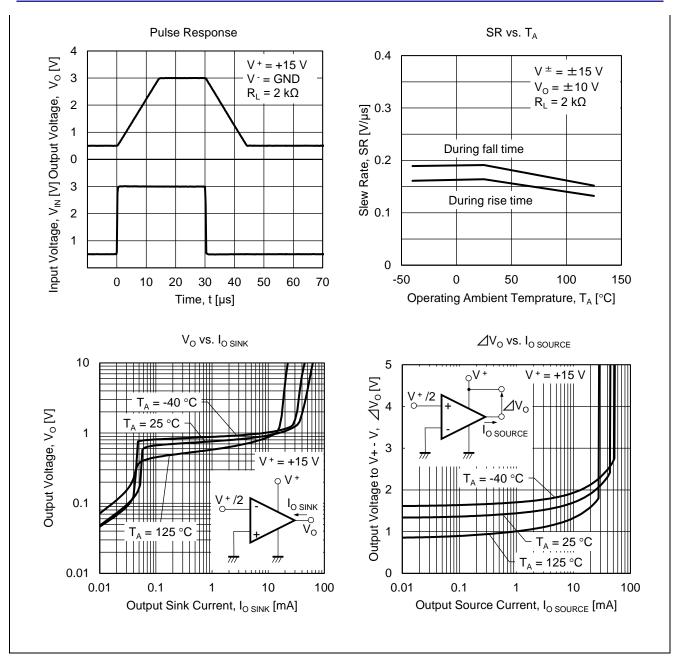
TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25 °C, TYP.) (Reference Value)











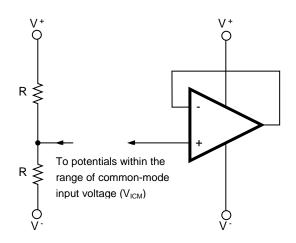


PRECAUTION

• The process of unused circuits

If there is unused circuit, the following connection is recommended.

Process example of unused circuits



Remark: A midpoint potential of V^+ and V^- is applied to this example.

Ratings of input/output pin voltage

When the voltage of input/output pin exceeds the absolute maximum rating, the parasitic diode within the IC may conduct, causing characteristics degradation or damage. In addition, if the input pin is lower than V^- , or the output pin exceeds the power supply voltage, it is recommended to make a clamp circuit using a diode with low forward voltage (e.g.: Schottky diode) as protection.

• Range of common-mode input voltage

When the supply voltage does not meet the condition of electrical characteristics, the range of commonmode input voltage is as follows.

 V_{ICM} (TYP.): V⁻ to V⁺ - 1.5 (V) (T_A = 25°C).

During designing, do include some tolerance by considering temperature characteristics and etc.

Maximum output voltage

The TYP. value range of the maximum output voltage when the supply voltage does not meet the condition of electrical characteristics is as follows:

 V_{om^+} (TYP.): V⁺ – 1.5 (V) (T_A = 25°C), V_{om^-} (TYP.) (I_{O SINK} ≤ 50 µA): Approx. V⁻ (V) (T_A = 25°C).

During designing, include some tolerance such as characteristics variation and temperature characteristics consideration and so forth. In addition, also note that the output voltage range $(V_{om}^+ - V_{om}^-)$ will become narrow when an output current increases.

• Operation of output

This IC output level consist of a class C push-pull. Therefore, when a load resistance is connected to the midpoint potential of V⁺, V⁻, a crossover distortion occurs during the transition state of output current flow direction (source, sink).

Handling of ICs

Warpage or bending of a PCB board will apply stress to the ICs, the characteristic may change due to piezoelectric effect. Therefore, pay attention to warpage or bending of the board.

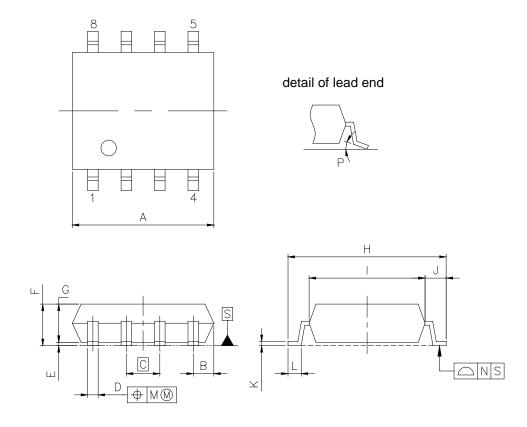


PACKAGE DRAWINGS

8-PIN PLASTIC SOP

| JEITA Package code | RENESAS code | Previous code | MASS (TYP.) [g] |
|--------------------|--------------|---------------|-----------------|
| P-SOP8-0225-1.27 | PRSP0008DL-A | S8GM-50-225B | 0.08 |

Unit : mm



NOTE

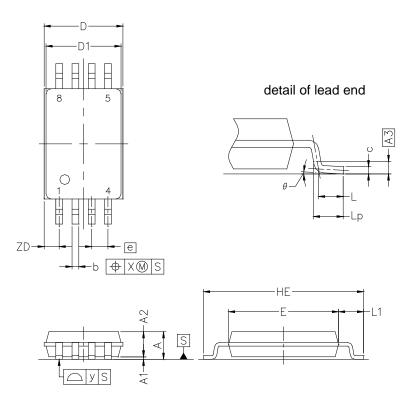
Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS |
|------|--------------------------------|
| A | 5.2 ^{+0.17} -0.20 |
| В | 0.78 MAX |
| С | 1.27 (T.P) |
| D | 0.42 ^{+0.08} -0.07 |
| E | 0.1 ±0.1 |
| F | 1.59 ±0.21 |
| G | 1.49 |
| Н | 6.5 ±0.3 |
| | 4.4 ±0.15 |
| J | 1.1 ±0.2 |
| K | 0.17 ^{+0.08} -0.07 |
| L | 0.6 ±0.2 |
| М | 0.12 |
| Ν | 0.10 |
| Р | 3° +7° -3° |



8-PIN PLASTIC TSSOP

| JEITA Package code | RENESAS code | Previous code | MASS(TYP.) [g] |
|--------------------|--------------|---------------|----------------|
| P-TSSOP8-0225-0.65 | PTSP0008JD-A | P8GR-65-9LG | _ |



NOTE

Each lead centerline is located within 0.10 mm of its true position at maximum material condition.

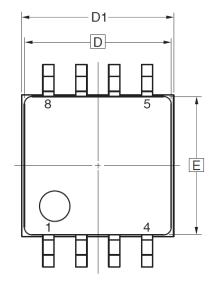
| ITEM | MILLIMETERS |
|------|--------------------------------|
| D | 3.15 ±0.15 |
| D1 | 3.00 ±0.10 |
| E | 4.40 ±0.10 |
| HE | 6.40 ±0.20 |
| Α | 1.20 MAX. |
| A1 | 0.10 ±0.05 |
| A2 | 1.00 ±0.05 |
| A3 | 0.25 |
| b | 0.24 ^{+0.06} -0.05 |
| С | 0.145 ±0.055 |
| L | 0.5 |
| Lp | 0.60 ±0.15 |
| L1 | 1.00 ±0.20 |
| θ | 3° +5° -3° |
| е | 0.65 |
| х | 0.10 |
| у | 0.10 |
| ZD | 0.60 |

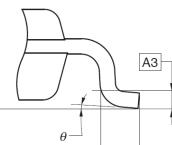


8-PIN PLASTIC MSOP

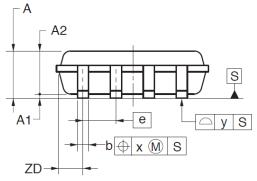
| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|-----------------------|--------------|---------------|-----------------|
| P-TSSOP8-2.8x2.9-0.65 | PTSP0008JF-A | P8MP-65-KAA-1 | 0.02 |

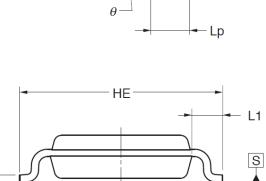
С





detail of lead end





NOTE

Each lead centerline is located within 0.10 mm of its true position at maximum material condition.

| | (UNIT:mm) |
|------|----------------------------|
| ITEM | DIMENSIONS |
| D | 2.90 |
| D1 | $3.00\pm\!0.20$ |
| E | 2.80 |
| HE | $4.00\pm\!0.20$ |
| е | 0.65 |
| b | $0.22\pm\!0.05$ |
| А | 1.03 MAX. |
| A1 | $0.08\pm\!0.05$ |
| A2 | 0.85 ± 0.05 |
| A3 | 0.25 |
| L1 | 0.60±0.20 |
| С | $0.145 \pm 0.05 \\ - 0.03$ |
| Lp | 0.37 ±0.10 |
| Х | 0.10 |
| У | 0.10 |
| θ | 3° +5° -3° |
| ZD | 0.525 |
| | |



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