## General Description

The 845252 is a 3.3V/2.5V CML clock generator designed for Ethernet applications. The device synthesizes either a 50MHz, 62.5MHz, 100MHz, 125MHz, 156.25MHz, 250MHz or 312.5MHz clock signal with excellent phase jitter performance. The clock signal is distributed to two low-skew differential CML outputs. The device is suitable for driving the reference clocks of Ethernet PHYs. The device supports 3.3V and 2.5V voltage supply and is packaged in a small, lead-free (RoHS 6) 32-lead VFQFN package. The extended temperature range supports telecommunication, wireless infrastructure and networking end equipment requirements. The device is a member of the family of High Performance Clock Solutions from IDT.

## Features

- Clock generation of: 50MHz, 62.5MHz, 100MHz, 125MHz, 156.25MHz, 250MHz and 312.5MHz
- Two differential CML clock output pairs
- Crystal interface designed for 25MHz, 18pF parallel resonant crystal
- RMS phase jitter @ 125MHz, using a 25MHz crystal (1.875MHz – 20MHz): 400fs (typical), 3.3V
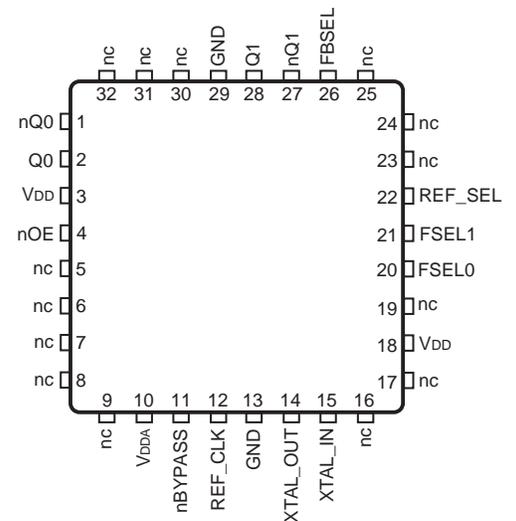
| Offset | Noise Power |
|---|---|
| 100Hz | -102.4 dBc/Hz |
| 1kHz | -119.4 dBc/Hz |
| 10kHz | -124.8 dBc/Hz |
| 100kHz | -125.7 dBc/Hz |

- LVCMOS interface levels for the control inputs
- Full 3.3V and 2.5V supply voltage
- Available in lead-free (RoHS 6) 32 VFQFN package
- -40°C to 85°C ambient operating temperature
- For functional replacement part use 8T49N241

## Block Diagram
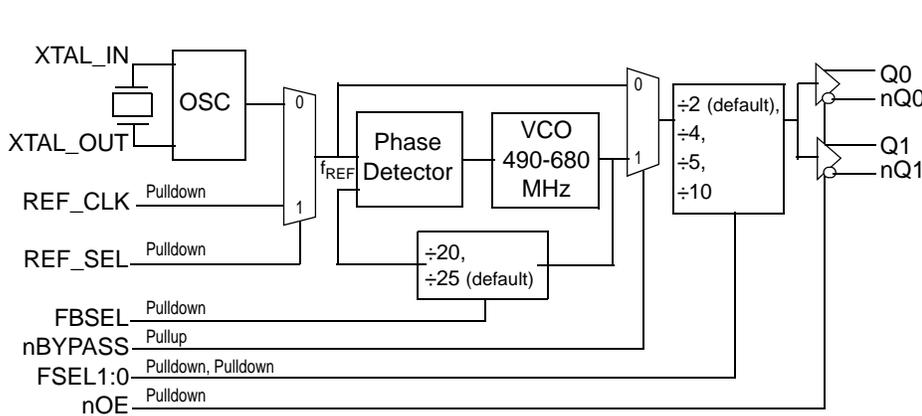


## Pin Assignment



**845252**
**32 lead VFQFN**
**5.0mm x 5.0mm x 0.925mm package body**
**K Package**
**Top View**

# Table 1. Pin Descriptions

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1, 2 | nQ0, Q0 | Output | | Differential clock output pair. CML interface levels. |
| 3, 18 | $V_{DD}$ | Power | | Core supply pins. |
| 4 | nOE | Input | Pulldown | Output enable pin. See Table 3E for function. LVCMOS/LVTTL interface levels. |
| 5, 6, 7, 8, 9, 16, 17, 19, 23, 24, 25, 30, 31, 32 | nc | Unused | | Do not connect. |
| 10 | $V_{DDA}$ | Power | | Analog supply pin. |
| 11 | nBYPASS | Input | Pullup | PLL bypass pin. See Table 3D for function. LVCMOS/LVTTL interface levels. |
| 12 | REF_CLK | Input | Pulldown | Single-ended reference clock input. LVCMOS/LVTTL interface levels. |
| 13, 29 | GND | Power | | Power supply ground. |
| 14, 15 | XTAL_OUT, XTAL_IN | Input | | Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output. |
| 20, 21 | FSEL0, FSEL1 | Input | Pulldown | Output frequency divider select enable pins. See Table 3C for function. LVCMOS/LVTTL interface levels. |
| 22 | REF_SEL | Input | Pulldown | PLL reference clock select pin. See Table 3A for function. LVCMOS/LVTTL interface levels. |
| 26 | FBSEL | Input | Pulldown | PLL feedback divider select pin. See Table 3B for function. LVCMOS/LVTTL interface levels. |
| 27, 28 | nQ1, Q1 | Output | | Differential clock output pair. CML interface levels. |

NOTE: *Pulldown* and *Pullup* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

# Table 2. Pin Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | 4 | | pF |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | kΩ |
| $R_{PULLUP}$ | Input Pullup Resistor | | | 51 | | kΩ |

# Function Tables

### Table 3A. PLL Reference Clock Select Function Table

| Input<br>REF_SEL | Operation |
|---|---|
| 0 (default) | The crystal interface is the selected. |
| 1 | The REF_CLK input is the selected. |

NOTE: REF_SEL is an asynchronous control.

### Table 3B. PLL Feedback Select Function Table

| Input<br>FBSEL | Operation |
|---|---|
| 0 (default) | $f_{VCO} = f_{REF} * 25$ |
| 1 | $f_{VCO} = f_{REF} * 20$ |

NOTE: FBSEL is an asynchronous control.

### Table 3C. Output Divider Select Function Table

| Input | | | Output Frequency $f_{OUT}$ with $f_{REF}$ = 25MHz | |
|---|---|---|---|---|
| FSEL1 | FSEL0 | Operation | FBSEL = 0 | FBSEL = 1 |
| 0 (default) | 0 (default) | $f_{OUT} = f_{VCO} \div 2$ | 312.5MHz | 250MHz |
| 0 | 1 | $f_{OUT} = f_{VCO} \div 4$ | 156.25MHz | 125MHz |
| 1 | 0 | $f_{OUT} = f_{VCO} \div 5$ | 125MHz | 100MHz |
| 1 | 1 | $f_{OUT} = f_{VCO} \div 10$ | 62.5MHz | 50MHz |

NOTE: FSEL[1:0] are asynchronous controls.

### Table 3D. PLL nBYPASS Function Table

| Input<br>nBYPASS | Operation |
|---|---|
| 0 | PLL is bypassed. The reference frequency $f_{REF}$ is divided by the selected output divider. AC specifications do not apply in PLL bypass mode. |
| 1 (default) | PLL is enabled. The reference frequency $f_{REF}$ is multiplied by the selected feedback divider and then divided by the selected output divider. |

NOTE: nBYPASS is an asynchronous control.

### Table 3E. Output Enable Function Table

| Input<br>nOE | Operation |
|---|---|
| 0 (default) | Outputs enabled. |
| 1 | Outputs disabled (high-impedance). |

NOTE: nOE is an asynchronous control.

# Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device.
These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond
those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for
extended periods may affect product reliability.

| Item | Rating |
|---|---|
| Supply Voltage, $V_{DD}$ | 4.6V |
| Inputs, $V_I$ | -0.5V to $V_{DD}$ + 0.5V |
| Outputs, $I_O$<br> Continuous Current<br> Surge Current | <br>10mA<br>15mA |
| Package Thermal Impedance, $\theta_{JA}$ | 43.4°C/W (0 mps) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

# DC Electrical Characteristics

### Table 4A. Power Supply DC Characteristics, $V_{DD}$ = 3.3V±5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{DDA}$ | Analog Supply Voltage | | $V_{DD} - 0.12$ | 3.3 | $V_{DD}$ | V |
| $I_{DD}$ | Power Supply Current | | | | 88 | mA |
| $I_{DDA}$ | Analog Supply Current | | | | 12 | mA |

### Table 4B. Power Supply DC Characteristics, $V_{DD}$ = 2.5V±5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Core Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| $V_{DDA}$ | Analog Supply Voltage | | $V_{DD} - 0.11$ | 2.5 | $V_{DD}$ | V |
| $I_{DD}$ | Power Supply Current | | | | 84 | mA |
| $I_{DDA}$ | Analog Supply Current | | | | 11 | mA |

**Table 4C. LVCMOS/LVTTL Input DC Characteristics,** $V_{DD}$ = 3.3V±5% or 2.5V±5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|--------|-----------|---|-----------------|---------|---------|---------|-------|
| $V_{IH}$ | Input High Voltage | | $V_{DD}$ = 3.3V | 2 | | $V_{DD}$ + 0.3 | V |
| | | | $V_{DD}$ = 2.5V | 1.7 | | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | | $V_{DD}$ = 3.3V | -0.3 | | 0.8 | V |
| | | | $V_{DD}$ = 2.5V | -0.3 | | 0.7 | V |
| $I_{IH}$ | Input High Current | FBSEL, nOE, FSEL[1:0], REF_SEL, REF_CLK | $V_{DD}$ = $V_{IN}$ = 3.465V | | | 150 | µA |
| | | nBYPASS | $V_{DD}$ = $V_{IN}$ = 3.465V | | | 5 | µA |
| $I_{IL}$ | Input Low Current | FBSEL, nOE, FSEL[1:0], REF_SEL, REF_CLK | $V_{DD}$ = 3.465V or 2.625V, $V_{IN}$ = 0V | -5 | | | µA |
| | | nBYPASS | $V_{DD}$ = 3.465V or 2.625V, $V_{IN}$ = 0V | -150 | | | µA |

**Table 4D. CML DC Characteristics,** $V_{DD}$ = 3.3V±5% or 2.5V±5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------|-----------|-----------------|---------|---------|---------|-------|
| $V_{OH}$ | Output High Voltage | | $V_{DD}$ - 0.02 | $V_{DD}$ - 0.01 | $V_{DD}$ | V |
| $V_{OUT}$ | Output Voltage Swing | | 325 | 400 | 600 | mV |
| $V_{DIFF\_OUT}$ | Differential Output Voltage Swing | | 650 | 800 | 1200 | mV |

**Table 5. Crystal Characteristics**

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------|---------|---------|---------|-------|
| Mode of Oscillation | | | Fundamental | | |
| Frequency | | | 25 | | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitance | | | | 7 | pF |

# AC Characteristics

**Table 6A. AC Characteristics,** $V_{DD}$ = 3.3V±5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency; NOTE 1 | FBSEL = 0, FSEL[1:0] = 00 | | 312.5 | | MHz |
| | | FBSEL = 0, FSEL[1:0] = 01 | | 156.25 | | MHz |
| | | FBSEL = 0, FSEL[1:0] = 10 | | 125 | | MHz |
| | | FBSEL = 0, FSEL[1:0] = 11 | | 62.5 | | MHz |
| | | FBSEL = 1, FSEL[1:0] = 00 | | 250 | | MHz |
| | | FBSEL = 1, FSEL[1:0] = 01 | | 125 | | MHz |
| | | FBSEL = 1, FSEL[1:0] = 10 | | 100 | | MHz |
| | | FBSEL = 1, FSEL[1:0] = 11 | | 50 | | MHz |
| tsk(o) | Output Skew; NOTE 1, 2, 3 | | | | 60 | ps |
| tjit(Ø) | RMS Phase Jitter (Random); NOTE 4 | FSEL = 0, 125MHz, Integration Range: 1.875MHz – 20MHz | | 400 | | fs |
| | | FSEL = 0, 156.25MHz, Integration Range: 1.875MHz – 20MHz | | 408 | | fs |
| $t_R$ / $t_F$ | Output Rise/Fall Time | 20% to 80% | 300 | | 850 | ps |
| odc | Output Duty Cycle | FBSEL[1:0] ≠ 10 | 48 | | 52 | % |
| | | FBSEL[1:0] = 10 | 46 | | 54 | % |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: $f_{REF}$ = 25 MHz.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
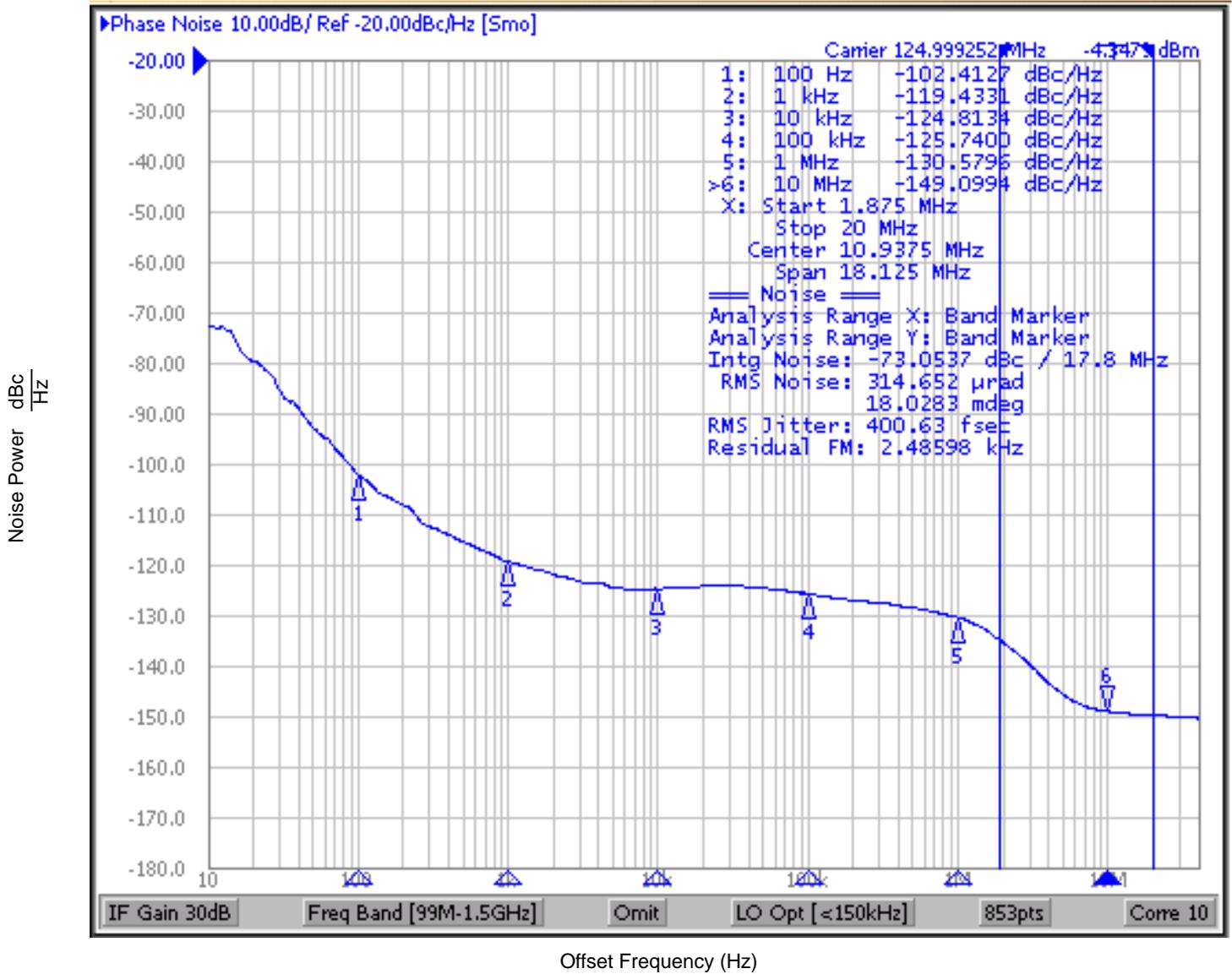NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Please refer to the phase noise plots.

**Table 6B. AC Characteristics,** $V_{DD}$ = 2.5V±5%, $T_A$ = -40°C to 85°C

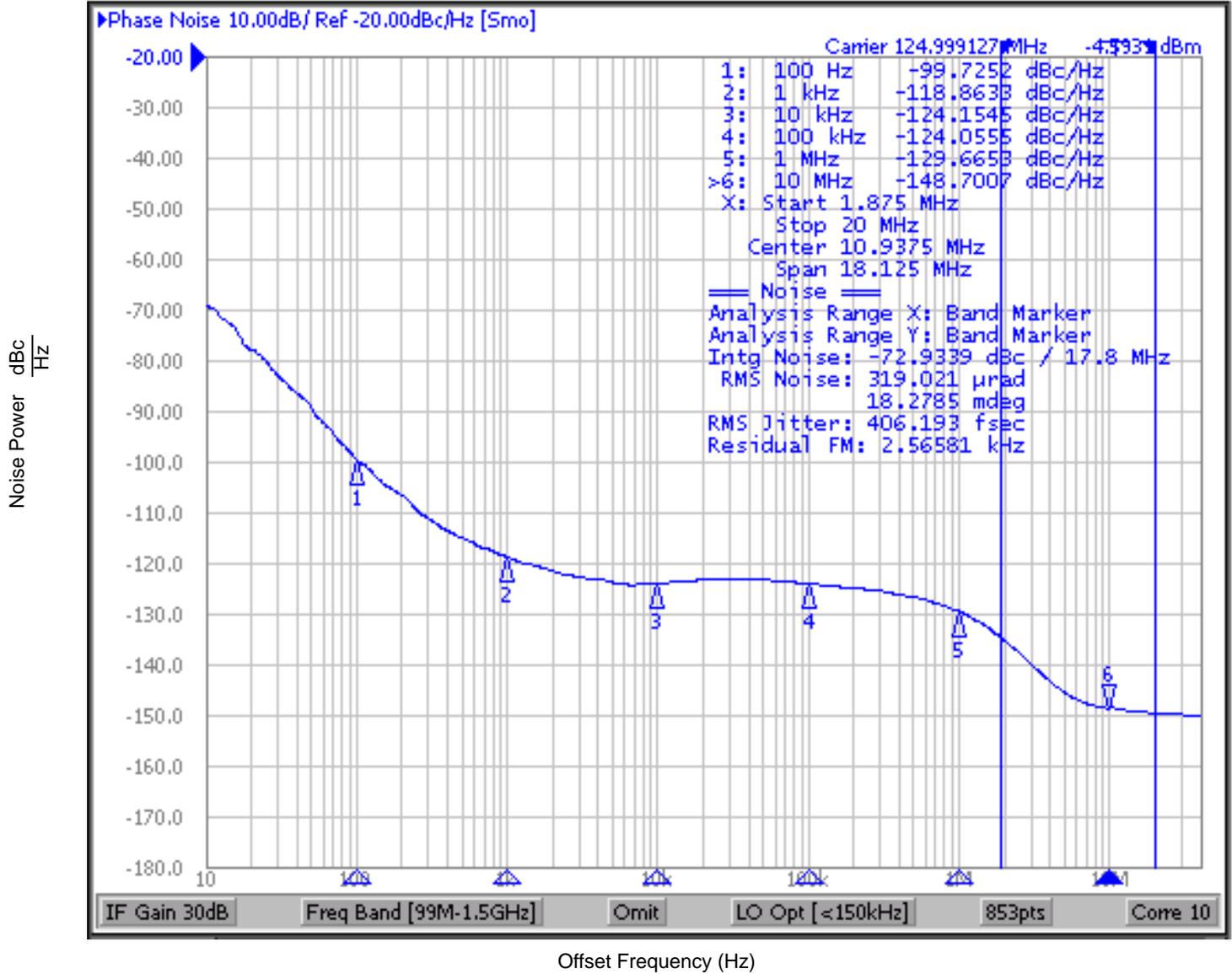| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency; NOTE 1 | FBSEL = 0, FSEL[1:0] = 00 | | 312.5 | | MHz |
| | | FBSEL = 0, FSEL[1:0] = 01 | | 156.25 | | MHz |
| | | FBSEL = 0, FSEL[1:0] = 10 | | 125 | | MHz |
| | | FBSEL = 0, FSEL[1:0] = 11 | | 62.5 | | MHz |
| | | FBSEL = 1, FSEL[1:0] = 00 | | 250 | | MHz |
| | | FBSEL = 1, FSEL[1:0] = 01 | | 125 | | MHz |
| | | FBSEL = 1, FSEL[1:0] = 10 | | 100 | | MHz |
| | | FBSEL = 1, FSEL[1:0] = 11 | | 50 | | MHz |
| tsk(o) | Output Skew; NOTE 1, 2, 3 | | | | 60 | ps |
| tjit(Ø) | RMS Phase Jitter (Random); NOTE 4 | FSEL = 0, 125MHz, Integration Range: 1.875MHz – 20MHz | | 406 | | fs |
| | | FSEL = 0, 156.25MHz, Integration Range: 1.875MHz – 20MHz | | 441 | | fs |
| $t_R$ / $t_F$ | Output Rise/Fall Time | 20% to 80% | 300 | | 850 | ps |
| odc | Output Duty Cycle | FBSEL[1:0] ≠ 10 | 48 | | 52 | % |
| | | FBSEL[1:0] = 10 | 46 | | 54 | % |

For NOTES see Table 6A above.

# Typical Phase Noise at 125MHz (3.3V)



Offset Frequency (Hz)

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# Typical Phase Noise at 125MHz (2.5V)

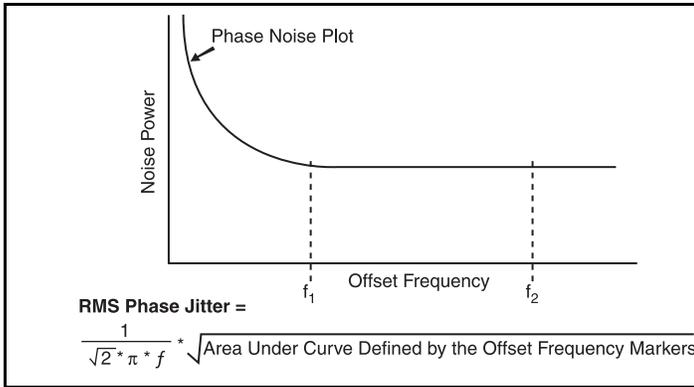Revision B,   November 11, 2016

# Parameter Measurement Information
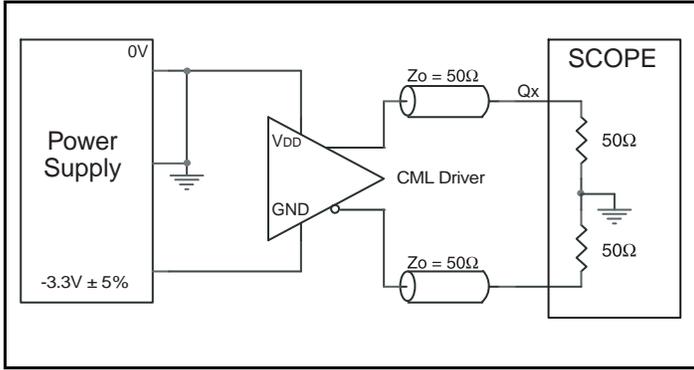


**3.3V CML Output Load AC Test Circuit**
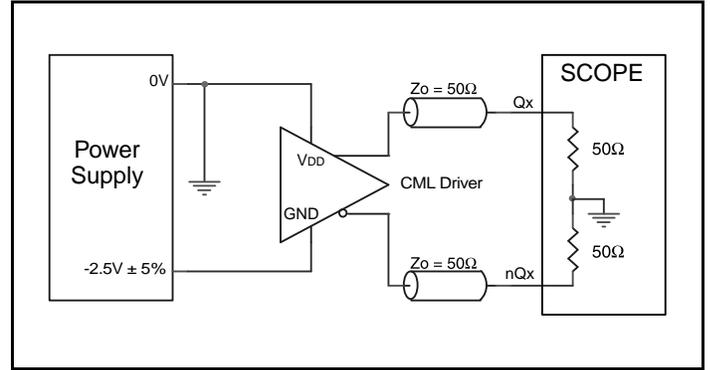


**2.5V CML Output Load AC Test Circuit**



**RMS Phase Jitter =**

$$\frac{1}{\sqrt{2} * \pi * f} * \sqrt{\text{Area Under Curve Defined by the Offset Frequency Markers}}$$

**RMS Phase Jitter**
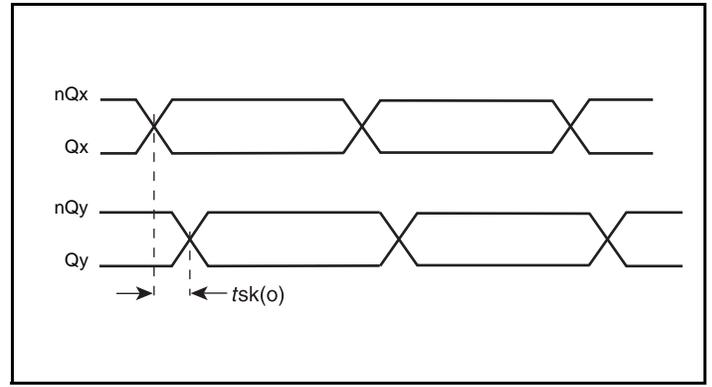


**Output Skew**
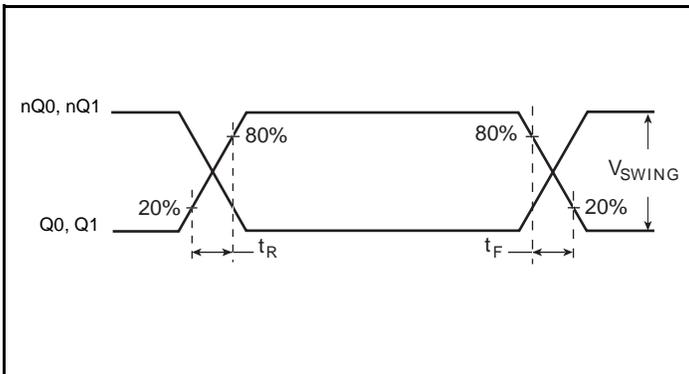


**Output Rise/Fall Time**



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$
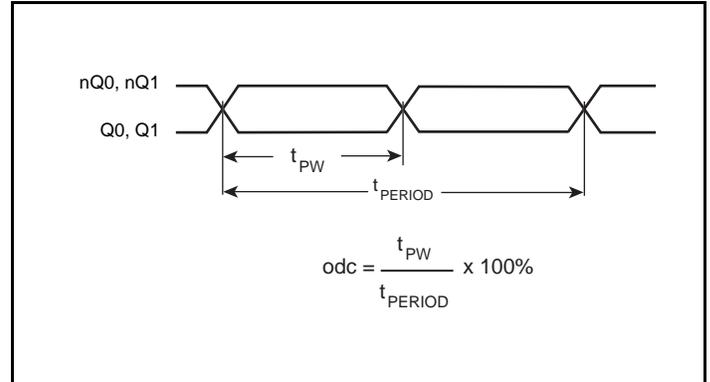
**Output Duty Cycle/Pulse Width/Period**

# Application Information

## Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 845252 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. $V_{DD}$ and $V_{DDA}$ should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic $V_{DD}$ pin and also shows that $V_{DDA}$ requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the $V_{DDA}$ pin.



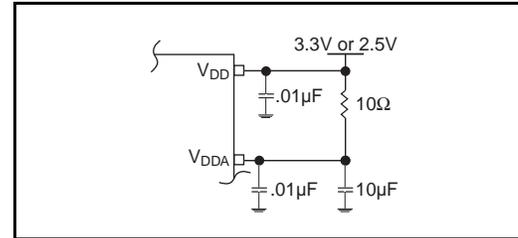**Figure 1. Power Supply Filtering**

## Recommendations for Unused Input and Output Pins

### Inputs:

#### LVCMOS Control Pins

All control pins have internal pullups and pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

#### Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

#### REF_CLK Input

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

### Outputs:

#### CML Outputs

All unused CML outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

# Crystal Input Interface

The 845252 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.
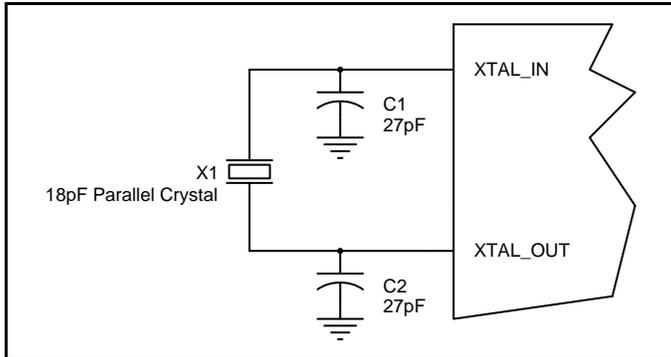


**Figure 2. Crystal Input Interface**

# LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS signals, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.
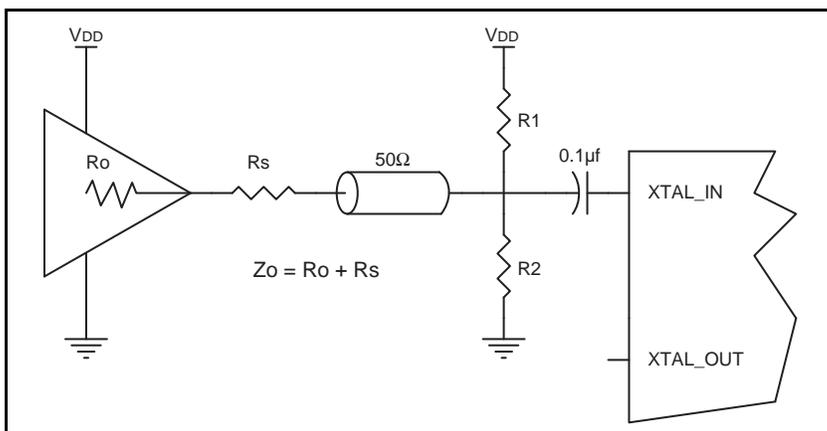


**Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface**

## VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor's Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.
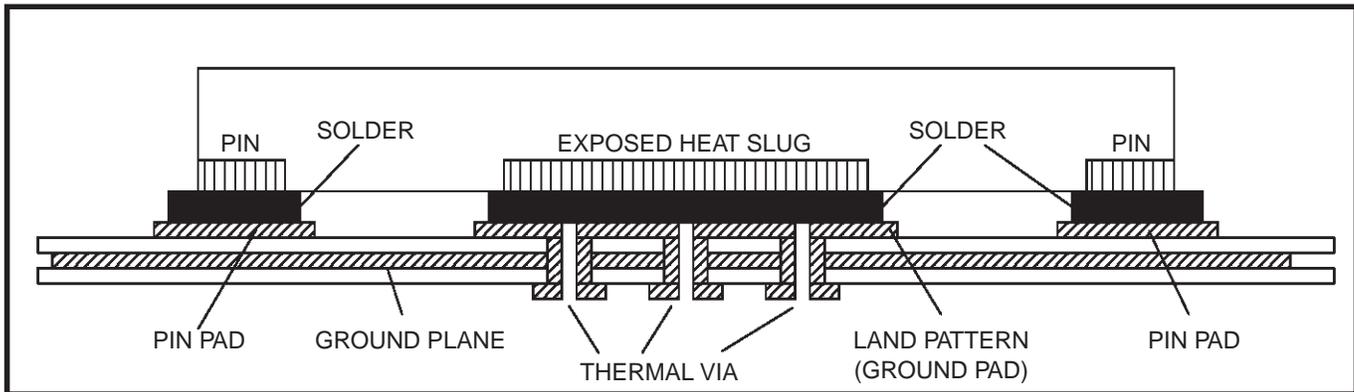


**Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)**

# Power Considerations

This section provides information on power dissipation and junction temperature for the 845252.
Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 845252 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for $V_{DD}$ = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = $V_{DD\_MAX}$ * ($I_{DD}$ + $I_{DDA}$) = 3.465V * (88mA + 12mA) = **346.5mW**

- Power (outputs)$_{MAX}$ = **35.76mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 * 35.76mW = **71.52mW**

**Total Power**$_{\_MAX}$ (3.465V, with all outputs switching) = 346.5mW + 71.52mW = **418.02mW**

### 2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

$\theta_{JA}$ = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming no air flow and a multi-layer board, the appropriate value is 43.4°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.418W * 43.4°C/W = 103°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 7. Thermal Resistance $\theta_{JA}$ for 32 Lead VFQFN, Forced Convection**

| $\theta_{JA}$ by Velocity | | | |
|---|---|---|---|
| Meters per Second | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 43.4°C/W | 37.9°C/W | 34.0°C/W |

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### 3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the CML driver output pair. The CML output circuit and termination are shown in Figure 5.
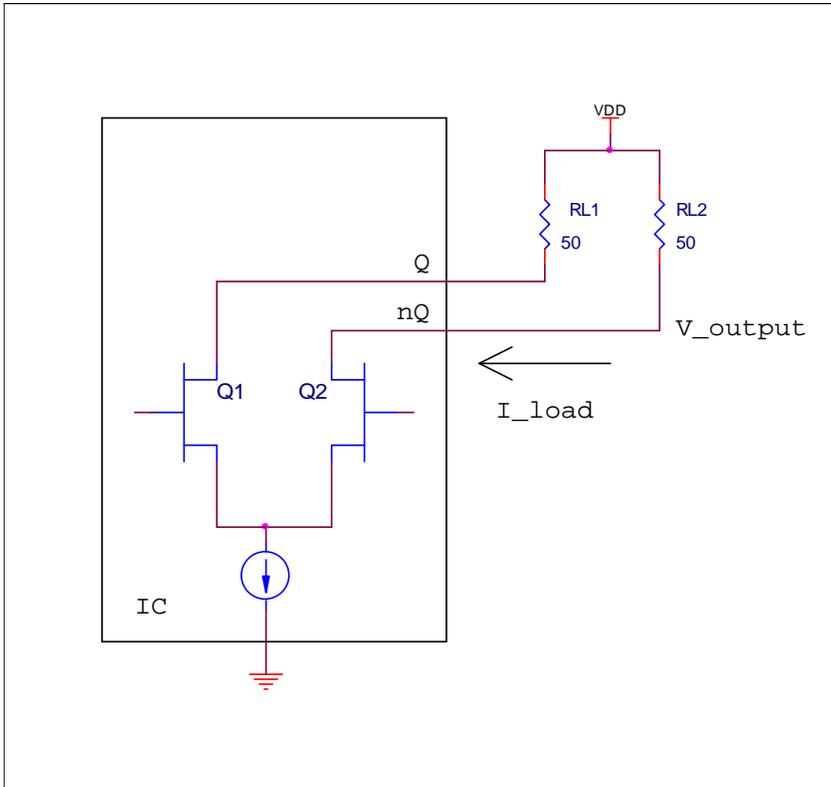


**Figure 5. CML Driver (without built-in 50Ω pullup) Circuit and Termination**

To calculate worst case power dissipation into the load, use the following equations:

Power dissipation when the output driver is logic LOW:

Pd_L = I Load * V Output

$= (V_{OUT\_MAX} /R_{L)} * (V_{DD\_MAX} - V_{OUT\_MAX})$

$= (600mV/50Ω) * (3.465V - 600mV)$

$= 34.38mW$

Power dissipation when the output driver is logic HIGH:

Pd_H = I Load * V Output

$= (0.02V/50Ω) * (3.465V - 0.02V)$

$= 1.38mW$

Total Power Dissipation per output pair = Pd_H + Pd_L = **35.76mW**

# Reliability Information

**Table 8.** $\theta_{JA}$ **vs. Air Flow Table for a 32 VFQFN**

| $\theta_{JA}$ vs. Air Flow | | | |
|---|---|---|---|
| Meters per Second | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 43.4°C/W | 37.9°C/W | 34.0°C/W |

# Transistor Count

The transistor count for the 845252 is: 3064

# Package Outline and Package Dimensions
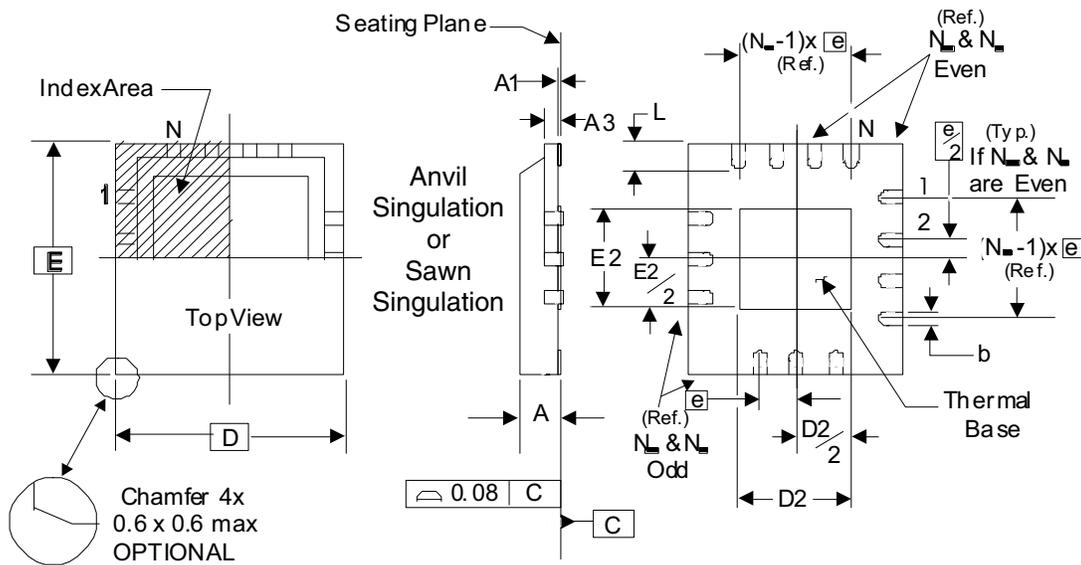
### Package Outline - K Suffix for VFQFN Packages



**NOTE:** The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pin-out are shown on the front page. The package dimensions are in Table 9.

**Table 9. Package Dimensions**

| JEDEC Variation: VHHD-2/-4 All Dimensions in Millimeters | | | |
|---|---|---|---|
| **Symbol** | **Minimum** | **Nominal** | **Maximum** |
| **N** | | 32 | |
| **A** | 0.80 | | 1.00 |
| **A1** | 0 | | 0.05 |
| **A3** | | 0.25 Ref. | |
| **b** | 0.18 | 0.25 | 0.30 |
| **N$_D$ & N$_E$** | | | 8 |
| **D & E** | | 5.00 Basic | |
| **D2 & E2** | 3.0 | | 3.3 |
| **e** | | 0.50 Basic | |
| **L** | 0.30 | 0.40 | 0.50 |

Reference Document: JEDEC Publication 95, MO-220

**Table 10. Ordering Information**

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|---|---|---|---|---|
| 845252AKILF | ICS45252AIL | Lead-Free, 32 Lead VFQFN | Tray | -40°C to 85°C |
| 845252AKILFT | ICS45252AIL | Lead-Free, 32 Lead VFQFN | Tape & Reel | -40°C to 85°C |

# Revision History Sheet

| Rev | Table | Page | Description of Change | Date |
|---|---|---|---|---|
| A | | 1 | Product Discontinuation Notice - Last time buy expires November 2, 2016.<br>PDN# CQ-15-05 | 11/6/15 |
| B | T10 | 16 | Obsolete datasheet per PDN# CQ-15-05.<br>Ordering Information table - deleted Tape & Reel count and table note.<br>Updated datasheet header/footer. | 11/11/16 |
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