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## M32C/80 Series

### Using DMAC II (Single Transfer)

#### 1. Abstract

This application note describes how to use DMAC II in single transfer mode.

#### 2. Introduction

The explanation of this issue is applied to the following condition:

Applicable MCU: M32C/80 Series

This program can also be used when operating other microcomputers within the M16C family, provided they have the same SFR (Special Function Registers) as the M32C/85 microcomputers. However, some functions may have been modified.

Refer to the User's Manual for details. Use functions covered in this Application Note only after careful evaluation.

#### 3. Detailed description

The following explains a method for transferring data from memory to memory by means of a DMAC II transfer when the cause of an interrupt with priority level 7 has occurred.

##### 3.1. DMAC II Transfer Mode

This application note example offers functions of single transfer mode shown in Table 1.

**Table 1. Selectable functions in single transfer mode**

Item	Definition	Selection
Transfer Block	8 bits	Yes
	16 bits	
Transfer Data	Immediate data	
	Data in memory	Yes
Source Direction	Fixed address	
	Forward address	Yes
Destination Direction	Fixed address	Yes
	Forward address	
Calculation Transfer Function	Without Calculation Transfer Function	Yes
	With Calculation Transfer Function	
End-of-Transfer Interrupt	Interrupts not used	Yes
	Interrupts used	
Chained Transfer Function	Not chain transferred	Yes
	Chain transferred	

### 3.2. DMAC II Index

The DMAC II index is configured with 8 bytes when interrupts and chain transfers are not used in single transfer mode. The DMAC II index must be located on the RAM area.

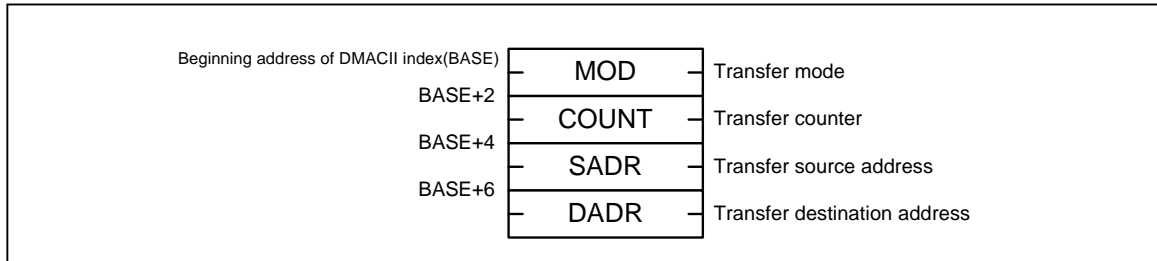


Figure 1.DMAC II Index

### 3.3. DMAC II Transfer

The interrupt requests from all peripheral functions whose ILVL2–ILVL0 bits in the interrupt control register have been set to “111b” constitute the cause of requests to DMAC II. In this application note, the INT0 interrupt is used for the cause of DMAC II request.

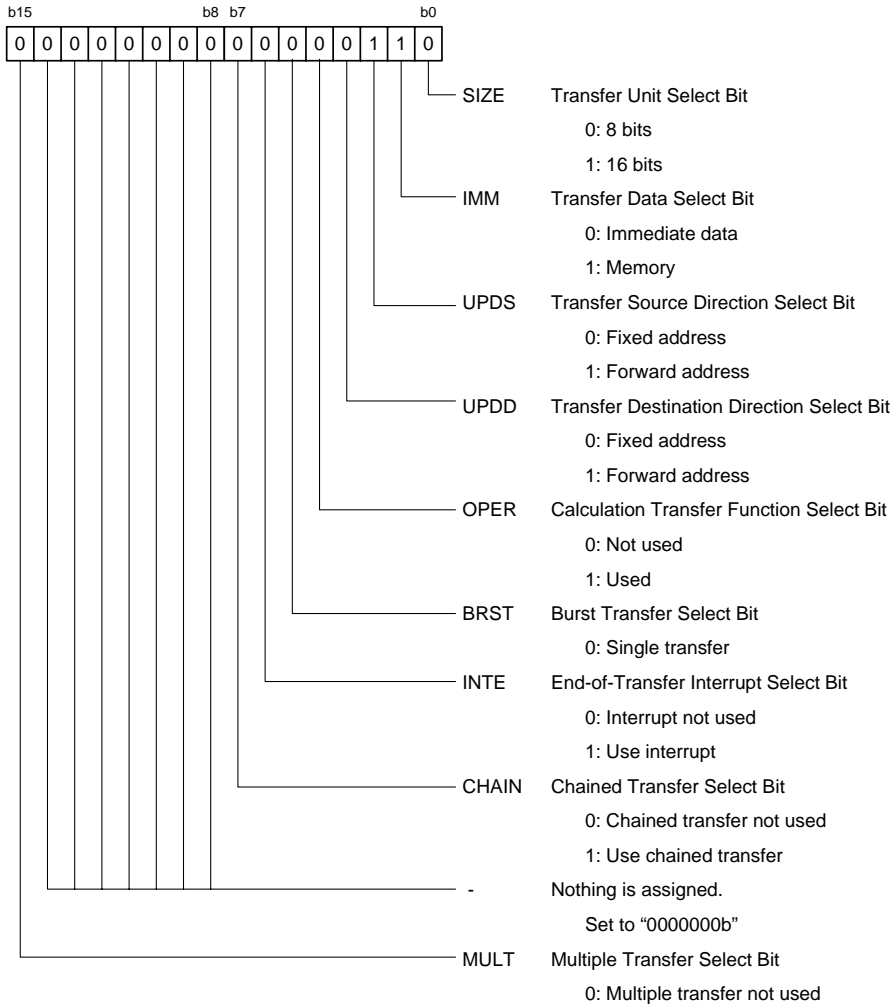
### 3.4. Setting Up the Variable Vector Table

Set the beginning address of the DMAC II index in the interrupt vector for the peripheral function interrupt that constitutes the cause of DMAC II request.

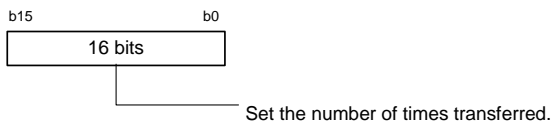
### 3.5. Register setting

To enable the operation defined in "Section 3. Detailed description", the following register settings must be taken place step by step. For detail configuration of each register, please refer to M32C/80 Series HARDWARE MANUAL.

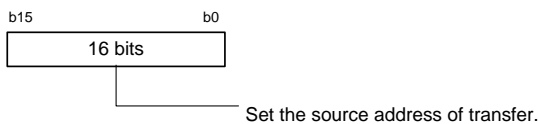
(1) Transfer mode (MOD)



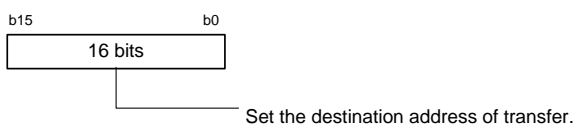
(2) Transfer count (COUNT)



(3) Transfer source address (SADR)



(4) Transfer destination address (DADR)





#### 4. Example of a Sample Program

```

/*****
/* FILENAME: rej05b0508_src.c
/* Ver : 1.00
/* FUNCTION: DMAII (Single Transfer)
/*****
/*****
/* include file
/*****
#include <stdio.h>
#include "sfr32c83.h"

/*****
/* DMAII Set
/*****
struct{
    union {
        struct{
            char    size:1;        /* Transfer Unit Select Bit */
            char    imm:1;        /* Transfer Data Select Bit */
            char    upds:1;       /* Transfer Source Direction Select Bit */
            char    updd:1;       /* Transfer Destination Direction Select Bit */
            char    oper:1;       /* Calculation Transfer Function Select Bit */
            char    brst:1;       /* Burst Transfer Select Bit */
            char    inte:1;       /* End-of-Transfer Interrupt Select Bit */
            char    chain:1;      /* Chained Transfer Select Bit */
            char    reserve:7;
            char    mult:1;       /* Multiple Transfer Select Bit */
        }bit;
        unsigned short    all;
    }mod;
    unsigned short count;      /* Transfer count */
    unsigned char near *sadr;  /* Transfer source address */
    unsigned char near *dadr;  /* Transfer destination address */
}dm_index;

/* Transfer data array */
static unsigned char near data[5] = {0x11,0x22,0x33,0x44,0x55};
/* Transfer destination memory */
static unsigned char near dest;

/*****
/* main
/*****
void main(void){
    asm(" fclr i "); /* Interrupt disable */
    /* DMAII setting */
    dm_index.mod.all = 0x0006; /* b0 = Transfer Unit:      8bit */
                                /* b1 = Transfer Data:      Memory */
                                /* b2 = Transfer Source:    Forward */
                                /* b3 = Transfer Destination: Fixed */
                                /* b4 = Calculation Transfer: None */
                                /* b5 = Burst Transfer:      Single */
                                /* b6 = Interrupt:          None */
                                /* b7 = Chained Transfer:    None */
                                /* b8 - b14 = Reserved (all "0") */
                                /* b15 = Multiple Transfer:   None */

    dm_index.count = 5;        /* number of transfer = 5 */
    dm_index.sadr = data;     /* Source of transfer = beginning address of the data array */
    dm_index.dadr = &dest;    /* Destination of transfer = Destination address */

    /* Set the interrupt used for DMAC II */
    rlv1 = 0x20;             /* Interrupt priority level 7 is used for DMAC II transfers */

    int0ic = 0x07;          /* INTO interrupt level 7 (used for DMAII) */

    while(1);
}

```

## 5. Relocatable Vector Tables

```

;-----
; variable vector section
;-----
        .section vector,ROMDATA          ; variable vector table
        .org      VECTOR_ADR

        .word     dummy_int             ; BRK (software int 0)
        .word     dummy_int             ;
        .word     dummy_int             ;
        .word     dummy_int             ;
        .word     dummy_int             ;
        .word     dummy_int             ;
        .word     dummy_int             ;
        .word     dummy_int             ; DMA0 (software int 8)

;
;
;                (Omission)
;
;
        .word     dummy_int             ; INT5 (software int 26)
        .word     dummy_int             ; INT4 (software int 27)
        .word     dummy_int             ; INT3 (software int 28)
        .word     dummy_int             ; INT2 (software int 29)
        .word     dummy_int             ; INT1 (software int 30)
        .glb     _dm_index
        .word     _dm_index             ; INT0 (software int 31)
        .word     dummy_int             ; TIMER B5 (software int 32)

;
;
;                (Omission)
;
;

```



6. Reference

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Hardware Manual

M32C/80 Group Hardware Manual

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## REVISION HISTORY

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		Page	Summary
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