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R8C/25 Group

Timer RA in Pulse Period Measurement Mode

1. Abstract

This document describes a program for timer RA in pulse period measurement mode.

2. Introduction

The application example described in this document applies to the following MCU and parameter(s):

- MCU : R8C/25 Group

This program can be used with other R8C/Tiny Series MCUs which have analogous special function registers (SFRs) as the R8C/25 Group. Check the manual for any additions and modifications to functions. Careful evaluation is recommended before using this application note.

3. Application Example Description

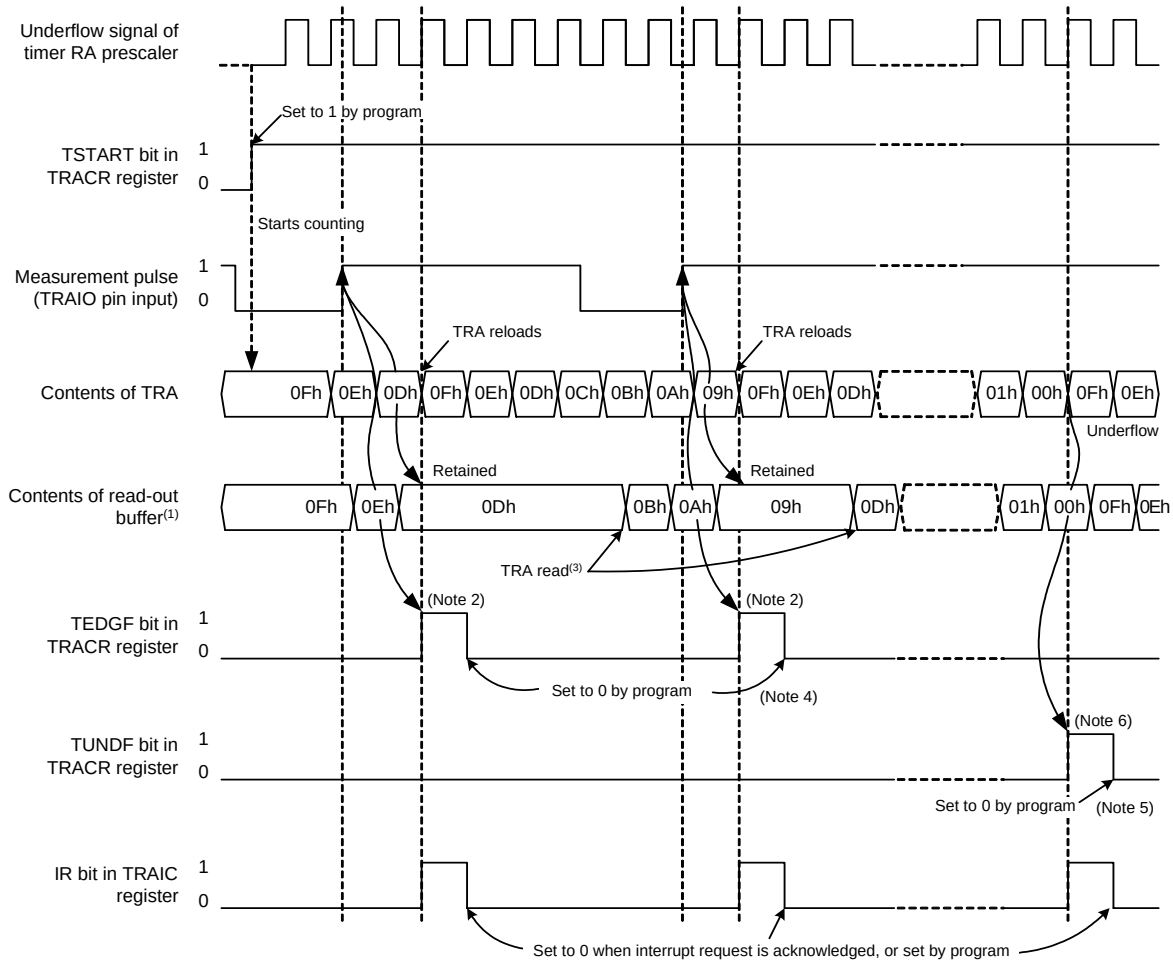
In pulse period measurement mode, the pulse period of an external signal input from the $\overline{\text{INT1}}$/TRAIO pin is measured.

The setting conditions for this program are as follows:

- Count source :f8
- Measurement period :The period from one rising edge to the next rising edge of the measured pulse
- Input pin :$\overline{\text{INT1}}$/TRAIO pin (P1_7)
- TRAIO input filter :No filter
- Timer RA prescaler underflow period :10 μs

40 MHz (fOCO) × f2 (FRA2) × f8 (TCK0 to TCK2) × 25 (TRAPRE register) = 10 μs

Figure 3.1 shows an Operating Example in Pulse Period Measurement Mode.



The period from one rising edge to the next rising edge of the measured pulse is measured (TEDGSEL = 0) with the default value of the TRA register as 0Fh.

NOTES:
1. The contents of the read-out buffer can be read by reading the TRA register in pulse period measurement mode.
2. After an active edge of the measured pulse is input, the TEDGF bit in the TRACR register is set to 1 (active edge found) when the timer RA prescaler underflows for the second time.
3. The TRA register should be read before the next active edge is input after the TEDGF bit is set to 1 (active edge found). The contents in the read-out buffer are retained until the TRA register is read. If the TRA register is not read before the next active edge is input, the measured result of the previous period is retained.
4. To set to 0 by a program, use a MOV instruction to write 0 to the TEDGF bit in the TRACR register. At the same time, write 1 to the TUNDF bit in the TRACR register.
5. To set to 0 by a program, use a MOV instruction to write 0 to the TUNDF bit. At the same time, write 1 to the TEDGF bit.
6. Bits TUNDF and TEDGF are both set to 1 if timer RA underflows and reloads on an active edge simultaneously.

Figure 3.1 Operating Example in Pulse Period Measurement Mode

This sample program may include bit operations of unused functions for the SFR bit layout. Set these values according to the operating conditions of the user system.

3.1 Pin Used

Table 3.1 Pin Used and Its Function

Pin	I/O	Function
P1_7/TRAIO/$\overline{\text{INT1}}$	Input	Measurement pulse input

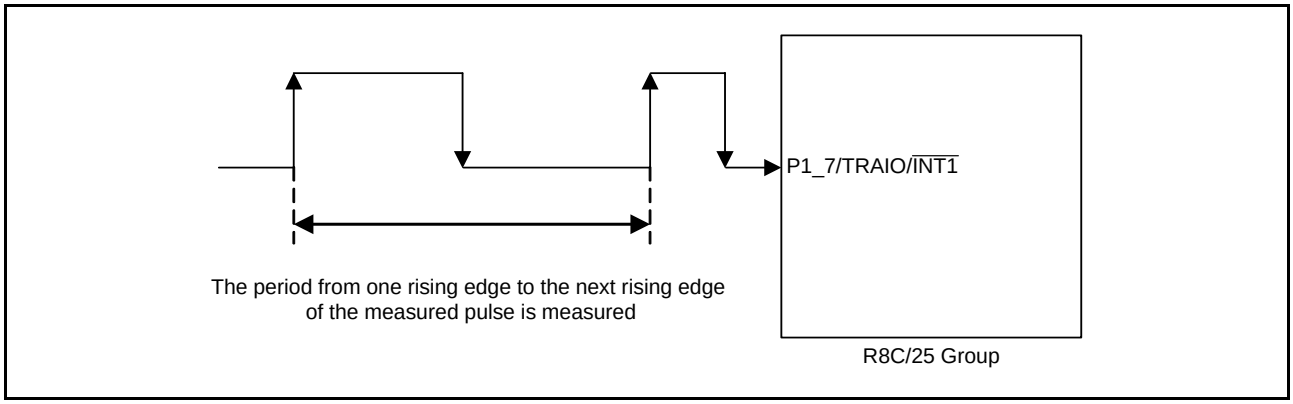


Figure 3.2 Pin Used

3.2 Memory Usage

Table 3.2 Memory Usage

Memory Usage	Size	Remarks
ROM	246 bytes	In main.c module
RAM	5 bytes	In main.c module
Maximum user stack usage	10 bytes	main function: 7 bytes timer_ra_init function: 3 bytes
Maximum interrupt stack usage	18 bytes	TRA_int function: 18 bytes

Memory usage varies depending on the C compiler version and the compile option.
The above applies under the following conditions:

- C compiler: M16C/60, 30, 20, 10, Tiny, R8C/Tiny Series Compiler V.5.40 Release 00
- Compile option: -c -finfo; NOTE: -dir “$(CONFIGDIR)” -R8C

NOTE: Unavailable in the R8C/Tiny-exclusive free version.

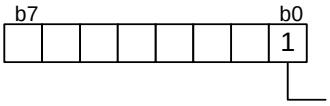
4. Setup

This section shows the initial setting procedures and values to perform the example described in **3. Application Example Description**. Refer to the **R8C/25 Group Hardware Manual** for details on individual registers.

4.1 System Clock Setting

(1) Enable writing to registers CM0, CM1, OCD, FRA0, FRA1, and FRA2.

Protect Register



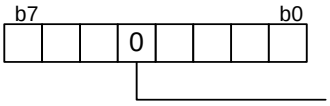
PRCR [Address 000Ah]

PRC0 Protect bit 0

Writing to registers CM0, CM1, OCD, FRA0, FRA1, and FRA2 enabled

(2) Start the low-speed on-chip oscilltor.

System Clock Control Register 1



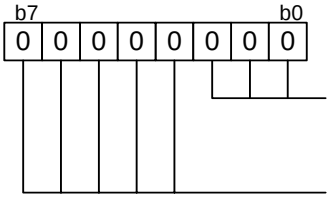
CM1 [Address 0007h]

CM14 Low-speed on-chip oscillator oscillation stop bit

Low-speed on-chip oscillator oscillates

(3) Set the division ratio of the high-speed on-chip oscillator clock.

High-Speed On-Chip Oscillator Control Register 2



FRA2 [Address 0025h]

FRA22 to FRA20 High-speed on-chip oscillator frequency switch bit

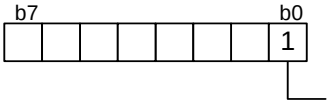
Divide-by-2 mode

($\overline{\text{b7-b3}}$) Reserved bits

Set to 0.

(4) Start the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0



FRA0 [Address 0023h]

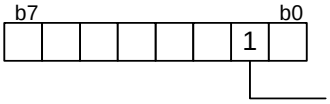
FRA00 High-speed on-chip oscillator enable bit

High-speed on-chip oscillator oscillates

(5) Wait until oscillation stabilizes.

(6) Select the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0



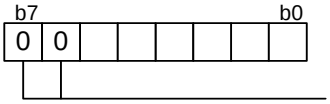
FRA0 [Address 0023h]

FRA01 High-speed on-chip oscillator select bit

High-speed on-chip oscillator selected

(7) Set system clock division select bits 1.

System Clock Control Register 1



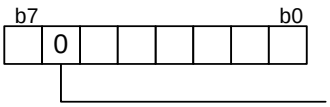
CM1 [Address 0007h]

CM17 and CM16 System clock division select bits 1

No division mode

(8) Set system clock division select bit 0.

System Clock Control Register 0



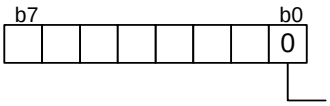
CM0 [Address 0006h]

CM06 System clock division select bit 0

CM16 and CM17 enabled

(9) Disable writing to registers CM0, CM1, OCD, FRA0, FRA1, and FRA2.

Protect Register



PRCR [Address 000Ah]

PRC0 Protect bit 0

Writing to registers CM0, CM1, OCD, FRA0, FRA1, and FRA2 disabled

4.2 Pulse Period Measurement Mode Setting

(1) Set the port P1 direction register.

Port P1 Direction Register

b7							b0
0							

PD1 [Address 00E3h]

PD1_7 Port P1_7 direction bit
Input mode

(2) Stop the timer RA count.

Timer RA Control Register

b7							b0
							0

TRACR [Address 0100h]

TSTART Timer RA count start bit
Count stops

(3) Wait until the TCSTF bit in the TRACR register is set to 0.

(4) Set the timer RA interrupt control register (timer RA interrupt disabled).

Timer RA Interrupt Control Register

b7							b0
0	0	0	0	0	0	0	0

TRAIC [Address 0056h]

ILVL2 to ILVL0 Interrupt priority level select bits 2 to 0
Level 0 (interrupt disabled)

IR Interrupt request bit
No interrupt request

($\overline{b7}$-$\overline{b4}$) Nothing is assigned.
Set to 0.

(5) Forcibly stop the timer RA count.

Timer RA Control Register

b7							b0
					1		

TRACR [Address 0100h]

TSTOP Timer RA count forcible stop bit
Count forcibly stopped

(6) Set the timer RA prescaler register.

Timer RA Prescaler Register

b7							b0
0	0	0	1	1	0	0	0

TRAPRE [Address 0103h]

Timer RA underflow period setting
25 – 1 (0 x 18) setting

(7) Set the timer RA register.

Timer RA Register

b7							b0
1	1	1	1	1	1	1	1

TRA [Address 0104h]

Timer RA register initial value setting
0xFF setting

(8) Set the timer RA control register.

Timer RA Control Register

b7							b0
0	0	0	0	0	0	0	0

TRACR [Address 0100h]

TSTART Timer RA count start bit
Count stops

TCSTF Timer RA count status flag
Unavailable. Set to 0.

TSTOP Timer RA count forcible stop bit
Unavailable. Set to 0.

($\overline{b3}$) Nothing is assigned.
Set to 0.

TEDGF Timer RA edge judgment flag
No active edge

TUNDF Timer RA underflow flag
No underflow

($\overline{b7}$-$\overline{b6}$) Nothing is assigned.
Set to 0.

(9) Set the timer RA I/O control register.

Timer RA I/O Control Register

b7	b6	b5	b4	b3	b2	b1	b0	
0	0	0	0	0	0	0	0	TRAIOC [Address 0101h]

TEDGSEL	TRAIO polarity switch bit The period from one rising edge to the next rising edge of the measured pulse is measured.
TOPCR	TRAIO output control bit Set to 0 in pulse period measurement mode.
TOENA	TRAO output enable bit Set to 0 in pulse period measurement mode.
TIOSEL	$\overline{INT1}$/TRAIO select bit $\overline{INT1}$/TRAIO pin (P1_7)
TIPF1 and TIPF0	TRAIO input filter select bits No filter
($\overline{b7}$-$\overline{b6}$)	Nothing is assigned. Set to 0.

(10) Set the timer RA mode register.

Timer RA Mode Register

b7	b6	b5	b4	b3	b2	b1	b0	
0	0	0	1	0	1	0	0	TRAMR [Address 0102h]

TMOD2 to TMOD0	Timer RA operating mode select bits Pulse period measurement mode
($\overline{b3}$)	Nothing is assigned. Set to 0.
TCK2 to TCK0	Timer RA count source select bit f8 selected
TCKCUT	Timer RA count source cutoff bit Count source provided

(11) Set the timer RA interrupt control register.

Timer RA Interrupt Control Register

b7							b0
0	0	0	0	0	1	1	1

TRAIC [Address 0056h]

ILVL2 to ILVL0 Interrupt Priority Level Select Bits 2 to 0
Level 7

IR Interrupt request bit
No interrupt request

(b7-b4) Nothing is assigned.
Set to 0.

(12) Start the timer RA count.

Timer RA Control Register

b7							b0
							1

TRACR [Address 0100h]

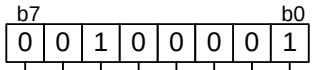
TSTART Timer RA count start bit
Count starts

(13) Wait until the TCSTF bit in the TRACR register is set to 1.

(14) Immediately after the count starts, allow two cycles or more of the timer RA prescaler.

(15) Set the TEDGF bit in the TRACR register to 0 before use.

Timer RA Control Register



TRACR [Address 0100h]

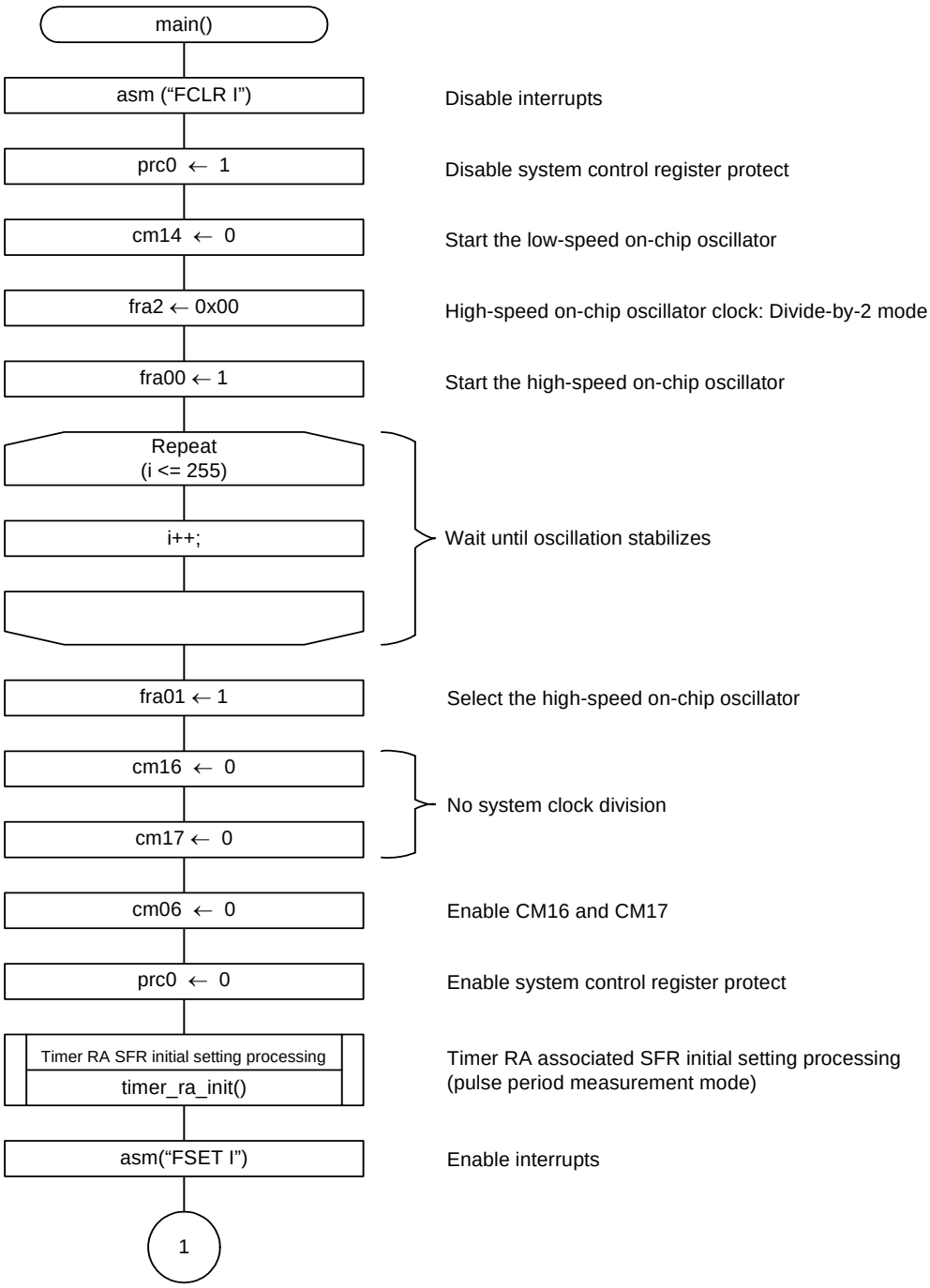
TSTART	Timer RA count start bit Count starts
TCSTF	Timer RA count status flag Unavailable. Set to 0.
TSTOP	Timer RA count forcible stop bit Unavailable. Set to 0.
($\overline{b3}$)	Nothing is assigned. Set to 0.
TEDGF	Timer RA edge judgment flag No active edge
TUNDF	Timer RA underflow flag No underflow
($\overline{b7}$-$\overline{b6}$)	Nothing is assigned. Set to 0.

NOTE:
In pulse width measurement mode and pulse period measurement mode, use the MOV instruction to set the TRACR register. Write 1 to bits TEDGF and TUNDF to avoid their values being changed.

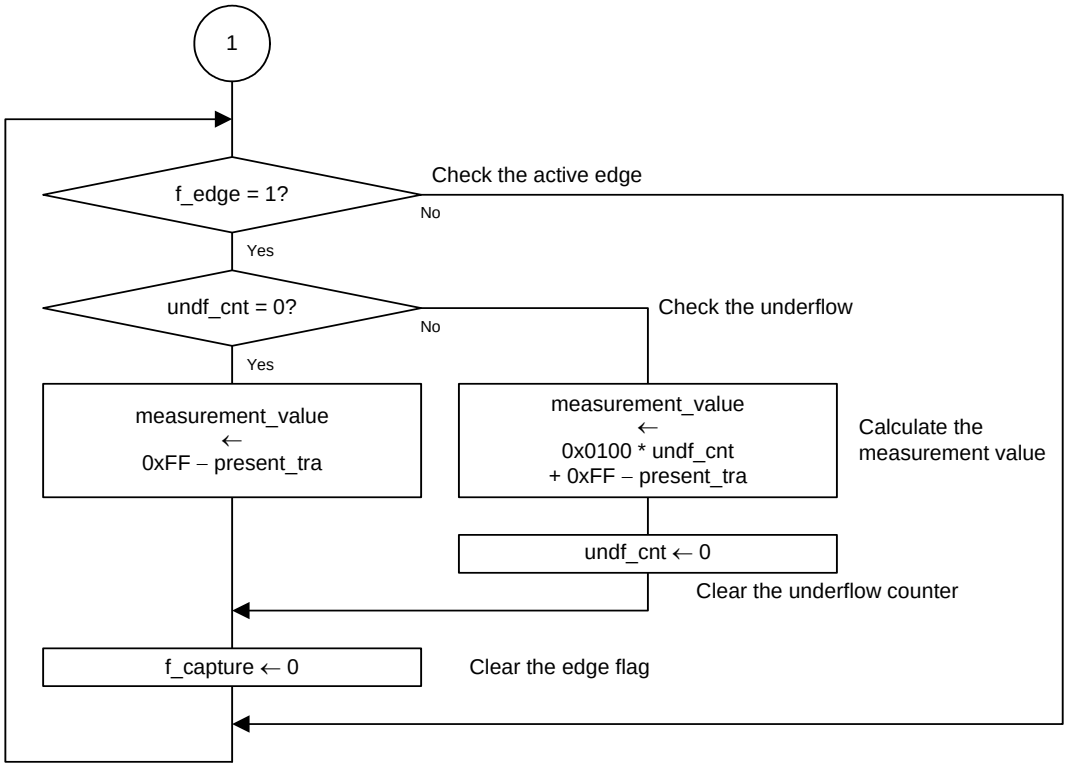
5. Flowchart

5.1 Main Function

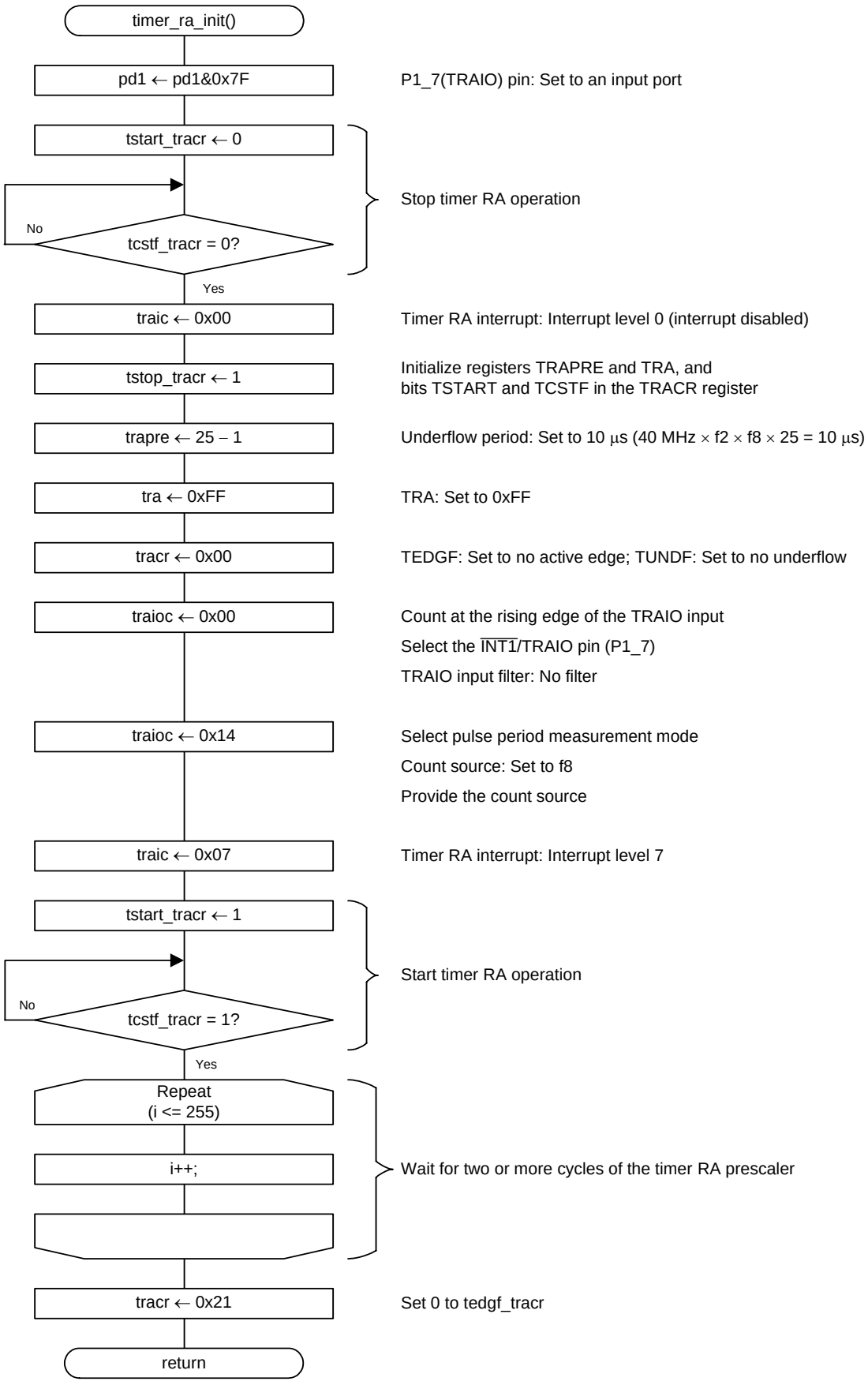
5.1.1 Main Function 1



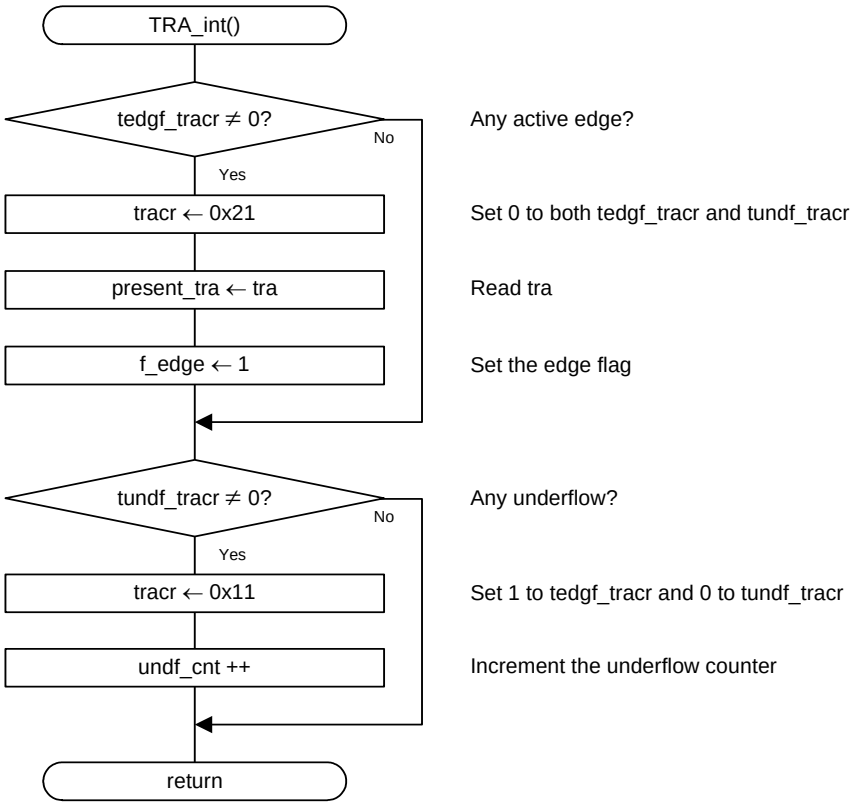
5.1.2 Main Function 2



5.2 Timer RA Associated SFR Initial Setting Processing



5.3 Timer RA Interrupt Handling



6. Sample Programming Code

A sample program can be downloaded from the Renesas Technology website.
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7. Reference Documents

Hardware Manual
R8C/25 Group Hardware Manual
The latest version can be downloaded from the Renesas Technology website.

Technical Update/Technical News
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REVISION HISTORY	R8C/25 Group Timer RA in Pulse Period Measurement Mode

Rev.	Date	Description	
		Page	Summary
1.00	Sep 15, 2006	–	First Edition issued
2.00	June 29, 2007	2 to 4	3. Application Example Description modified
		5 to 11	4. Setup SFR setting procedures added
		12	5.1.1 Main Function 1 Oscillation stabilization processing added
		13	5.1.2. Main Function 2 Pulse period measurement calculation processing added
		14	5.2 Timer RA Associated SFR Initial Setting Processing modified
		15	5.3 Timer RA Interrupt Handling added

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