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M32C/84 Group

Stop Mode Set-Up

1. Abstract

Setting and operation for entering stop mode are described here. Figure 1 shows the set-up procedure.
A reference program is an example when using the INT0 interrupt for a return factor from stop mode.

2. Introduction

This application note is applied to the M32C/84 group Microcomputers.

This program can be operated under the condition of M16C family products with the same SFR(Special Function Register) as M32C/84 Group products. Because some functions may be modified of the M16C family products, see the user's manual. When using the functions shown in this application note, evaluate them carefully for an operation.

3. Set-up

- Initial Setting

(1) Set each interrupt priority level after setting the exit priority level, required to exit stop mode, controlled by the RLVL2 to RLVL0 bits in the RLVL register, to ”7”

- Before Entering Stop Mode

(2) Set the I flag to “0”
(3) Set the interrupt priority level of the interrupt being used to exit stop mode
(4) Set the interrupt priority levels of the interrupts, not being used to exit stop mode, to “0”
(5) Set IPL in the FLG register. Then set the exit priority level to the same level as IPL
Interrupt priority level of the interrupt used to exit stop mode > IPL = the exit priority level
(6) Set the PRC0 bit in the PRCR register to “1” (write enable)
(7) Select the main clock as the CPU clock
- When the CPU clock source is the sub clock
(a) set the CM05 bit in the CM0 register to “0” (main clock oscillates)
(b) set the CM07 bit in the CM0 register to “0” (clock selected by the CM21 bit divided by MCD register setting)
- When the CPU clock source is the PLL clock
(a) set the CM17 bit in the CM1 register to “0” (main clock)
(b) set the PLC07 bit in the PLC0 register to “0” (PLL off)
- When the CPU clock source is the on-chip oscillator clock
(a) set MCD4 to MCD0 bits to “01000_2” (divide-by-8 mode)
(b) set the CM05 bit to “0” (main clock oscillates)
(c) set the CM21 bit in the CM2 register to “0” (clock selected by the CM17 bit)
- When main clock direct mode is used
(a) set the PRC1 bit in the PRCR register to “1” (write enable)
(b) set the PM24 bit in the PM2 register to “0” (clock selected by the CM07 bit)
(8) The oscillation stop detect function is used, set the CM20 bit in the CM2 register to “0” (oscillation stop detect function disabled)
(9) Set the I flag to “1”
(10) Set the CM10 bit to “1” (all clock stops)

- After Exiting Stop Mode

(11) Set the exit priority level to “7” as soon as exiting stop mode

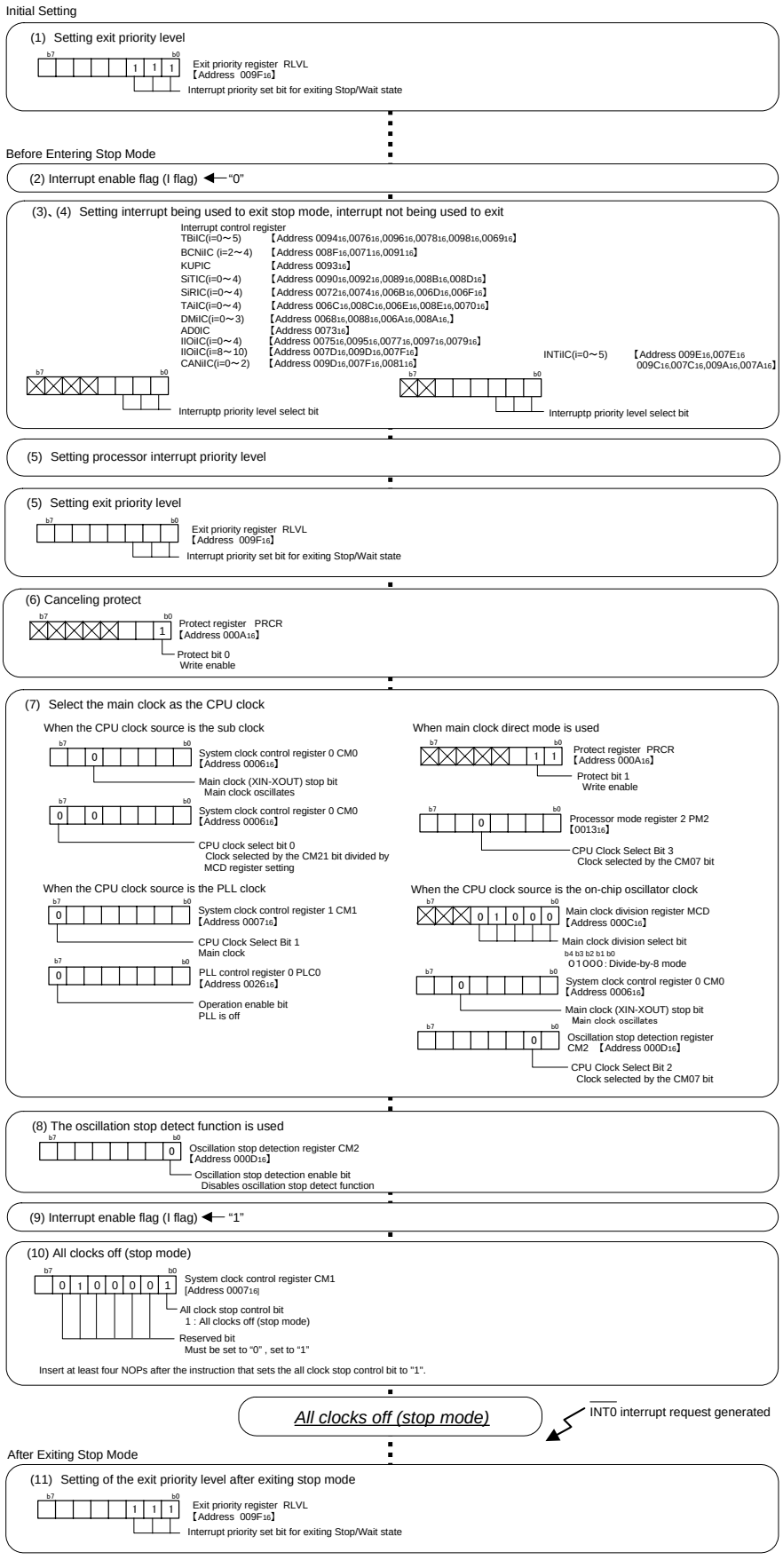

Figure 1. Example of stop mode set-up

4. The example of reference program

```
;******************************************************************************
;
;    M32C/84 Program Collection
;
;    FILE NAME : rjj05b0765_src.a30
;    CPU       : M32C/84 Group
;    FUNCTION  : Stop Mode Set-up
;    HISTORY   : 2005.4.7   Ver 1.00
;
;    Copyright(C)2005, Renesas Technology Corp.
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;
;******************************************************************************
;******************************************************************************
;         Include
;******************************************************************************
;
        .LIST       off                 ;Stops outputting lines to the assembler list file
        .INCLUDE    sfr32c84.inc        ;Reads the file that defined SFR
        .LIST       on                  ;Starts outputting lines to the assembler list file
;
;******************************************************************************
;         Symbol definition
;******************************************************************************
;
RAM_TOP             .equ    000400h     ;Start address of RAM
RAM_END             .equ    002affh     ;End address of RAM
ROM_TOP             .equ    0fe0000h    ;Start address of ROM
VECT_TOP            .equ    0fffe00h    ;Start address of vect_top
FIXED_VECT_TOP      .equ    0ffffdch    ;Start address of fixed_vect_top
;
;******************************************************************************
;         Program area
;******************************************************************************
;==============================================================================
;         Start up
;==============================================================================
        .SECTION    PROGRAM, CODE       ;Declares section name and section type
        .ORG        ROM_TOP             ;Declares start address
START:
        ldc         #RAM_END+1,isp      ;Sets interrupt stack pointer
        mov.b       #03h, prcr          ;Removes protect
        mov.b       #00000000b, pm0     ;Single-chip mode
        mov.b       #00000000b, pm1     ;
```

```
        mov.b       #00001000b, cm0         ;Xcin-Xcout High
        mov.b       #00100000b, cm1         ;
        mov.b       #00010010b, mcd         ;No division mode
        mov.b       #00h, prcr              ;Protects all registers
        ldc         #VECT_TOP,intb          ;Sets interrupt table register
;
;=========================================================================
;         Main program
;=========================================================================
MAIN:
;
        mov.b       #00000111b,rlvl         ;M16C-97-0303(Japanese) countermeasure
;                           | | |           ;M16C-97-0307(Engish) countermeasure
;                           | | |           ;Exit priority register
;                           +++-----------------;Interrupt priority set bit for exiting stop/wait state
                                            ;(111:Level 7, interrupt disabled)
STOP_MODE:
        fclr        i                       ;Clear interrupt enable flag
        mov.b       #00000101b,int0ic       ;Interrupt control register
;                           | +++-----------------;Interrupt priority level select bit
;                           |               ;(101:Level 5, interrupt disabled)
;                           +-------------------------;Interrupt request bit (0:Interrupt not requested)
        ldipl       #3                      ;Intterrupt permission level: 3
        mov.b       #00000011b,rlvl         ;Exit priority register
;                            +++-----------------;Interrupt priority set bit for exiting stop/wait state
                                            ;(011:Level 3, interrupt disabled)
        fset        i                       ;Set interrupt enable flag
;
        mov.b       #00000001b,prcr         ;Removes protect
        bset        cm10                    ;Stop mode
        mov.b       #00000000b,prcr         ;Protects all registers
        jmp.b       MAIN_A                  ;TN-16C-124A/JA(Japanese) countermeasure
;                                           ;TN-16C-124A/EA(English) countermeasure
MAIN_A:
;
        nop
        nop
        nop
        nop
;
MAIN_B:
;
        jmp         MAIN_B
;
;=========================================================================
;         Interrupt program
;=========================================================================
```

```
INT0_INT:
;
        mov.b           #00000111b,rlvl         ;Exit priority register
;                               +++-------------------;Interrupt priority set bit for exiting stop/wait state
                                                        ;(111:Level 7, interrupt disabled)
;
                reit
;
;=============================================================================
;       Dummy interrupt processing program
;=============================================================================
DUMMY:
                reit
;
;*****************************************************************************
;       Setting of variable vector table
;*****************************************************************************
;
        .SECTION        VECT,ROMDATA
        .ORG            VECT_TOP + (8*4)
;
        .lword                  DUMMY           ;DMA0 interrupt vector
        .lword                  DUMMY           ;DMA1 interrupt vector
        .lword                  DUMMY           ;DMA2 interrupt vector
        .lword                  DUMMY           ;DMA3 interrupt vector
        .lword                  DUMMY           ;TA0 interrupt vector
        .lword                  DUMMY           ;TA1 interrupt vector
        .lword                  DUMMY           ;TA2 interrupt vector
        .lword                  DUMMY           ;TA3 interrupt vector
        .lword                  DUMMY           ;TA4 interrupt vector
        .lword                  DUMMY           ;UART0 transmit/NACK interrupt vector
        .lword                  DUMMY           ;UART0 receive/ACK interrupt vector
        .lword                  DUMMY           ;UART1 transmit/NACK interrupt vector
        .lword                  DUMMY           ;UART1 receive/ACK interrupt vector
        .lword                  DUMMY           ;TB0 interrupt vector
        .lword                  DUMMY           ;TB1 interrupt vector
        .lword                  DUMMY           ;TB2 interrupt vector
        .lword                  DUMMY           ;TB3 interrupt vector
        .lword                  DUMMY           ;TB4 interrupt vector
        .lword                  DUMMY           ;INT5 interrupt vector
        .lword                  DUMMY           ;INT4 interrupt vector
        .lword                  DUMMY           ;INT3 interrupt vector
        .lword                  DUMMY           ;INT2 interrupt vector
        .lword                  DUMMY           ;INT1 interrupt vector
        .lword                  INT0_INT        ;INT0 interrupt vector
        .lword                  DUMMY           ;TB5 interrupt vector
        .lword                  DUMMY           ;UART2 transmit/NACK interrupt vector
```

```
        .lword                  DUMMY       ;UART2 receive/ACK interrupt vector
        .lword                  DUMMY       ;UART3 transmit/NACK interrupt vector
        .lword                  DUMMY       ;UART3 receive/ACK interrupt vector
        .lword                  DUMMY       ;UART4 transmit/NACK interrupt vector
        .lword                  DUMMY       ;UART4 receive/ACK interrupt vector
        .lword                  DUMMY       ;Bus collision detection,start/stop
                                            ;condition detection (UART2) interrupt vector
        .lword                  DUMMY       ;Bus collision detection,start/stop
                                            ;condition detection (UART3) interrupt vector
        .lword                  DUMMY       ;Bus collision detection,start/stop
                                            ;condition detection (UART4) interrupt vector
        .lword                  DUMMY       ;A-D interrupt vector
        .lword                  DUMMY       ;KEY interrupt vector
        .lword                  DUMMY       ;IntelligentI/O interrupt vector0
        .lword                  DUMMY       ;IntelligentI/O interrupt vector1
        .lword                  DUMMY       ;IntelligentI/O interrupt vector2
        .lword                  DUMMY       ;IntelligentI/O interrupt vector3
        .lword                  DUMMY       ;IntelligentI/O interrupt vector4
        .lword                  DUMMY       ;IntelligentI/O interrupt vector8
        .lword                  DUMMY       ;IntelligentI/O interrupt vector9,CAN0
        .lword                  DUMMY       ;IntelligentI/O interrupt vector10,CAN1
        .lword                  DUMMY       ;CAN2
;
;*****************************************************************************
;           Setting of fixed vector
;*****************************************************************************
;
        .SECTION        F_VECT,ROMDATA
        .ORG            FIXED_VECT_TOP
;
        .lword                  DUMMY       ;Undefined instruction interrupt vector
        .lword                  DUMMY       ;Overflow (INTO instruction) interrupt vector
        .lword                  DUMMY       ;BRK instruction interrupt vector
        .lword                  DUMMY       ;Address match interrupt vector
        .lword                  DUMMY       ;
        .lword                  DUMMY       ;Watchdog timer interrupt vector
        .lword                  DUMMY       ;
        .lword                  DUMMY       ;NMI interrupt vector
        .lword                  START       ;Sets start vector
;
        .end
```

5. Referense

Hardware manual
M32C/84 group version Hardware Manual
(Use the latest on the web-site: http://www.renesas.com)

6. Web-site and contact for support

Renesas web-site
http://www.renesas.com/

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Revision

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