RZ/A2M Group

Example of booting from OctaFlash™ using SPI multi I/O bus controller

Introduction

This application note describes an example of booting from the OctaFlash via the SPI multi-I/O bus controller (hereinafter called "SPIBSC") of RZ/A2M by using the boot mode 4 (Octal-SPI flash boot 1.8V) function.

Products

RZ/A2M

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

1.1 Booting from OctaFlash

In boot mode 4, the RZ/A2M boots from the Octal-SPI flash memory allocated to the SPI multi-I/O bus space. This application note describes an example in which OctaFlash is used as the Octal-SPI flash memory to boot the RZ/A2M (hereinafter called "OctaFlash boot").

Figure 1.1 shows the Conceptual diagram of OctaFlash boot operation.

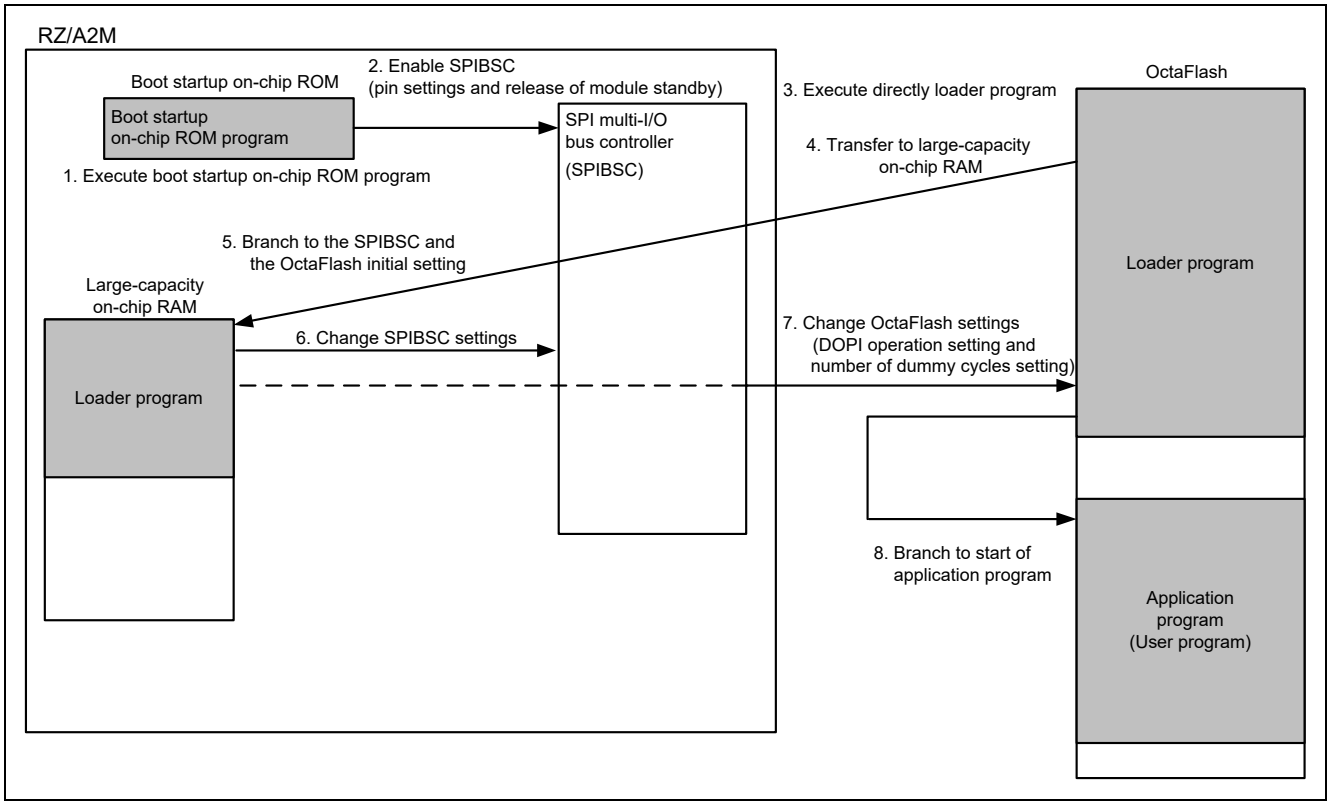


Figure 1.1 Conceptual diagram of OctaFlash boot operation

The conceptual diagram of OctaFlash boot operation is described below.

1 The RZ/A2M runs the boot startup on-chip ROM program after power-on reset is canceled.
2 When started up by OctaFlash boot, the boot startup on-chip ROM program sets the SPIBSC to external address space read mode to enable to directly run programs allocated to the SPI multi-I/O bus space.
3 Directly execute the loader program stored in the OctaFlash.
4 The loader program is transferred from the OctaFlash to the large-capacity on-chip RAM by section initialization of the loader program.
5 Branch to the SPIBSC and the OctaFlash initial setting transferred to the large-capacity on-chip RAM.
6 The loader program changes the SPIBSC settings.
7 The loader program changes the OctaFlash settings.
8 Execution branches to the start address of the application program.

The boot startup on-chip ROM program makes settings to allow common access to typical Octal-SPI flash memory devices, so it is necessary to provide the optimal settings to the Octal-SPI flash memory used by the customer. This application note describes how to allocate the loader program to the start address (H'2000_0000) of the SPI multi-I/O bus space branched by the boot startup on-chip ROM program, and then branch to the customer-created application program (user program) after the loader program are provided optimal settings to the OctaFlash used by the customer

1.2 Peripheral Functions Used

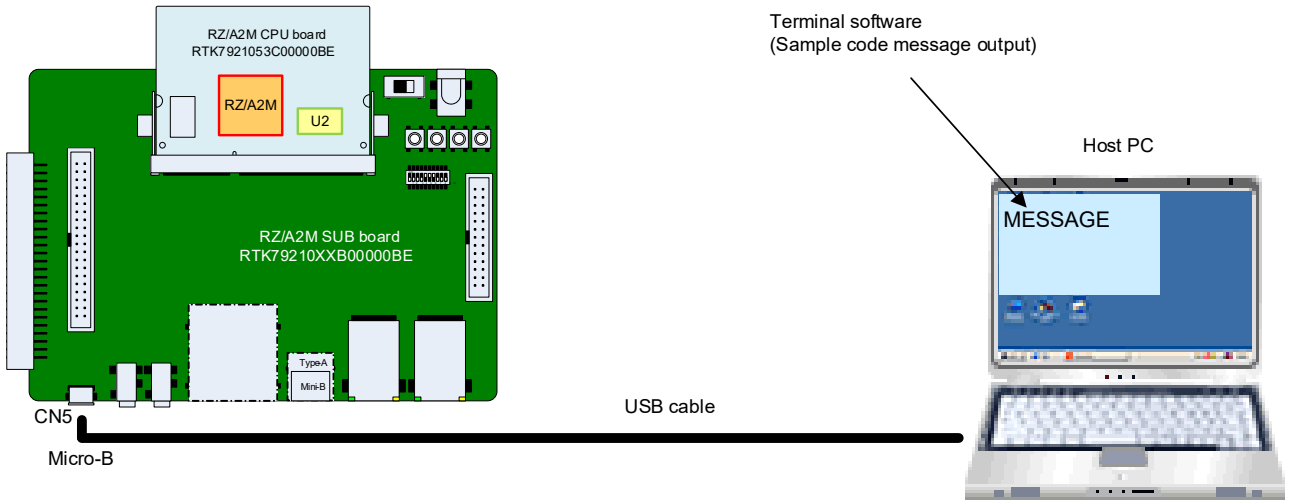
This sample code not only configures the SPIBSC but also initializes the clock pulse oscillator, interrupt controller, general-purpose input/output ports, memory management unit, primary cache (L1 cache), and secondary cache (L2 cache).

In this application note, the SPI multi-I/O bus controller is referred to as the SPIBSC, the Clock pulse generator as the CPG, the Interrupt controller as the INTC, the OS timer as the OSTM, the Serial communication interface with FIFO as the SCIFA, the General I/O ports as the GPIO, the Power-down modes as the STB, and the Memory management unit as the MMU.

Table 1.1 summarizes Peripheral functions and their applications, and Figure 1.2 shows Operating environment for the sample code.

Table 1.1 Peripheral functions and their applications

Peripheral Function	Application
SPI multi-I/O bus controller (SPIBSC)	When set to external address space read mode, it generates signals that enable the CPU to directly read from OctaFlash connected to the SPI multi-I/O bus space.
Clock pulse generator (CPG)	Generate the operating frequency of the RZ/A2M.
Interrupt controller (INTC)	Control OSTM channel 0, OSTM channel 2 and SCIFA channel 4 interrupts.
OS timer (OSTM)	Use OSTM channel 0 and channel 2 • Channel 0 Control the cycle for blinking LED • Channel 2 Use for time management by OS Abstraction Layer
Serial communication interface with FIFO (SCIFA)	Communicate between SCIFA channel 4 and the host PC.
General I/O ports (GPIO)	Switch multiplexed pin functions for SCIFA channel 4. Control pin for LED on/off.
Power-down modes (STB)	Cancel the module standby state of the RZ/A2M's peripheral I/O. Enable writing to the on-chip data retention RAM.
Memory management unit (MMU), L1 cache, and L2 cache	Generate conversion tables such as specifying valid area of L1 cache or specifying memory type in the RZ/A2M external address area. Enable the L1 and L2 caches.



Note: Since RTK7921053C00000BE is not equipped with OctaFlash, this sample code does not run on it as it is. Therefore, the serial flash memory for U2 of RTK7921053C00000BE is replaced with OctaFlash here so that this sample code can run on it.

Figure 1.2 Operating environment

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Confirmed operation conditions (1/2)

Item	Contents
MCU used	RZ/A2M
Operating frequency (Note)	CPU clock (Iϕ): 528MHz Image processing clock (Gϕ): 264MHz Internal bus clock (Bϕ): 132MHz Peripheral clock 1 (P1ϕ): 66MHz Peripheral clock 0 (P0ϕ): 33MHz QSPI0_SPCLK: 132MHz CKIO: 132MHz
Operating voltage	Power supply voltage (I/O): 3.3V Power supply voltage (1.8/3.3V switch I/O (PVcc_SPI)): 1.8V Power supply voltage (internal): 1.2V
Integrated development environment	e2 studio V7.8.0
C compiler	GNU Arm Embedded Toolchain 6-2017-q2-update
	Compiler option (addition of directory path excluded) Release configuration: -mcpu=cortex-a9 -march=armv7-a -marm -mlittle-endian -mfloat-abi=hard -mfpu=neon -mno-unaligned-access -Os -ffunction-sections -fdata-sections -Wunused -Wuninitialized -Wall -Wextra -Wmissing-declarations -Wconversion -Wpointer-arith -Wpadded -Wshadow -Wlogical-op -Waggregate-return -Wfloat-equal -Wnull-dereference -Wmaybe-uninitialized -Wstack-usage=100 -fabi-version=0 Hardware Debug configuration: -mcpu=cortex-a9 -march=armv7-a -marm -mlittle-endian -mfloat-abi=hard -mfpu=neon -mno-unaligned-access -Og -ffunction-sections -fdata-sections -Wunused -Wuninitialized -Wall -Wextra -Wmissing-declarations -Wconversion -Wpointer-arith -Wpadded -Wshadow -Wlogical-op -Waggregate-return -Wfloat-equal -Wnull-dereference -Wmaybe-uninitialized -g3 -Wstack-usage=100 -fabi-version=0

Note: The operating frequency used in clock mode 1 (Clock input of 24MHz from EXTAL pin)

Table 2.2 Confirmed operation conditions (2/2)

Item	Contents
Operating mode	Boot mode 4 (Octal-SPI flash boot 1.8V)
Communications settings of the terminal software	• Baud rate: 115200bps • Data length: 8 bits • Parity: None • Stop bits: 1 bit • Flow control: None
Boards used	RZ/A2M CPU board RTK7921053C00000BE (Note) RZ/A2M SUB board RTK79210XXB00000BE
Devices used (functions used on the board)	• OctaFlash allocated to SPI multi-I/O bus space Manufacturer: Macronix, Product No.: MX25UM51245G • RL78/G1C (Convert between USB communication and serial communication to communicate with the host PC.) • LED1

Note: Since RTK7921053C00000BE is not equipped with OctaFlash, this sample code does not run on it as it is. Therefore, the serial flash memory for U2 of RTK7921053C00000BE is replaced with OctaFlash here so that this sample code can run on it.

3. Reference Application Notes

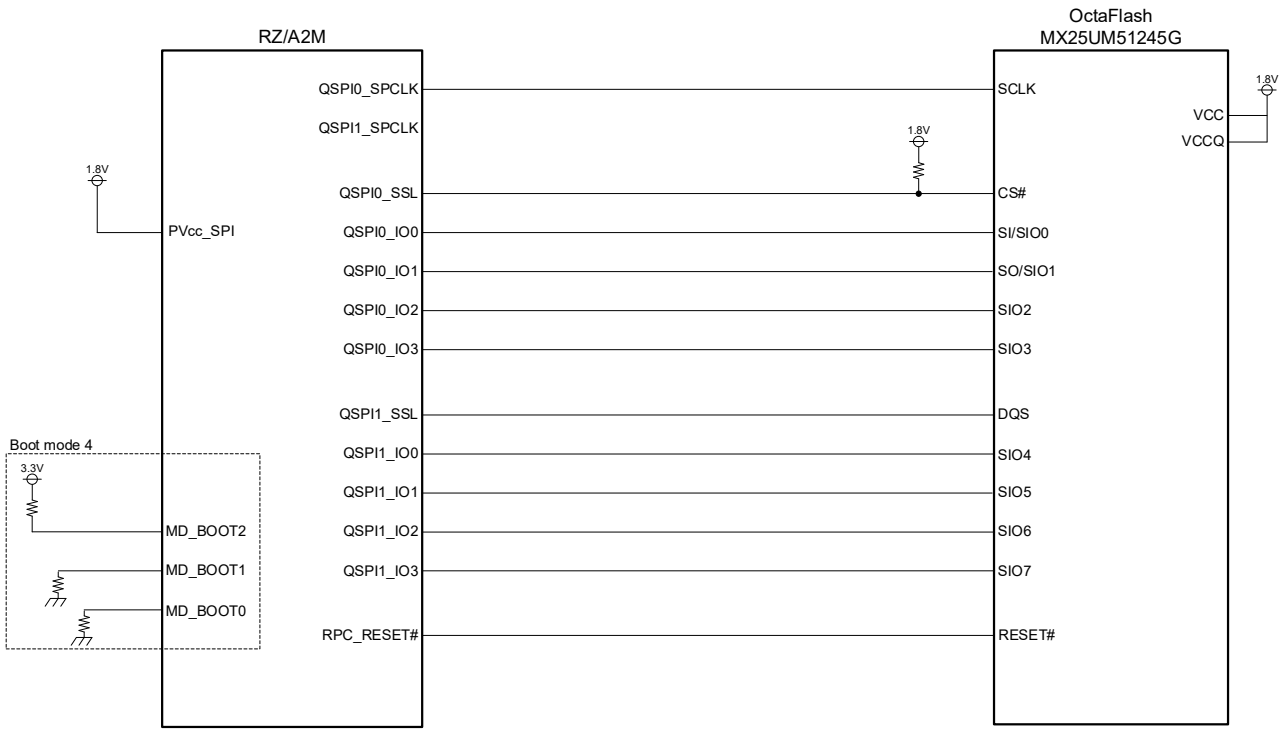
For additional information associated with this document, refer to the following application notes.

- RZ/A2M Group: Example of Initialization (R01AN4321EJ)

4. Hardware

4.1 Hardware Configuration

In the OctaFlash boot example introduced in this application note, processing is performed by the programs stored in the OctaFlash connected to the SPI multi-I/O bus space using boot mode 4. Figure 4.1 shows the Connection example for booting from OctaFlash in boot mode 4.



Notes: 1. # is a symbol that indicates negative logic (or active low).
2. With the boot program stored in the on-chip ROM of the RZ/A2M, which is executed after cancellation of power on reset, QSPI0_SPCLK, QSPI0_SSL, QSPI0_IO0, and QSPI0_IO1 are used for SPI mode boot.

Figure 4.1 Connection example for booting from OctaFlash in boot mode 4

4.2 Pins Used

Table 4.1 lists the Pins used and their functions.

Table 4.1 Pins used and their functions

Pin name	I/O	Function
MD_BOOT2	Input	Select boot mode (set to boot mode 4) MD_BOOT2: "H", MD_BOOT1: "L", MD_BOOT0: "L"
MD_BOOT1	Input	
MD_BOOT0	Input	
QSPI0_SPCLK	Output	OctaFlash clock
QSPI0_SSL	Output	OctaFlash slave select
QSPI0_IO0	I/O	OctaFlash data 0
QSPI0_IO1	I/O	OctaFlash data 1
QSPI0_IO2	I/O	OctaFlash data 2
QSPI0_IO3	I/O	OctaFlash data 3
QSPI1_SSL	Input	OctaFlash data strobe
QSPI1_IO0	I/O	OctaFlash data 4
QSPI1_IO1	I/O	OctaFlash data 5
QSPI1_IO2	I/O	OctaFlash data 6
QSPI1_IO3	I/O	OctaFlash data 7
RPC_RESET#	Output	OctaFlash reset
P6_0	Output	Turns on and off LED
RxD4(P9_1)	Input	Serial receive data signal
TxD4(P9_0)	Output	Serial transmit data signal

Note: # is a symbol that indicates negative logic (or active low).

5. Software

5.1 Operation Overview

This section provides an overview of the sample code operation presented in this application note.

5.1.1 Terms Related to OctaFlash Boot

Table 5.1 lists the Terms related to OctaFlash boot operation described in this application note.

Table 5.1 Terms related to OctaFlash boot operation

Term	Description
Boot startup on-chip ROM program	This program provides settings to directly execute the programs stored in the Octal-SPI flash memory connected to the SPI multi-I/O bus space when started up in boot mode 4 (Octal-SPI flash boot 1.8V). Here, Octal-SPI flash memory is accessed in SPI mode. The RZ/A2M branches to the address of H'2000_0000 which is the start address of the SPI multi-I/O bus space after the boot startup on-chip ROM program has been executed. Note that the boot startup on-chip ROM program makes settings to enable common access to typical Octal-SPI flash memory devices. Since this program is stored in the on-chip ROM of the RZ/A2M, it does not need to be created by the customer.
Loader program	This program is executed after the boot startup on-chip ROM program process has completed. The loader program allows access to the OctaFlash used as the Octal-SPI flash memory in the optimal way. The loader program makes settings to the registers in the SPIBSC and to the registers in the OctaFlash corresponding to the OctaFlash used by the customer, and then branches to the start address of the application program. The loader program should be created by the customer according to the specifications of the OctaFlash to be used while referring to this application note. In the sample code, the initial settings are optimized for use with the Macronix OctaFlash (product No.: MX25UM51245G).
Application program (User program)	This program should be created by customers depending on their system to be used.

5.1.2 Operation Overview of Sample Code Overall

The sample code comprises the loader program executed after boot startup on-chip ROM program process completion and the application program.

1 Loader program (Project name: rza2m_spibsc_octaflash_boot_loader_gcc)
The loader program provides optimal settings to the OctaFlash used (Macronix OctaFlash (product No.: MX25UM51245G)). The loader program is located at the start address (H'2000_0000) of the SPI multi-I/O bus space, which is branched from the boot startup on-chip ROM program. After the loader program runs, it branches to the start address of the application program.
The start address of the application program is specified by the linker_script.ld symbol definition "__application_base_address".

2 Application program (Project name: rza2m_spibsc_octaflash_boot_sample_osless_gcc)
This is an application program to be executed after optimal settings for the OctaFlash are provided in the loader program. Change the location address so the "VECTOR_TABLE" section in the application program is consistent with the address specified by "__application_base_address".
In the sample code, the application program is located at address H'2001_0000.

Figure 5.1 shows the Operation overview of sample code presented in this application note.

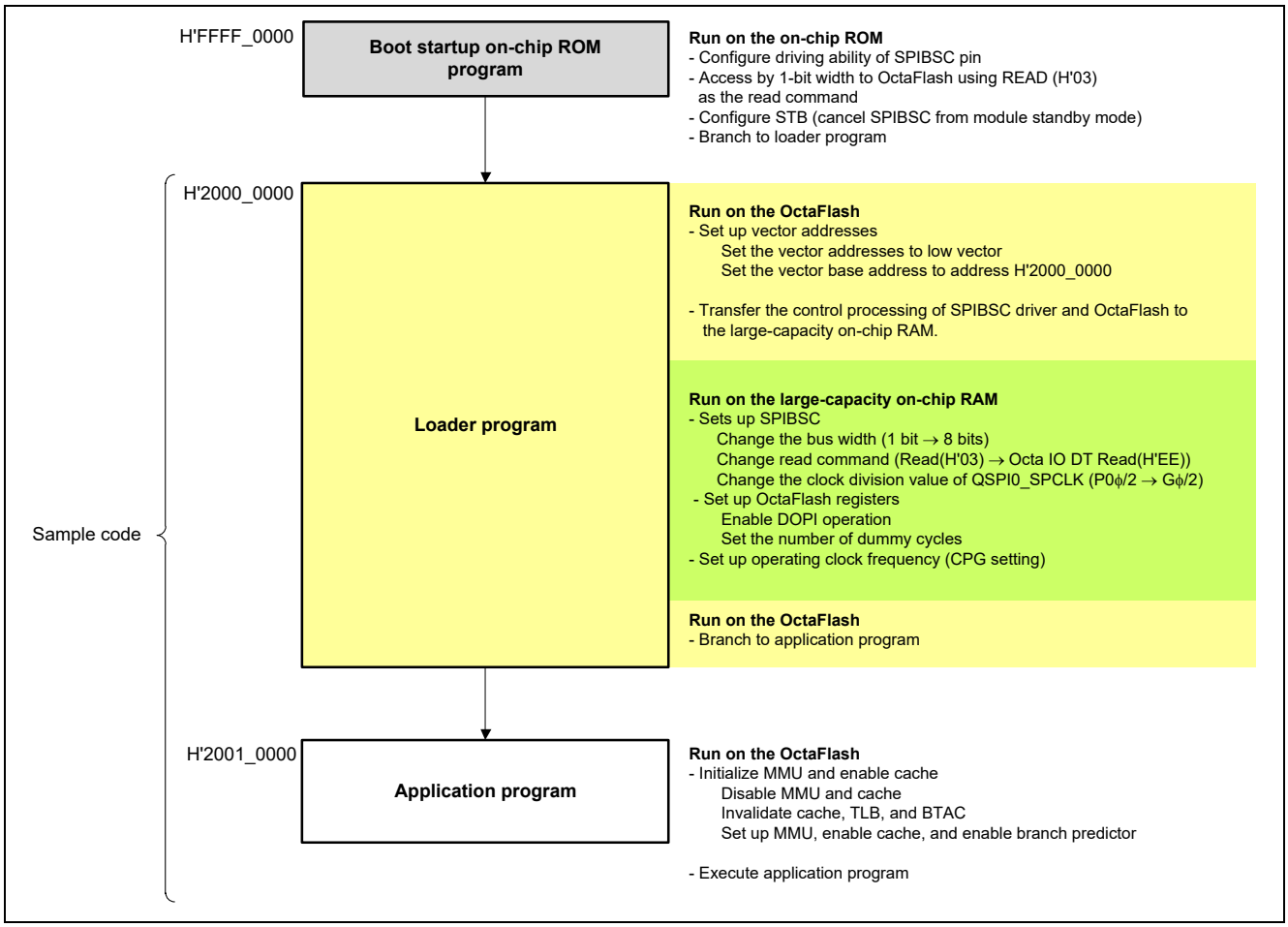


Figure 5.1 Operation overview of sample code

5.1.3 Operation Overview of Loader Program

The loader program is executed after the boot startup on-chip ROM program process has completed. The loader program should be located at the start address (H'2000_0000) of the SPI multi-I/O bus space branched from the boot startup on-chip ROM program.

The boot startup on-chip ROM program makes settings to enable the SPIBSC to operate in external address space read mode. These settings cause the RZ/A2M to convert read operations targeting the SPI multi-I/O bus space to SPI communication so that the direct read operations are enabled to the connected Octal-SPI flash memory. This makes it possible for the RZ/A2M to directly run programs allocated to the SPI multi-I/O bus space. The settings for commands targeting the Octal-SPI flash memory used in SPI communication conversion allow common access to typical Octal-SPI flash memory devices (settings for access in SPI mode), so it is necessary to provide the optimal settings to the Octal-SPI flash memory used by the customer in the loader program.

The loader program uses the OctaFlash as the Octal-SPI flash memory and provides a processing for the optimal access to the OctaFlash. In order to optimally access the OctaFlash, the settings need to be provided in two places: the registers in the SPIBSC module (hereinafter called "SPIBSC settings") and the registers in the OctaFlash (hereinafter called "OctaFlash settings").

In the loader program, the data bus width is set to 8 bits, optimized to the used read command in DOPI mode, and the SPIBSC register is set to optimize the transfer bit rate. Also, a Macronix OctaFlash (product No.: MX25UM51245G) register is set to establish the number of OctaFlash dummy cycles, enable DOPI operations, and change to 4-byte addressing, and optimal settings are established to access MX25UM51245G.

The process that establishes the loader program's SPIBSC settings and OctaFlash settings cannot be set by the program allocated to the SPI multi-I/O bus space, so these should be executed in the area other than the SPI multi-IO bus space. In the sample code, the SPIBSC driver process and OctaFlash control process are transferred to the large-capacity on-chip RAM to be executed.

Refer to Table 5.2 to Table 5.4 for the settings after execution of the boot startup on-chip ROM program and loader program.

Table 5.2 to Table 5.4 list the settings made by the boot startup on-chip ROM program and the loader program.

After the settings listed in Table 5.2 to Table 5.4 are made, the loader program branches to the start address of the application program. In the sample code, the application program is allocated to the area starting at H'2001_0000, which is to be the branch target.

Table 5.2 Settings for the Boot Startup On-Chip ROM Program and Loader Program (1/3)

	Item	After execution of boot startup on-chip ROM program	After execution of loader program
SPIBSC settings	Delay settings		
	Next access delay setting: SSLDR.SPNDL[2:0]	B'000 (1 QSPIn_SPCLK)	B'000 (1 QSPIn_SPCLK)
	QSPIn_SSL negate delay setting: SSLDR.SLNDL[2:0]	B'000 (1 QSPIn_SPCLK)	B'000 (1 QSPIn_SPCLK)
	Clock delay setting: SSLDR.SCKDL[2:0]	B'000 (1.5 QSPIn_SPCLK)	B'000 (1.5 QSPIn_SPCLK)
	Serial clock (QSPI0_SPCLK):	Pϕ / 2=16.5 [MHz] (Note 1)	Gϕ / 2=132 [MHz] (Note 1)
	QSPIn_SSL output idle value fix:	Sets output values in QSPIn_SSL negation period to the last bit value of the previous transfer	Sets the connection of Octal-SPI flash memory
	QSPIn_IO3 setting	CMNCR.MOIIO3[1:0]=B'10	CMNCR.MOIIO3[1:0]=B'01
	QSPIn_IO2 setting	CMNCR.MOIIO2[1:0]=B'10	CMNCR.MOIIO2[1:0]=B'01
	QSPIn_IO1 setting	CMNCR.MOIIO1[1:0]=B'10	CMNCR.MOIIO1[1:0]=B'01
	QSPIn_IO0 setting	CMNCR.MOIIO0[1:0]=B'10	CMNCR.MOIIO0[1:0]=B'01
	Sets the output value of the pin for 1-bit size:	Sets the pin output value for 1-bit size to the last bit value of the previous transfer	Sets the pin output value for 1-bit size to Hi-Z
	QSPIn_IO3 setting	CMNCR.IO3FV[1:0]=B'10	CMNCR.IO3FV[1:0]=B'11
	QSPIn_IO2 setting	CMNCR.IO2FV[1:0]=B'10	CMNCR.IO2FV[1:0]=B'11
	QSPIn_IO0 setting	CMNCR.IO0FV[1:0]=B'10	CMNCR.IO0FV[1:0]=B'11 (Note 2)
	Data bus width: CMNCR.BSZ[1:0]	4 bits B'00	8 bits (Octal-SPI flash memory) B'01
	Read cache: DRCR.RBE	1 (Enabled)	1 (Enabled)
	QSPIn_SSL Negation: DRCR.SSLE	QSPIn_SSL negate every transfer end 0	Address holds assertion of QSPIn_SSL as continuously as possible. If discontinuous from previous transfer address, QSPIn_SSL is negated. 1
	Read data burst length: DRCR.RBURST[4:0]	4 data units (32 bytes) B'00011	4 data units (32 bytes) B'00011
	Data read bit width: DRENR.DRDB[1:0]	1 bit B'00	4 bits (8-bit width) B'10
	Read command: DRCMR.CMD[7:0] DRCMR.OCMD[7:0]	Read H'03 —	Quad I/O DT Read H'EE H'11
	Command enable: DRENR.CDE	Output enabled 1	Output enabled 1
	Command bit width: DRENR.CDB[1:0]	1 bit B'00	4 bits (8-bit width) B'10
	Optional command enable: DRENR.OCDE	Output disabled 0	Output disabled 0
	Optional command bit width: DRENR.OCDB[1:0]	—	4 bits (8-bit width) B'10

Table 5.3 Settings for the boot startup on-chip ROM program and loader program (2/3)

	Item	After execution of boot startup on-chip ROM program	After execution of loader program
SPIBSC settings	Address enable: DRENR.ADE[3:0]	Output address [23:0] B'0111	Octal-SPI flash memory output B'1100
	Address bit size: DRENR.ADB[1:0]	1 bit B'00	4 bits (8-bit width) B'10
	Option data enable: DRENR.OPDE[3:0]	Output disabled B'0000	Output disabled B'0000
	Option data bit size: DRENR.OPDB[1:0]	—	—
	Option data: DROPR.OPD3[7:0] DROPR.OPD2[7:0] DROPR.OPD1[7:0] DROPR.OPD0[7:0]	 — — — —	 — — — —
	Dummy cycle enable: DRENR.DME	Insertion disabled 0	Insertion enabled 1
	Number of dummy cycles: DRDMCR.DMCYC[4:0]	—	14 cycles B'01101
	Extended upper address: DREAR.EAC[2:0] DREAR.EAV[7:0]	External address bits [24:0] enabled Directly accessible 32MB spaces B'000 H'00	External address bits [27:0] enabled Directly accessible 256MB spaces B'011 H'00
	Transfer format: DRDRENR.HYPE[2:0] DRDRENR.ADDRE DRDRENR.OPDRE DRDRENR.DRDRE PHYOFFSET1.DDRTMG[1:0] PHYOFFSET2.OCTTMG[2:0]	Address, option data, and data are transferred in SDR mode, SPI flash mode B'000 0 0 0 B'11 (SDR) B'100 (Serial flash)	Address, option data, and data are transferred in DDR mode, and Octal-SPI flash memory is accessed B'101 1 1 1 B'10 (DDR) B'011 (Octal-SPI flash memory operation)
	Octal-SPI flash memory alternative alignment: PHYCNT.ALT_ALIGN PHYCNT.OCTA[1:0]	Alternative alignment during Octal-SPI flash memory connection is not supported. 0 B'00	Alternative alignment during Octal-SPI flash memory connection is supported. 1 B'01
	Octal-SPI flash memory protocol mode: PHYCNT.OCT	Octal-SPI flash memory protocol mode not used 0	Octal-SPI flash memory protocol mode used 1
	External data strobe: PHYCNT.EXDS	External data strobe signal not used 0	External data strobe signal used 1
	Device selection: PHYCNT.PHYMEM[1:0]	SDR mode serial flash B'00	DDR mode Octal-SPI flash memory B'01
	High-Speed response mode: PHYCNT.HS	High-Speed response mode not used 0	High-Speed response mode not used 0
	Clock timing switching: PHYCNT.CKSEL[1:0]	— B'00	Octal-SPI flash memory connection is set B'11

Table 5.4 Settings for the boot startup on-chip ROM program and loader program (3/3)

	Item	After execution of boot startup on-chip ROM program	After execution of loader program
Pin settings	Pin voltage	Setting in which SPIBSC pin operates at 1.8V	Setting in which SPIBSC pin operates at 1.8V
	PPOC.POCSEL0	1	0
	PPOC.POC0	0	0
	Driving capability		
	PSPIBSC[31:0]	H'0FFF_FFFF (Driving capability of SPIBSC-related pin is 12mA)	H'0FFF_FFFF (Driving capability of SPIBSC-related pin is 12mA)
OctaFlash settings	Configuration Register 2 (Note 3)		
	Address: H'0000_0000	No change	DTR OPI enable DOPI=1, SOPI=0
	Address: H'0000_0300	No change	Number of dummy cycles: 14 DC[2:0] = B'011
Other	Operating clock settings Clock input of 24MHz from EXTAL pin in clock mode 1	Iϕ =132[MHz] Gϕ =264[MHz] Bϕ =132[MHz] P1ϕ =66[MHz] P0ϕ =33[MHz]	Iϕ =528[MHz] Gϕ =264[MHz] Bϕ =132[MHz] P1ϕ =66[MHz] P0ϕ =33[MHz]
	SPIBSC clock selection	Select P0ϕ	Select Gϕ
	SCLKSEL.SPICR[1:0]	B'00	B'11
	CPU exception vector position	High vector (from H'FFFF_0000)	Low vector (from H'0000_0000)
	CP15 vector-based address register (VBAR)	—	H'2000_0000

Notes: 1. The operating clock frequency of QSPI0_SPCLK is set according the combination of Operating clock settings and SPIBSC clock selection.
2. The IO0FV bit in the CMNCR register must be set to B'11 (QSPIn_IO0 pin output value is set to Hi-Z) when data read transfer size is not 1 bit.
3. In boot mode 4 (Octal-SPI flash booting 1.8V) of RZ/A2M, the boot program sets the SPIBSC register to issue a read command (opcode: H'03, address: 24 bits, dummy cycle: none) as the command to the OctaFlash. Therefore, if the OctaFlash cannot receive the above read command by the register value in Octal-SPI flash booting, normal booting may not be possible.
4. Since the CAL bit in PHYCNT need not be set if OctaFlash is accessed in the external address space read mode, it is not listed in the above table. If OctaFlash is accessed in manual mode, the CAL bit must always be set to 1 each time before sending a command to OctaFlash.

5.1.4 Application Program

(1) Operation of the application program

After a reset is cancelled, the boot startup on-chip ROM program and loader program are executed in that order. Then the execution transfers to the application program that is allocated to address H'2001_0000.

In the startup process, the settings for the stack pointer, MMU, and FPU are executed. The section initialization is performed, and it branches to the resetprg function.

In the resetprg function, after RTC and USB unused channel initialization processing is executed, L1 cache and L2 cache are enabled and INTC initialization is performed. The large-capacity on-chip RAM address is set in VBAR to enable high-speed interrupt processing, IRQ interrupt and FIQ interrupt are enabled, and the main function is called.

In the main function, CPG, OSTM channel 0, SCIFA channel 4, and GPIO initial setting processing is performed. As a result of this initialization processing, the main function outputs the character strings (startup message) to the terminal on the host PC connected with the serial interface and sets the OSTM channel 0 timer to interval timer mode to activate the timer. It generates the OSTM channel 0 interrupt with a cycle of 500ms and repeats turning on/off the LED on the CPU board every 500ms using such interrupt.

For details on the initialization executed by the application program, refer to the application note "RZ/A2M Group Example of Initialization".

(2) Notes to be observed when creating an application program

The application program should be allocated to the address branched from the loader program. Note that the application program should be allocated to the different sector in the OctaFlash from the one in the loader program.

The sector size of the Macronix OctaFlash (MX25UM51245G) is 4KB. In the sample code, the application program is allocated to the address of H'2001_0000 (Sector no. 16).

Figure 5.2 shows the Sample code program allocation.

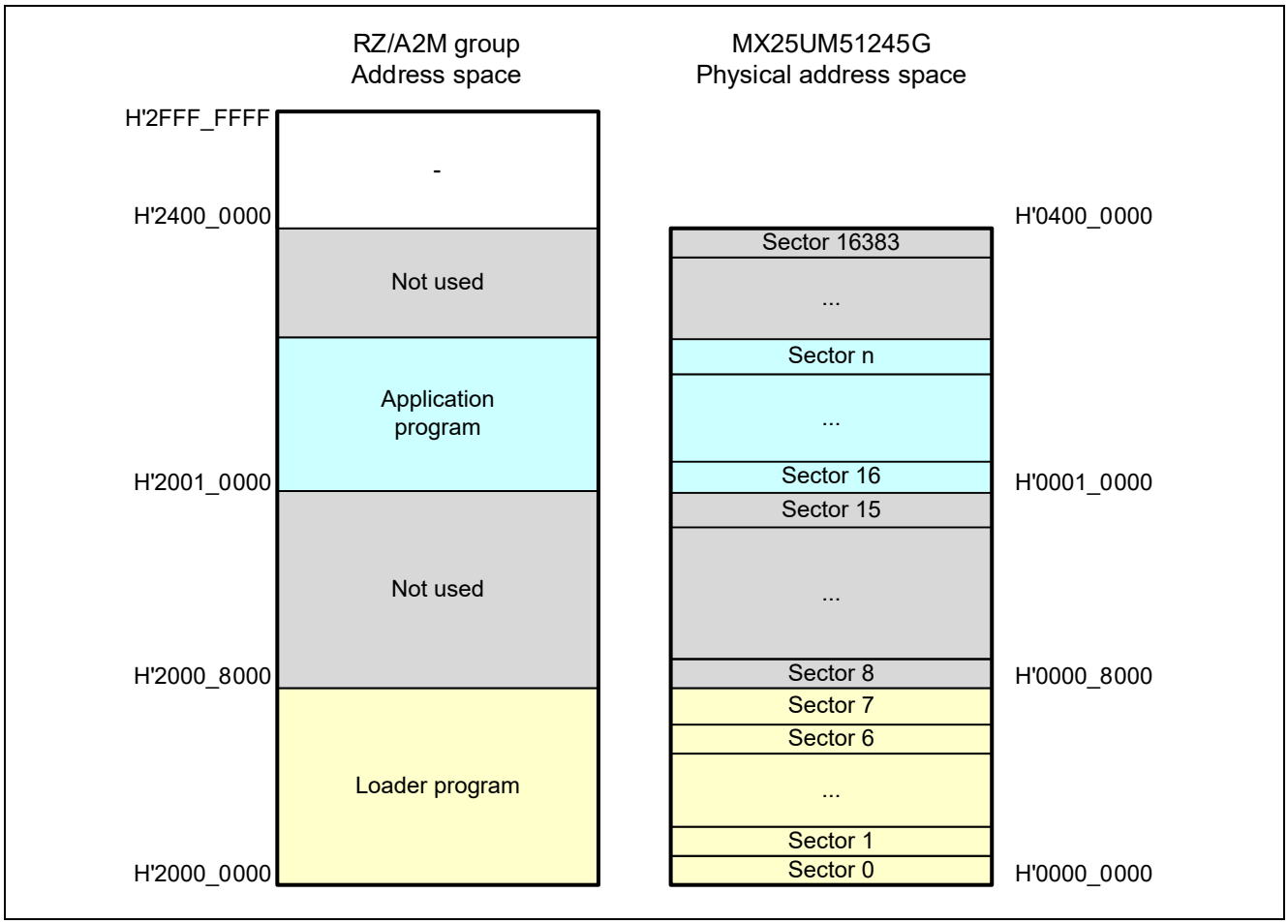


Figure 5.2 Sample code program allocation

The start address of the application program can be changed by making the following changes:

- Project for the loader program
  The branch to the starting address of the application program is executed by the loader program (reset_handler.asm). Specify the destination of branch with the linker script symbol definition "__application_base_address" in linker_script.ld.
- Project for the application program
  Change the allocation address so that the VECTOR_TABLE section of the application program matches the address that is specified in "__application_base_address".

5.2 Peripheral Functions and Memory Allocation in Sample Code

5.2.1 Setting for Peripheral Functions

Table 5.5 lists the Setting for Peripheral Functions during execution of the sample code.

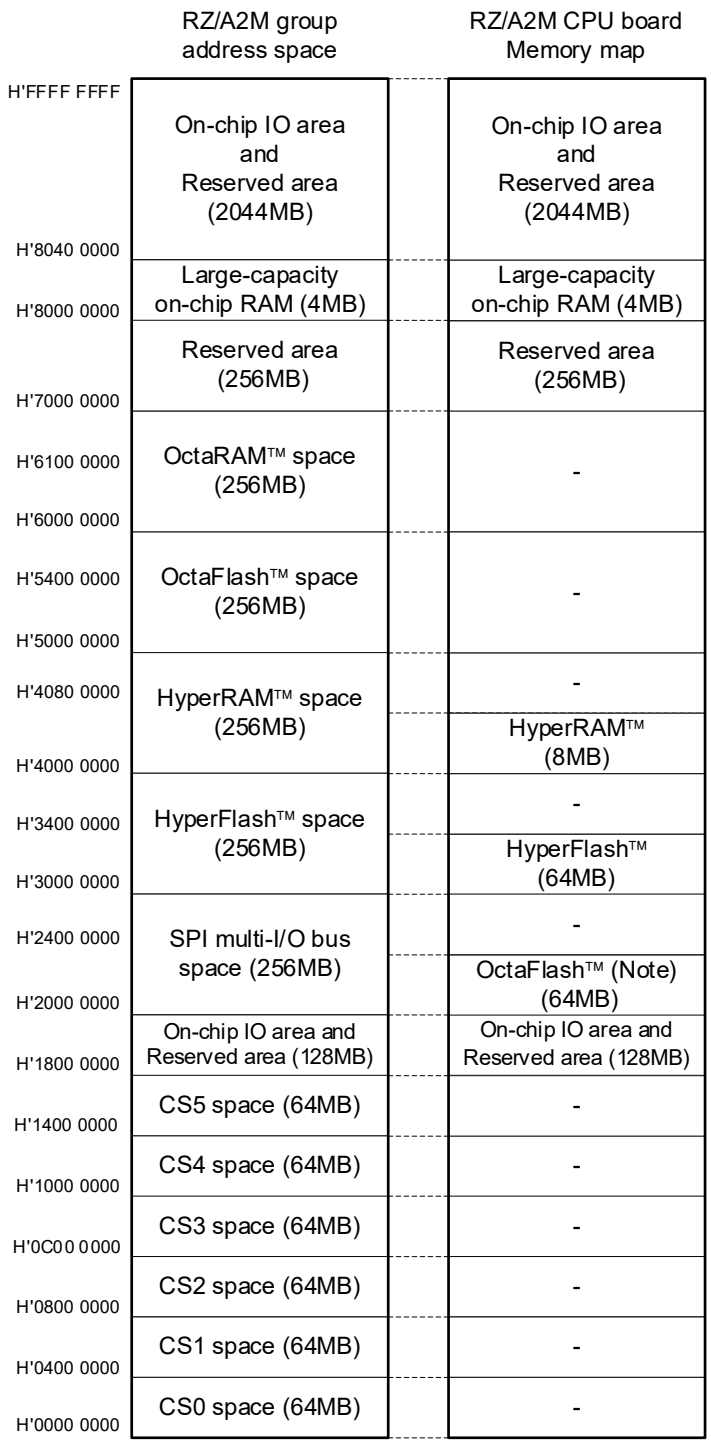
Table 5.5 Setting for Peripheral Functions

Module	Settings
CPG	CPU clock: Set to 1/2 the PLL circuit frequency Internal bus clock: Set to 1/8 the PLL circuit frequency Peripheral clock 1 (P1ϕ): Set to 1/16 the PLL circuit frequency If the input clock is 24MHz in clock mode 1 (divider 1: ×1/2, PLL circuit: ×88), set to the following frequencies • CPU clock (Iϕ): 528MHz • Image processing clock (Gϕ): 264MHz • Internal bus clock (Bϕ): 132MHz • Peripheral clock 1 (P1ϕ): 66MHz • Peripheral clock 0 (P0ϕ): 33MHz • QSPI0_SPCLK: 132MHz (when Gϕ is selected) • CKIO clock: 132MHz (when Bϕ is selected)
SPIBSC	When set to the external address space read mode, it generates the signals which enable the CPU to read directly from the OctaFlash connected to the SPI multi-I/O bus space.
STB	Write permission to on-chip data retention RAM and provision of clock to peripheral functions Clock is supplied to OSTM0, OSTM2, SCIFA4, and SPIBSC with STBCR3, STBCR4, and STBCR8.
GPIO	PORT6 and PORT9 shared pin functions are set. • P6_0: Turns on and off LED • P9_1: RxD4, P9_0: TxD4
OSTM	Sets the channel 0 and the channel 2 in interval timer mode. • Channel 0 Sets the timer counter to have interrupt request generated every 500ms when P1ϕ=66MHz. Generate the intervals at which the LEDs are turned on and off. • Channel 2 Sets the timer counter to have interrupt request generated every 1ms when P1ϕ=66MHz. Used for time management via OS Abstraction Layer.
INTC	Initializes INTC, and registers and executes OSTM channel 0 interrupt (interrupt ID is 88) handler, OSTM channel 2 interrupt (interrupt ID is 90) handler and SCIFA channel 4 interrupt (interrupt ID is 322, 323) handler
SCIFA	Sets the channel 4 in asynchronous communication mode • Data length: 8 bits • Stop bits: 1 bit • Parity: None • Data transfer direction: LSB first transfer Sets the clock source without frequency dividing, the baud rate generator to double speed mode, and the basic clock at 8 times the bit rate when P1ϕ is 66MHz. Sets the bit rate to 71 so that the bit rate is 115200bps. (The bit rate error is -0.53%)

5.2.2 Memory Mapping

Figure 5.3 shows the RZ/A2M Group Address Space and RZ/A2M CPU board memory map.

In the sample code, the code and data that use the ROM area are assigned to the OctaFlash connected to the SPI multi-I/O bus, and the code and data that use the RAM area are assigned to the large-capacity on-chip RAM.



Note: Since the RZ/A2M CPU board is not equipped with OctaFlash, the serial flash memory for U2 of the RZ/A2M CPU board is replaced with OctaFlash so that this sample code can run on it.

Figure 5.3 Memory mapping

5.2.3 Section Assignment in Sample Code

Table 5.6 shows the Sections and Objects to Be Used in the Loader Program.

For section assignments used in the application program, refer to the application note "RZ/A2M Group Example of Initialization".

Table 5.6 Sections and Objects to Be Used in the Loader Program

Output section name	Input section name Input object name	Description	Loading area	Execution area
LOAD_MODULE1	VECTOR_TABLE	Exception processing vector table	FLASH	FLASH
LOAD_MODULE2	*/r_cpg/*.o (.text .rodata)	CPG settings processing	FLASH	LRAM
	*/rza_io_regrw.o (.text .rodata)	I/O register access processing		
	/r_spibsc/.o (.text .rodata)	SPIBSC settings processing		
	*/hwsetup.o (.text .rodata)	Hardware Setup settings processing		
	* (.data .data.*)	Data area with default initial values		
LOAD_MODULE3	RESET_HANDLER	Reset processing	FLASH	FLASH
	INIT_SECTION */sections.o	Section initialization processing		
	* (.text .text.*)	Code area for defaults		
	* (.rodata .rodata.*)	Constant data area for defaults		
.data.memclk_setup	*/r_memclk_setup.o (.text .rodata .data)	Memory clock setting processing	FLASH	LRAM
	*/r_spibsc_setup.o (.text .rodata .data)	Memory clock setting processing for SPIBSC		
	*/r_*_memclk_setup.o (.text .rodata .data)	Memory clock setting processing for each driver		
.bss.memclk_setup	*/r_memclk_setup.o (.bss COMMON)	Data area without default initial values for memory clock settings processing	—	LRAM
	*/r_spibsc_setup.o (.bss COMMON)	Data area without default initial values for memory clock settings processing for SPIBSC		
	*/r_*_memclk_setup.o (.bss COMMON)	Data area without default initial values for memory clock settings processing for each driver		
.stack	None	Stack area for SVC mode	—	LRAM
.bss	* (.bss .bss.*) * (COMMON)	Data area without default initial values	—	LRAM
.heap	None	Heap area	—	LRAM

Note: "FLASH" and "LRAM" shown in Loading Area and Execution Area indicate the OctaFlash area and the large-capacity on-chip RAM area respectively.

5.3 Interrupt Used

Interrupt is not used in the loader program.

For interrupt used in the application program, refer to the application note "RZ/A2M Group Example of Initialization".

5.4 Data Types

Table 5.7 shows the Data Types Used in the Sample Code.

Table 5.7 Data Types Used in the Sample Code

Symbol	Description
char_t	8-bit character
bool_t	Boolean type. Value is true (1) or false (0).
int_t	Fast integer, signed, 32-bit integer in this sample code
int8_t	8-bit integer, signed (defined in standard library stdint.h)
int16_t	16-bit integer, signed (defined in standard library stdint.h)
int32_t	32-bit integer, signed (defined in standard library stdint.h)
int64_t	64-bit integer, signed (defined in standard library stdint.h)
uint8_t	8-bit integer, unsigned (defined in standard library stdint.h)
uint16_t	16-bit integer, unsigned (defined in standard library stdint.h)
uint32_t	32-bit integer, unsigned (defined in standard library stdint.h)
uint64_t	64-bit integer, unsigned (defined in standard library stdint.h)
float32_t	32-bit float
float64_t	64-bit float
float128_t	128-bit float

5.5 Constants Used by the Loader Program

Table 5.8 and Table 5.9 list the constants used by the loader program.

For the constants used in the application program, refer to the application note "RZ/A2M Group Example of Initialization".

Table 5.8 Constants Used in the Loader Program (1/2)

Constant	Setting value	Description
STARTUP_CFG_BOOT_MODE	(4)	Sets Octal-SPI flash boot for operation
STARTUP_CFG_SPIBSC_CONNECT_DEVICE_TYPE	(2)	Sets the Octal-SPI flash memory as flash memory to be connected to SPIBSC
STARTUP_CFG_PROJECT_TYPE	(0)	Information indicating that it is a loader program
SPIBSC_SUCCESS	(0)	Normal end
SPIBSC_ERR_INVALID	(-1)	Error end
SPIBSC_PORT_VOLTAGE_3_3V	(0)	Sets the operating voltage of the dedicated pin used by the SPIBSC to 3.3V
SPIBSC_PORT_VOLTAGE_1_8V	(1)	Sets the operating voltage of the dedicated pin used by the SPIBSC to 1.8V
SPIBSC_FLASH_OCTA	(1)	Sets the flash memory type to OctaFlash
SPIBSC_MODE_MANUAL	(0)	Sets the SPIBSC operating mode to manual mode
SPIBSC_MODE_XIP	(1)	Sets the SPIBSC operating mode to external address space read mode
SPIBSC_CMNCR_BSZ_SINGLE	(0)	Sets the data bus width of the flash memory to be connected to SPIBSC to 4 bits
SPIBSC_CMNCR_BSZ_DUAL	(1)	Sets the data bus width of the flash memory to be connected to SPIBSC to 8 bits
SPIBSC_OCTA_OPI_DISABLE	(0)	Used as information to disable DOPI mode by Configuration Register 2 of the OctaFlash (MX25UM51245G)
SPIBSC_OCTA_OPI_ENABLE	(1)	Used as information to enable DOPI mode by Configuration Register 2 of the OctaFlash (MX25UM51245G)
SPIBSC_RDSR_WEL	(0x02)	Used as information to refer to the Status Register's WEL bit of the OctaFlash (MX25UM51245G)
SPIBSC_RDSR_WIP	(0x01)	Used as information to refer to the Status Register's WIP bit of the OctaFlash (MX25UM51245G)
SPIBSC_1BIT_WIDTH	(0)	Sets the command, optional command, address, option data, and transfer data bit width to 1 bit
SPIBSC_8BIT_WIDTH	(2)	Sets the command, optional command, address, option data, and transfer data bit width to 8 bits
SPIBSC_OUTPUT_DISABLE	(0)	Disables the output of command, optional command, address, option data, and dummy cycle
SPIBSC_OUTPUT_ENABLE	(1)	Enables the output of command, optional command, and dummy cycle
SPIBSC_OUTPUT_ADDR_24	(0x07)	Outputs a 24-bit address
SPIBSC_OUTPUT_ADDR_32	(0x0f)	Outputs a 32-bit address
SPIBSC_OUTPUT_ADDR_OCTA	(0x0c)	Outputs an address for Octal-SPI flash memory
SPIBSC_OUTPUT_OPD_3	(0x08)	Outputs option data OPD3
SPIBSC_OUTPUT_OPD_32	(0x0c)	Outputs option data OPD3 and OPD2
SPIBSC_OUTPUT_OPD_321	(0x0e)	Outputs option data OPD3, OPD2, and OPD1
SPIBSC_OUTPUT_OPD_3210	(0x0f)	Outputs option data OPD3, OPD2, OPD1, and OPD0

Table 5.9 Constants Used in the Loader Program (2/2)

Constant	Setting value	Description
SPIBSC_DUMMY_02CYC	(1)	Sets the number of dummy cycles to 2
SPIBSC_DUMMY_03CYC	(2)	Sets the number of dummy cycles to 3
SPIBSC_DUMMY_04CYC	(3)	Sets the number of dummy cycles to 4
SPIBSC_DUMMY_05CYC	(4)	Sets the number of dummy cycles to 5
SPIBSC_DUMMY_06CYC	(5)	Sets the number of dummy cycles to 6
SPIBSC_DUMMY_07CYC	(6)	Sets the number of dummy cycles to 7
SPIBSC_DUMMY_08CYC	(7)	Sets the number of dummy cycles to 8
SPIBSC_DUMMY_09CYC	(8)	Sets the number of dummy cycles to 9
SPIBSC_DUMMY_10CYC	(9)	Sets the number of dummy cycles to 10
SPIBSC_DUMMY_11CYC	(10)	Sets the number of dummy cycles to 11
SPIBSC_DUMMY_12CYC	(11)	Sets the number of dummy cycles to 12
SPIBSC_DUMMY_13CYC	(12)	Sets the number of dummy cycles to 13
SPIBSC_DUMMY_14CYC	(13)	Sets the number of dummy cycles to 14
SPIBSC_DUMMY_15CYC	(14)	Sets the number of dummy cycles to 15
SPIBSC_DUMMY_16CYC	(15)	Sets the number of dummy cycles to 16
SPIBSC_DUMMY_17CYC	(16)	Sets the number of dummy cycles to 17
SPIBSC_DUMMY_18CYC	(17)	Sets the number of dummy cycles to 18
SPIBSC_DUMMY_19CYC	(18)	Sets the number of dummy cycles to 19
SPIBSC_DUMMY_20CYC	(19)	Sets the number of dummy cycles to 20
SPIBSC_DDR_TRANSFER	(1)	Sets the address, option data, and data transfer to DDR transfer
SIPBSC_SDR_TRANSFER	(0)	Sets the address, option data, and data transfer to SDR transfer
SPIBSC_QSPI_IO_OUTPUT_0	(0x00)	Sets the QSPIn_IO output value to 0
SPIBSC_QSPI_IO_OUTPUT_1	(0x01)	Sets the QSPIn_IO output value to 1
SPIBSC_QSPI_IO_OUTPUT_PREVIOUS	(0x02)	Sets the QSPIn_IO output value to previous state
SPIBSC_QSPI_IO_OUTPUT_HI_Z	(0x03)	Sets the QSPIn_IO output value to HI-Z
SPIBSC_MANUAL_8BIT_TRANSFERRED	(0x8)	Sets the transfer bit during data transfer in manual mode to 8 bits
SPIBSC_MANUAL_16BIT_TRANSFERRED	(0x8)	Sets the transfer bit during data transfer in manual mode to 16 bits
SPIBSC_MANUAL_32BIT_TRANSFERRED	(0xf)	Sets the transfer bit during data transfer in manual mode to 32 bits
SPIBSC_MANUAL_64BIT_TRANSFERRED	(0xf)	Sets the transfer bit during data transfer in manual mode to 64 bits

5.6 List of Structures/Unions Used by the Loader Program

Table 5.10 to Table 5.22 list the structures used by the loader program.

Table 5.10 Structure for Configuring the SPIBSC Register (st_spibsc_config_t)

Member	Description
uint8_t flash_type	Specifies the type of connected flash memory. SPIBSC_FLASH_OCTA: OctaFlash
uint8_t flash_num	Specifies the data bus width of flash memory. SPIBSC_CMNCR_BSZ_SINGLE: 4-bit width (unsupported) SPIBSC_CMNCR_BSZ_DUAL: 8-bit width
uint8_t flash_port_voltage	Specifies the voltage setting of the SPIBSC's dedicated pin. SPIBSC_PORT_VOLTAGE_3_3V: 3.3V SPIBSC_PORT_VOLTAGE_1_8V: 1.8V

Table 5.11 Structure for Configuring the SPIBSC External Address Space Read Mode (st_spibsc_xip_config_t) (1/6)

Member	Description
uint8_t command_name[20]	Character string that identifies the read command • This member does not affect the register settings.
uint8_t cmd	Read command • Specifies the read command output to the OctaFlash when converting read operations targeting the SPI multi-I/O bus space to SPI communication. • The setting value of this member is set in the CMD[7:0] bit field in the data read command setting register (DRCMR).
uint8_t cmd_width	Read command bit width • Specifies the bit width used when issuing read commands. • Settable values: SPIBSC_1BIT_WIDTH: 1-bit width SPIBSC_8BIT_WIDTH: 8-bit width • The setting value of this member is set in the CDB[1:0] bit field in the data read enable setting register (DRENR).
uint8_t cmd_output_enable	Read command enable • Selects whether or not a read command is issued. • Settable values: SPIBSC_OUTPUT_DISABLE: Not issued SPIBSC_OUTPUT_ENABLE: Issued • The setting value of this member is set in the CDE bit field in the data read enable setting register (DRENR).
uint8_t ocmd	Optional command • Specifies the optional command output to the OctaFlash when converting read operations targeting the SPI multi-I/O bus space to SPI communication. • The setting value of this member is set in the OCMD[7:0] bit field in the data read command setting register (DRCMR).
uint8_t ocmd_width	Optional command bit width • Specifies the bit width used when issuing optional commands. • Settable values: SPIBSC_1BIT_WIDTH: 1-bit width SPIBSC_8BIT_WIDTH: 8-bit width • The setting value of this member is set in the OCDB[1:0] bit field in the data read enable setting register (DRENR).
uint8_t ocmd_output_enable	Optional command enable • Selects whether or not an optional command is issued. • Settable values: SPIBSC_OUTPUT_DISABLE: Not issued SPIBSC_OUTPUT_ENABLE: Issued • The setting value of this member is set in the OCDE bit field in the data read enable setting register (DRENR).

Table 5.12 Structure for Configuring the SPIBSC External Address Space Read Mode (st_spibsc_xip_config_t) (2/6)

Member	Description
uint8_t addr_width	Address bit width • Specifies the address bit width output to the OctaFlash when converting read operations targeting the SPI multi-I/O bus space to SPI communication. • Settable values: SPIBSC_1BIT_WIDTH: 1-bit width SPIBSC_8BIT_WIDTH: 8-bit width • The setting value of this member is set in the ADB[1:0] bit field in the data read enable setting register (DRENR).
uint8_t addr_output_enable	Address enable • Specifies the address output to the OctaFlash when converting read operations targeting the SPI multi-I/O bus space to SPI communication. • Settable values: SPIBSC_OUTPUT_DISABLE: Not output SPIBSC_OUTPUT_ADDR_24: 24-bit address output SPIBSC_OUTPUT_ADDR_32: 32-bit address output SPIBSC_OUTPUT_ADDR_OCTA: Octal-SPI flash memory address output • The setting value of this member is set in the ADE[3:0] bit field in the data read enable setting register (DRENR).
uint8_t addr_ddr_enable	Address DDR enable • Selects SDR/DDR transfer for the address output in external address space read mode. • Settable values: SPIBSC_SDR_TRANSFER: SDR transfer SPIBSC_DDR_TRANSFER: DDR transfer • The setting value of this member is set in the ADDRE bit field in the data read DDR enable register (DRDRENR).
uint8_t reserve1	Reserve data • This member is not referenced in the sample code.
uint8_t reserve2	Reserve data • This member is not referenced in the sample code.

Table 5.13 Structure for Configuring the SPIBSC External Address Space Read Mode (st_spibsc_xip_config_t) (3/6)

Member	Description
uint8_t opdata_width	Option data bit width • Specifies the bit width used when issuing option data. • Settable values: SPIBSC_1BIT_WIDTH: 1-bit width SPIBSC_8BIT_WIDTH: 8-bit width • The setting value of this member is set in the OPDB[1:0] bit field in the data read enable setting register (DRENR).
uint8_t opdata_output_enable	Option data enable • Selects whether or not the option data is issued. • Settable values: SPIBSC_OUTPUT_DISABLE: Not output SPIBSC_OUTPUT_OPD_3: OPD3 output SPIBSC_OUTPUT_OPD_32: OPD3, OPD2 output SPIBSC_OUTPUT_OPD_321: OPD3, OPD2, OPD1 output SPIBSC_OUTPUT_OPD_3210: OPD3, OPD2, OPD1, OPD0 output • The setting value of this member is set in the OPDE[3:0] bit field in the data read enable setting register (DRENR).
uint8_t opdata_ddr_enable	Option data DDR enable • Selects SDR/DDR transfer for the option data output in external address space read mode. • Settable values: SPIBSC_SDR_TRANSFER: SDR transfer SPIBSC_DDR_TRANSFER: DDR transfer • The setting value of this member is set in the OPDRE bit field in the data read DDR enable register (DRDRENR).
uint8_t opd3 uint8_t opd2 uint8_t opd1 uint8_t opd0	Option data • Specifies the option data output to the OctaFlash when converting read operations targeting the SPI multi-I/O bus space to SPI communication. • The setting value of this member is set in the OPD3[7:0], OPD2[7:0], OPD1[7:0], and OPD0[7:0] bit fields in the data read option setting register (DROPR).

Table 5.14 Structure for Configuring the SPIBSC External Address Space Read Mode (st_spibsc_xip_config_t) (4/6)

Member	Description
uint8_t reserve3	Reserve data This member is not referenced in the sample code.
uint8_t dummy_cycle_enable	Dummy cycle enable • Selects whether or not dummy cycles are inserted. • Settable values: SPIBSC_OUTPUT_DISABLE: Not inserted SPIBSC_OUTPUT_ENABLE: Inserted • The setting value of this member is set in the DME bit field in the data read enable setting register (DRENR).
uint8_t dummy_cycle_count	Number of dummy cycles • Sets the number of inserted dummy cycles. • Settable values: SPIBSC_DUMMY_02CYC to SPIBSC_DUMMY_20CYC • The setting value of this member is set in the DMCYC[4:0] bit field in the data read dummy cycle setting register (DRDMCR).
uint8_t data_width	Data read bit width • Specifies the data read bit width of the OctaFlash when converting read operations targeting the SPI multi-I/O bus space to SPI communication. • Settable values: SPIBSC_1BIT_WIDTH: 1-bit width SPIBSC_8BIT_WIDTH: 8-bit width • The setting value of this member is set in the DRDB[1:0] bit field in the data read enable setting register (DRENR).
uint8_t data_ddr_enable	Transfer data DDR enable • Selects SDR/DDR transfer for the data transferred in external address space read mode. • Settable values: SPIBSC_SDR_TRANSFER: SDR transfer SPIBSC_DDR_TRANSFER: DDR transfer • The setting value of this member is set in the DRDRE bit field in the data read DDR enable register (DRDRENR).

Table 5.15 Structure for Configuring the SPIBSC External Address Space Read Mode (st_spibsc_xip_config_t) (5/6)

Member	Description
uint8_t cmncr_moiio3	Level for QSPIn_IO3 while SSL negated. • Specify the level after finished the data transfer. • Settable values: SPIBSC_QSPI_IO_OUTPUT_0: The output value is 0. SPIBSC_QSPI_IO_OUTPUT_1: The output value is 1. SPIBSC_QSPI_IO_OUTPUT_PREVIOUS: The output value is that of the last bit in the previous transfer (the pin is placed in the Hi-Z state if that was the case in the previous transfer). SPIBSC_QSPI_IO_OUTPUT_HI_Z: The pin is placed in the Hi-Z state. • The setting value of this member is set in the MOIIO3[1:0] bit field in the Common Control Register (CMNCR).
uint8_t cmncr_moiio2	Level for QSPIn_IO2 while SSL negated. • Specify the level after finished the data transfer. • Settable values: SPIBSC_QSPI_IO_OUTPUT_0: The output value is 0. SPIBSC_QSPI_IO_OUTPUT_1: The output value is 1. SPIBSC_QSPI_IO_OUTPUT_PREVIOUS: The output value is that of the last bit in the previous transfer (the pin is placed in the Hi-Z state if that was the case in the previous transfer). SPIBSC_QSPI_IO_OUTPUT_HI_Z: The pin is placed in the Hi-Z state. • The setting value of this member is set in the MOIIO2[1:0] bit field in the Common Control Register (CMNCR).
uint8_t cmncr_moiio1	Level for QSPIn_IO1 while SSL negated. • Specify the level after finished the data transfer. • Settable values: SPIBSC_QSPI_IO_OUTPUT_0: The output value is 0. SPIBSC_QSPI_IO_OUTPUT_1: The output value is 1. SPIBSC_QSPI_IO_OUTPUT_PREVIOUS: The output value is that of the last bit in the previous transfer (the pin is placed in the Hi-Z state if that was the case in the previous transfer). SPIBSC_QSPI_IO_OUTPUT_HI_Z: The pin is placed in the Hi-Z state. • The setting value of this member is set in the MOIIO1[1:0] bit field in the Common Control Register (CMNCR).
uint8_t cmncr_moiio0	Level for QSPIn_IO0 while SSL negated. • Specify the level after finished the data transfer. • Settable values: SPIBSC_QSPI_IO_OUTPUT_0: The output value is 0. SPIBSC_QSPI_IO_OUTPUT_1: The output value is 1. SPIBSC_QSPI_IO_OUTPUT_PREVIOUS: The output value is that of the last bit in the previous transfer (the pin is placed in the Hi-Z state if that was the case in the previous transfer). SPIBSC_QSPI_IO_OUTPUT_HI_Z: The pin is placed in the Hi-Z state. • The setting value of this member is set in the MOIIO0[1:0] bit field in the Common Control Register (CMNCR).

Table 5.16 Structure for Configuring the SPIBSC External Address Space Read Mode (st_spibsc_xip_config_t) (6/6)

Member	Description
uint8_t cmncr_io3fv	Level for QSPIn_IO3 while 1-bit width transfer. • Specify the level while the data transfer is done by 1-bit width. • Settable values: SPIBSC_QSPI_IO_OUTPUT_0: The output value is 0. SPIBSC_QSPI_IO_OUTPUT_1: The output value is 1. SPIBSC_QSPI_IO_OUTPUT_PREVIOUS: The output value is that of the last bit in the previous transfer (the pin is placed in the Hi-Z state if that was the case in the previous transfer). SPIBSC_QSPI_IO_OUTPUT_HI_Z: The pin is placed in the Hi-Z state. • The setting value of this member is set in the IO3FV[1:0] bit field in the Common Control Register (CMNCR).
uint8_t cmncr_io2fv	Level for QSPIn_IO2 while 1-bit width transfer. • Specify the level while the data transfer is done by 1-bit width. • Settable values: SPIBSC_QSPI_IO_OUTPUT_0: The output value is 0. SPIBSC_QSPI_IO_OUTPUT_1: The output value is 1. SPIBSC_QSPI_IO_OUTPUT_PREVIOUS: The output value is that of the last bit in the previous transfer (the pin is placed in the Hi-Z state if that was the case in the previous transfer). SPIBSC_QSPI_IO_OUTPUT_HI_Z: The pin is placed in the Hi-Z state. • The setting value of this member is set in the IO2FV[1:0] bit field in the Common Control Register (CMNCR).
uint8_t cmncr_io0fv	Level for QSPIn_IO0 while 1-bit width read transfer. • Specify the level while the data read transfer is done by 1-bit width. • Settable values (Note): SPIBSC_QSPI_IO_OUTPUT_0: The output value is 0. SPIBSC_QSPI_IO_OUTPUT_1: The output value is 1. SPIBSC_QSPI_IO_OUTPUT_PREVIOUS: The output value is that of the last bit in the previous transfer (the pin is placed in the Hi-Z state if that was the case in the previous transfer). SPIBSC_QSPI_IO_OUTPUT_HI_Z: The pin is placed in the Hi-Z state. • The setting value of this member is set in the IO0FV[1:0] bit field in the Common Control Register (CMNCR).

Note: cmncr_io0fv must be set to "SPIBSC_QSPI_IO_OUTPUT_HI_Z" when data read transfer size is not 1 bit (data_width is not set to "SPIBSC_1BIT_WIDTH").

Table 5.17 SPIBSC Manual Mode Settings Structure (st_spibsc_manual_mode_command_config_t) (1/6)

Member	Description
uint8_t command_name[20]	Character string that identifies the SPI command • This member does not affect the register settings.
uint8_t cmd	Command • Specifies the command output in manual mode. • The setting value of this member is set in the CMD[7:0] bit field in the manual mode command setting register (SMCMR).
uint8_t cmd_width	Command bit width • Specifies the bit width used when issuing commands. • Settable values: SPIBSC_1BIT_WIDTH: 1-bit width SPIBSC_8BIT_WIDTH: 8-bit width • The setting value of this member is set in the CDB[1:0] bit field in the manual mode enable setting register (SMENR).
uint8_t cmd_output_enable	Command enable • Selects whether or not a command is issued. • Settable values: SPIBSC_OUTPUT_DISABLE: Not issued SPIBSC_OUTPUT_ENABLE: Issued • The setting value of this member is set in the CDE bit field in the manual mode enable setting register (SMENR).
uint8_t ocmd	Optional command • Specifies the optional command output in manual mode. • The setting value of this member is set in the OCMD[7:0] bit field in the manual mode command setting register (SMCMR).
uint8_t ocmd_width	Optional command bit width • Specifies the optional command bit width in manual mode. • Settable values: SPIBSC_1BIT_WIDTH: 1-bit width SPIBSC_8BIT_WIDTH: 8-bit width • The setting value of this member is set in the OCDB[1:0] bit field in the manual mode enable setting register (SMENR).
uint8_t ocmd_enable	Optional command enable • Specifies whether or not the optional command is output in manual mode. • Settable values: SPIBSC_OUTPUT_DISABLE: Not output SPIBSC_OUTPUT_ENABLE: Output • The setting value of this member is set in the OCDE bit field in the manual mode enable setting register (SMENR).

Table 5.18 SPIBSC Manual Mode Settings Structure (st_spibsc_manual_mode_command_config_t) (2/6)

Member	Description
uint8_t addr_width	Address bit width • Specifies the address bit width in manual mode. • Settable values: SPIBSC_1BIT_WIDTH: 1-bit width SPIBSC_8BIT_WIDTH: 8-bit width • The setting value of this member is set in the ADB[1:0] bit field in the manual mode enable setting register (SMENR).
uint8_t addr_output_enable	Address enable • Specifies whether or not the address is output in manual mode. • Settable values: SPIBSC_OUTPUT_DISABLE: Not output SPIBSC_OUTPUT_ADDR_24: ADR[23:0] output SPIBSC_OUTPUT_ADDR_32: ADR[31:0] output SPIBSC_OUTPUT_ADDR_OCTA: Octal-SPI flash memory address output • The setting value of this member is set in the ADE[3:0] bit field in the manual mode enable setting register (SMENR).
uint8_t addr_sdr_ddr	Address DDR enable • Selects SDR/DDR transfer for the address output in manual mode. • Settable values: SPIBSC_SDR_TRANSFER: SDR transfer SPIBSC_DDR_TRANSFER: DDR transfer • The setting value of this member is set in the ADDRE bit field in the manual mode DDR enable register (SMDRENR).

Table 5.19 SPIBSC Manual Mode Settings Structure (st_spibsc_manual_mode_command_config_t) (3/6)

Member	Description
uint8_t opdata_width	Option data bit width • Specifies the option data bit width in manual mode. • Settable values: SPIBSC_1BIT_WIDTH: 1-bit width SPIBSC_8BIT_WIDTH: 8-bit width • The setting value of this member is set in the OPDB[1:0] bit field in the manual mode enable setting register (SMENR).
uint8_t opdata_output_enable	Option data enable • Specifies whether or not the option data is output in manual mode. • Settable values: SPIBSC_OUTPUT_DISABLE : Not output SPIBSC_OUTPUT_OPD_3 : OPD3 output SPIBSC_OUTPUT_OPD_32 : OPD3, OPD2 output SPIBSC_OUTPUT_OPD_321 : OPD3, OPD2, OPD1 output SPIBSC_OUTPUT_OPD_3210 : OPD3, OPD2, OPD1, OPD0 output • The setting value of this member is set in the OPDE[3:0] bit field in the manual mode enable setting register (SMENR).
uint8_t opdata_ddr_enable	Option data DDR enable • Selects SDR/DDR transfer for the option data output in manual mode. • Settable values: SPIBSC_SDR_TRANSFER: SDR transfer SPIBSC_DDR_TRANSFER: DDR transfer The setting value of this member is set in the OPDRE bit field in the manual mode DDR enable register (SMDRENR).
uint8_t opd3 uint8_t opd2 uint8_t opd1 uint8_t opd0	Option data • Specifies the option data output in manual mode. The setting value of this member is set in the OPD3[7:0], OPD2[7:0], OPD1[7:0], and OPD0[7:0] bit fields in the manual mode option setting register (SMOPR).

Table 5.20 SPIBSC Manual Mode Settings Structure (st_spibsc_manual_mode_command_config_t) (4/6)

Member	Description
uint8_t reserve3	Reserve data This member is not referenced in the sample code.
uint8_t dummy_cycle_output_enable	Dummy cycle enable • Specifies whether or not dummy cycles are inserted in manual mode. • Settable values: SPIBSC_OUTPUT_DISABLE: Not inserted SPIBSC_OUTPUT_ENABLE: Inserted • The setting value of this member is set in the DME bit field in the manual mode enable setting register (SMENR).
uint8_t dummy_cycle_count	Number of dummy cycles • Sets the number of inserted dummy cycles. • Settable values: SPIBSC_DUMMY_02CYC to SPIBSC_DUMMY_20CYC • The setting value of this member is set in the DMCYC[4:0] bit field in the manual mode dummy cycle setting register (SMDMCR).
uint8_t transfer_data_width	Transfer data bit width • Specifies the transfer data bit width in manual mode. • Settable values: SPIBSC_1BIT_WIDTH: 1-bit width SPIBSC_8BIT_WIDTH: 8-bit width • The setting value of this member is set in the SPIDB[1:0] bit field in the manual mode enable setting register (SMENR).
uint8_t transfer_data_sdr_ddr	Transfer data DDR enable • Selects SDR/DDR transfer for the data transferred in manual mode. • Settable values: SPIBSC_SDR_TRANSFER: SDR transfer SPIBSC_DDR_TRANSFER: DDR transfer • The setting value of this member is set in the SPIDRE bit field in the manual mode DDR enable register (SMDRENR).
uint8_t reserve1	Reserve data This member is not referenced in the sample code.
uint8_t reserve2	Reserve data This member is not referenced in the sample code.

Table 5.21 SPIBSC Manual Mode Settings Structure (st_spibsc_manual_mode_command_config_t) (5/6)

Member	Description
uint8_t cmncr_moiio3	Level for QSPIn_IO3 while SSL negated. • Specify the level after finished the data transfer. • Settable values: SPIBSC_QSPI_IO_OUTPUT_0: The output value is 0. SPIBSC_QSPI_IO_OUTPUT_1: The output value is 1. SPIBSC_QSPI_IO_OUTPUT_PREVIOUS: The output value is that of the last bit in the previous transfer (the pin is placed in the Hi-Z state if that was the case in the previous transfer). SPIBSC_QSPI_IO_OUTPUT_HI_Z: The pin is placed in the Hi-Z state. • The setting value of this member is set in the MOIIO3[1:0] bit field in the Common Control Register (CMNCR).
uint8_t cmncr_moiio2	Level for QSPIn_IO2 while SSL negated. • Specify the level after finished the data transfer. • Settable values: SPIBSC_QSPI_IO_OUTPUT_0: The output value is 0. SPIBSC_QSPI_IO_OUTPUT_1: The output value is 1. SPIBSC_QSPI_IO_OUTPUT_PREVIOUS: The output value is that of the last bit in the previous transfer (the pin is placed in the Hi-Z state if that was the case in the previous transfer). SPIBSC_QSPI_IO_OUTPUT_HI_Z: The pin is placed in the Hi-Z state. • The setting value of this member is set in the MOIIO2[1:0] bit field in the Common Control Register (CMNCR).
uint8_t cmncr_moiio1	Level for QSPIn_IO1 while SSL negated. • Specify the level after finished the data transfer. • Settable values: SPIBSC_QSPI_IO_OUTPUT_0: The output value is 0. SPIBSC_QSPI_IO_OUTPUT_1: The output value is 1. SPIBSC_QSPI_IO_OUTPUT_PREVIOUS: The output value is that of the last bit in the previous transfer (the pin is placed in the Hi-Z state if that was the case in the previous transfer). SPIBSC_QSPI_IO_OUTPUT_HI_Z: The pin is placed in the Hi-Z state. • The setting value of this member is set in the MOIIO1[1:0] bit field in the Common Control Register (CMNCR).
uint8_t cmncr_moiio0	Level for QSPIn_IO0 while SSL negated. • Specify the level after finished the data transfer. • Settable values: SPIBSC_QSPI_IO_OUTPUT_0: The output value is 0. SPIBSC_QSPI_IO_OUTPUT_1: The output value is 1. SPIBSC_QSPI_IO_OUTPUT_PREVIOUS: The output value is that of the last bit in the previous transfer (the pin is placed in the Hi-Z state if that was the case in the previous transfer). SPIBSC_QSPI_IO_OUTPUT_HI_Z: The pin is placed in the Hi-Z state. • The setting value of this member is set in the MOIIO0[1:0] bit field in the Common Control Register (CMNCR).

Table 5.22 SPIBSC Manual Mode Settings Structure (st_spibsc_manual_mode_command_config_t) (6/6)

Member	Description
uint8_t cmncr_io3fv	Level for QSPIn_IO3 while 1-bit width transfer. • Specify the level while the data transfer is done by 1-bit width. • Settable values: SPIBSC_QSPI_IO_OUTPUT_0: The output value is 0. SPIBSC_QSPI_IO_OUTPUT_1: The output value is 1. SPIBSC_QSPI_IO_OUTPUT_PREVIOUS: The output value is that of the last bit in the previous transfer (the pin is placed in the Hi-Z state if that was the case in the previous transfer). SPIBSC_QSPI_IO_OUTPUT_HI_Z: The pin is placed in the Hi-Z state. • The setting value of this member is set in the IO3FV[1:0] bit field in the Common Control Register (CMNCR).
uint8_t cmncr_io2fv	Level for QSPIn_IO2 while 1-bit width transfer. • Specify the level while the data transfer is done by 1-bit width. • Settable values: SPIBSC_QSPI_IO_OUTPUT_0: The output value is 0. SPIBSC_QSPI_IO_OUTPUT_1: The output value is 1. SPIBSC_QSPI_IO_OUTPUT_PREVIOUS: The output value is that of the last bit in the previous transfer (the pin is placed in the Hi-Z state if that was the case in the previous transfer). SPIBSC_QSPI_IO_OUTPUT_HI_Z: The pin is placed in the Hi-Z state. • The setting value of this member is set in the IO2FV[1:0] bit field in the Common Control Register (CMNCR).
uint8_t cmncr_io0fv	Level for QSPIn_IO0 while 1-bit width read transfer. • Specify the level while the data read transfer is done by 1-bit width. • Settable values (Note): SPIBSC_QSPI_IO_OUTPUT_0: The output value is 0. SPIBSC_QSPI_IO_OUTPUT_1: The output value is 1. SPIBSC_QSPI_IO_OUTPUT_PREVIOUS: The output value is that of the last bit in the previous transfer (the pin is placed in the Hi-Z state if that was the case in the previous transfer). SPIBSC_QSPI_IO_OUTPUT_HI_Z: The pin is placed in the Hi-Z state. The setting value of this member is set in the IO0FV[1:0] bit field in the Common Control Register (CMNCR).

Note: cmncr_io0fv must be set to "SPIBSC_QSPI_IO_OUTPUT_HI_Z" when data read transfer size is not 1 bit (data_width is not set to "SPIBSC_1BIT_WIDTH").

5.7 List of Variables for Loader Program

Table 5.23 lists the Variables Used in the Loader Program.

Table 5.23 Variables Used in the Loader Program

Variable name	Description	Comments
st_spibsc_xip_config_t gs_read_table[0]	For external address space read mode Settings table data for 8DTRD command in DOPI mode	Refer to Table 6.7
st_spibsc_manual_mode_command_config_t gs_command_table[0]	For manual mode Settings table data for RDSR command in SPI mode	Refer to Table 6.8
st_spibsc_manual_mode_command_config_t gs_command_table[1]	For manual mode Settings table data for RDCR command in SPI mode	Refer to Table 6.10
st_spibsc_manual_mode_command_config_t gs_command_table[2]	For manual mode Settings table data for RDCR2 command in SPI mode	Refer to Table 6.12
st_spibsc_manual_mode_command_config_t gs_command_table[3]	For manual mode Settings table data for WREN command in SPI mode	Refer to Table 6.14
st_spibsc_manual_mode_command_config_t gs_command_table[4]	For manual mode Settings table data for WRSR command in SPI mode	Refer to Table 6.16
st_spibsc_manual_mode_command_config_t gs_command_table[5]	For manual mode Settings table data for WRCR2 command in SPI mode	Refer to Table 6.19
st_spibsc_manual_mode_command_config_t gs_command_table[6]	For manual mode Settings table data for RDID command in SPI mode	Refer to Table 6.21
st_spibsc_manual_mode_command_config_t gs_command_table[7]	For manual mode Settings table data for RDSR command in DOPI mode	Refer to Table 6.9
st_spibsc_manual_mode_command_config_t gs_command_table[8]	For manual mode Settings table data for RDCR command in DOPI mode	Refer to Table 6.11
st_spibsc_manual_mode_command_config_t gs_command_table[9]	For manual mode Settings table data for RDCR2 command in DOPI mode	Refer to Table 6.13
st_spibsc_manual_mode_command_config_t gs_command_table[10]	For manual mode Settings table data for WREN command in DOPI mode	Refer to Table 6.15
st_spibsc_manual_mode_command_config_t gs_command_table[11]	For manual mode Settings table data for WRSR command in DOPI mode	Refer to Table 6.17
st_spibsc_manual_mode_command_config_t gs_command_table[12]	For manual mode Settings table data for WRCR command in DOPI mode	Refer to Table 6.18
st_spibsc_manual_mode_command_config_t gs_command_table[13]	For manual mode Settings table data for WRCR2 command in DOPI mode	Refer to Table 6.20
st_spibsc_manual_mode_command_config_t gs_command_table[14]	For manual mode Settings table data for RDID command in DOPI mode	Refer to Table 6.22
st_spibsc_manual_mode_command_config_t gs_command_table[15]	For manual mode Settings table data for 8DTRD command in DOPI mode	Refer to Table 6.23
st_spibsc_manual_mode_command_config_t gs_command_table[16]	For manual mode Settings table data for SE command in DOPI mode	Refer to Table 6.24
st_spibsc_manual_mode_command_config_t gs_command_table[17]	For manual mode Settings table data for PP command in DOPI mode	Refer to Table 6.25

5.8 List of Functions Used in the Loader Program

The sample code comprises interface functions (API functions) for using peripheral functions, user-defined functions (functions called by API functions) which must be prepared by the user for the purpose of the target system, and sample functions which are necessary for the sample code to operate.

For the functions of the loader program, Table 5.24 lists the Sample Functions, Table 5.25 lists the API Functions, and Table 5.26 lists the User-Defined Functions.

Table 5.24 Sample Functions

Function	Description
reset_handler	Reset handler processing (assembler function)
INITSCT	Program section initialization (assembler function)
R_SC_HardwareSetup	Initial setting of hardware used for booting
r_memclk_setup	Memory clock setting processing

Table 5.25 API Functions

Function	Description
R_SPIBSC_Setup	SPIBSC and OctaFlash initial setting
R_SPIBSC_Init	SPIBSC initial setting
R_SPIBSC_ChangeMode	SPIBSC operating mode setting
R_SPIBSC_SPICMDIssue	Issuance of SPI command to OctaFlash (manual mode)
R_SPIBSC_XipStopAccess	Stop access to OctaFlash
R_SPIBSC_FlushReadCache	Clear SPIBSC read cache
R_CPG_InitialiseHwIf	CPG initialization processing

Table 5.26 User-Defined Functions

Function	Description
Userdef_SPIBSC_OCTAFLASH_SetMode	OctaFlash register setting
Userdef_SPIBSC_OCTAFLASH_ReadStatus	OctaFlash status register read
Userdef_SPIBSC_OCTAFLASH_ReadConfig	OctaFlash configuration register read
Userdef_SPIBSC_OCTAFLASH_WriteStatus	OctaFlash status register and configuration register write
Userdef_SPIBSC_OCTAFLASH_WriteEnable	OctaFlash write enable
Userdef_SPIBSC_OCTAFLASH_WaitReady	OctaFlash write completion wait
Userdef_SPIBSC_OCTAFLASH_ReadConfig2	OctaFlash configuration register 2 read
Userdef_SPIBSC_OCTAFLASH_WriteConfig2	OctaFlash configuration register 2 write
Userdef_SPIBSC_OCTAFLASH_ReadId	OctaFlash ID information read
Userdef_SPIBSC_OCTAFLASH_Read	OctaFlash data read
Userdef_SPIBSC_OCTAFLASH_Erase	OctaFlash sector erase
Userdef_SPIBSC_OCTAFLASH_Write	OctaFlash data write
Userdef_PreHardwareSetup	Necessary hardware initialization processing before the SPIBSC initialization process
Userdef_PostHardwareSetup	Necessary hardware initialization processing after the SPIBSC initialization process

5.9 Function Specification

Specifications of the functions of the loader program are listed below.

reset_handler	
Outline	Reset handler processing
Declaration	reset_handler
Description	The entry function of the loader program.
Arguments	None
Return Value	None

INITSCT		
Outline	Program section initialization	
Declaration	void INITSCT(void)	
Description	The data with initial values which must be transferred to the RAM area (including code and constant data that must be executed in the RAM area) is transferred from the ROM area, and the initialization of the RAM area data with no initial values is performed.	
Arguments	p_dtbl	: Pointer to the area where the section information for data with initial values is stored
	p_btbl	: Pointer to the area where the section information for data with no initial values is stored
Return Value	None	

R_SC_HardwareSetup	
Outline	Initial setting of hardware used for booting
Declaration	void R_SC_HardwareSetup(void)
Description	Makes the optimal settings for the used OctaFlash, sets the SPIBSC to external address space read mode, and accesses the OctaFlash. In the sample code, set the OctaFlash (MX25UM51245G) registers and initialize SPIBSC registers according to the specifications of MX25UM51245G by calling the R_SPIBSC_Setup function.
Arguments	None
Return Value	None
Precautions	This function cannot be assigned to execute from the OctaFlash. This function must be assigned to an area other than the OctaFlash.

r_memclk_setup	
Outline	Memory clock setting processing
Declaration	void r_memclk_setup (void)
Description	Before the R_SC_HardwareSetup function is executed, this function sets the memory clock. In this sample code, no processing is performed.
Argument	None
Return Value	None
Precautions	This function cannot be assigned to execute from the OctaFlash. This function must be assigned to an area other than the OctaFlash.

R_SPIBSC_Setup	
Outline	SPIBSC and OctaFlash initial setting
Declaration	void R_SPIBSC_Setup (void)
Description	Makes the optimal settings for the used OctaFlash, sets the SPIBSC to external address space read mode, and accesses the OctaFlash. The following settings are made in the sample code. • Change to read command: H'03→H'EE • OctaFlash register setting Status register: QE bit set to 1 Configuration register 2 (address H'0000_0000): Set the DOPI bit to 1. Configuration register 2 (address H'0000_0300): DC[2:0] bit settings (The DC[2:0] bit setting differs depending on the read command. Refer to "Table 6.5 List of numbers of dummy cycles necessary for the maximum operating frequency of the MX25UM51245G".) • Change to QSPIn_SPCLK operating frequency: P0ϕ/2→Gϕ/2
Argument	ddrsdr : Specifying transfer mode SDR or DDR HWSETUP_SPIBSC_USE_DDR : DDR mode HWSETUP_SPIBSC_USE_SDR : SDR mode
Return Value	None
Precautions	This function cannot be assigned to execute from the OctaFlash. This function must be assigned to an area other than the OctaFlash.

R_SPIBSC_Init	
Outline	SPIBSC initial setting
Declaration	e_spibsc_err_t R_SPIBSC_Init(const spibsc_config_t *p_spibsc_config_tbl)
Description	The SPIBSC-related register initial setting is made by the argument spibsc_config_tbl. When this function has ended, external address space read mode settings are made. • Driving capability setting of SPIBSC-related pin • SPIBSC module standby cancellation • SPIBSC clock setting • SPIBSC-related register setting
Arguments	const spibsc_config_t *p_spibsc_config_tbl : Pointer to SPIBSC initial setting table
Return Value	SPIBSC_SUCCESS : Normal end
Precautions	This function cannot be assigned to execute from the OctaFlash. This function must be assigned to an area other than the OctaFlash.

R_SPIBSC_ChangeMode		
Outline	SPIBSC operating mode setting	
Declaration	void R_SPIBSC_ChangeMode(uint8_t mode, uint8_t sdr_ddr, uint8_t table_no)	
Description	The operating mode specified by the argument mode allows access to the OctaFlash in the transfer format specified by the arguments sdr_ddr and table_no.	
Arguments	uint8_t mode	: Operating mode SPIBSC_MODE_MANUAL : Manual mode SPIBSC_MODE_XIP : External address space read mode
	uint8_t sdr_ddr	: Transfer format SPIBSC_DDR_TRANSFER : DDR transfer SPIBSC_SDR_TRANSFER : SDR transfer
	uint8_t table_no	: External address space read mode command setting table number 0: Command setting table 0 is selected (DDR read command) 1: Command setting table 1 is selected (SDR read command)
Return Value	None	
Precautions	This function cannot be assigned to execute from the OctaFlash. This function must be assigned to an area other than the OctaFlash.	

R_SPIBSC_SPICMDIssue	
Outline	Issuance of SPI command to OctaFlash (for manual mode)
Declaration	spibsc_err_t R_SPIBSC_SPICMDIssue(uint8_t table_no, uint32_t addr, uint8_t *write_buff, uint32_t write_size, uint8_t *read_buff, uint32_t read_size)
Description	Uses the configuration table for issuing SPI commands specified by the argument table_no to issue SPI commands. According to the contents of table_no, when a write command is issued, the data stored in the argument *write_buff is written, at the number of bytes specified by the argument write_size from the address specified by the argument addr. When a read command is issued, the data is read at the number of bytes specified by the argument read_size from the address specified by the argument addr, and stored in the area specified by the argument *read_buff. Note that if a read command is issued with 8 or larger value specified for read_size as the number of bytes, the SPI command is issued repeatedly to perform read processing.
Arguments	uint8_t table_no : The table storing the setting information for the command used uint32_t addr : Address uint8_t * write_buff : Write buffer pointer uint32_t write_size : Number of bytes to write uint8_t * read_buff : Read buffer pointer uint32_t read_size : Number of bytes to read
Return Value	SPIBSC_SUCCESS : Normal end
Precautions	When a write command is issued, specify 0 for the read_size. When a read command is issued, specify 0 for the write_size. This function cannot be assigned to execute from the OctaFlash. This function must be assigned to an area other than the OctaFlash.

R_SPIBSC_XipStopAccess	
Outline	Stop access to OctaFlash
Declaration	void R_SPIBSC_XipStopAccess(void)
Description	Negates QSPIn_SSL with external address space read mode and stops access to the OctaFlash. When SPIBSC-related register settings are being made, this function is called so that the OctaFlash is not accessed.
Arguments	None
Return Value	None
Precautions	This function cannot be assigned to execute from the OctaFlash. This function must be assigned to an area other than the OctaFlash.

R_SPIBSC_FlushReadCache	
Outline	Clear SPIBSC read cache
Declaration	void R_SPIBSC_FlushReadCache(void)
Description	Clears the SPIBSC read cache.
Arguments	None
Return Value	None
Precautions	This function cannot be assigned to execute from the OctaFlash. This function must be assigned to an area other than the OctaFlash.

R_CPG_InitialiseHwIf		
Outline	CPC initialization processing	
Declaration	int_t R_CPG_InitialiseHwIf(void)	
Description	Uses the r_cpg_drv_sc_cfg.h CPG configuration data to make CPG register (FRQCR, CKIOSEL, SCLKSEL) settings. In this sample code, CPG settings are made so that the operating frequency in "Operating clock settings" and "SPIBSC clock selection" in "Table 5.4 Settings for the boot startup on-chip ROM program and loader program (3/3)" is used.	
Arguments	None	None
Return Value	DRV_SUCCESS	: Normal end
	DRV_ERROR	: r_cpg_drv_sc_cfg.h CPG configuration data is wrong
Precautions	This function must be assigned to the large-capacity on-chip RAM.	

Userdef_SPIBSC_OCTAFLASH_SetMode	
Outline	OctaFlash register setting
Declaration	void Userdef_SPIBSC_OCTAFLASH_SetMode(uint8_t mode, uint8_t sdr_ddr)
Description	Implement a processing that sets to the OctaFlash registers so that access is possible in the transfer format specified by the argument sdr_ddr via access at the bit width specified by the argument mode, according to the specifications of the OctaFlash to be used. In the sample code, MX25UM51245G register settings are made and access is set via DDR transfer at 4-bit width.
Arguments	uint8_t mode : Operating mode SPIBSC_OCTA_OPI_DISABLE: Single mode (bit width: 1 bit) SPIBSC_OCTA_OPI_ENABLE: OPI mode (bit width: 8 bits) uint8_t sdr_ddr : Transfer format SPIBSC_DDR_TRANSFER: DDR transfer SPIBSC_SDR_TRANSFER: SDR transfer (unsupported)
Return Value	None
Precautions	This function cannot be assigned to execute from the OctaFlash. This function must be assigned to an area other than the OctaFlash.

Userdef_SPIBSC_OCTAFLASH_ReadStatus	
Outline	OctaFlash status register read
Declaration	void Userdef_SPIBSC_OCTAFLASH_ReadStatus(uint8_t *p_status)
Description	Implement a processing to read the OctaFlash status register and to store the data read with the argument *p_status, according to the specifications of the OctaFlash to be used. In the sample code, a processing to read the status register of MX25UM51245G is performed.
Arguments	uint8_t *p_status : The value read from the status register
Return Value	None
Precautions	This function cannot be assigned to execute from the OctaFlash. This function must be assigned to an area other than the OctaFlash.

Userdef_SPIBSC_OCTAFLASH_ReadConfig	
Outline	OctaFlash configuration register read
Declaration	void Userdef_SPIBSC_OCTAFLASH_ReadConfig(uint8_t *p_config)
Description	Implement a processing to read the OctaFlash configuration register and to store the data read with the argument *p_config, according to the specifications of the OctaFlash to be used. In the sample code, a processing to read the configuration register of MX25UM51245G is performed.
Arguments	uint8_t *p_config : The value read from the configuration register
Return Value	None
Precautions	This function cannot be assigned to execute from the OctaFlash. This function must be assigned to an area other than the OctaFlash.

Userdef_SPIBSC_OCTAFLASH_WriteStatus	
Outline	OctaFlash status register and configuration register write
Declaration	void Userdef_SPIBSC_OCTAFLASH_WriteStatus(uint8_t *p_status, uint8_t *p_config)
Description	Implement a processing that sets the values specified by the arguments *p_status and *p_config to the OctaFlash status register and configuration register respectively, according to the specifications of the OctaFlash to be used. In the sample code, a processing to read the status register and configuration register of MX25UM51245G is performed.
Arguments	uint8_t *p_status : Setting in status register uint8_t *p_config : Setting in config register
Return Value	None
Precautions	This function cannot be assigned to execute from the OctaFlash. This function must be assigned to an area other than the OctaFlash.

Userdef_SPIBSC_OCTAFLASH_WriteEnable	
Outline	OctaFlash write enable
Declaration	void Userdef_SPIBSC_OCTAFLASH_WriteEnable(void)
Description	Implement the processing that enables the OctaFlash for writes, according to the specifications of the OctaFlash to be used. In the sample code, processing to issue "Write Enable Register (WREN)" commands to MX25UM51245G is performed.
Arguments	None
Return Value	None
Precautions	This function cannot be assigned to execute from the OctaFlash. This function must be assigned to an area other than the OctaFlash.

Userdef_SPIBSC_OCTAFLASH_WaitReady	
Outline	OctaFlash write completion wait
Declaration	void Userdef_SPIBSC_OCTAFLASH_WaitReady(void)
Description	Implement the processing that waits for the write to the OctaFlash to be completed, according to the specifications of the OctaFlash to be used. In the sample code, processing to issue "Read Status Register (RDSR)" commands to MX25UM51245G and to wait for the write to be completed is performed by referencing the status register contents.
Arguments	None
Return Value	None
Precautions	This function cannot be assigned to execute from the OctaFlash. This function must be assigned to an area other than the OctaFlash.

Userdef_SPIBSC_OCTAFLASH_ReadConfig2	
Outline	OctaFlash configuration register 2 read
Declaration	void Userdef_SPIBSC_OCTAFLASH_ReadConfig2(uint32_t addr, unit8_t *p_config)
Description	Implement a processing to read OctaFlash configuration register 2 and to store the data read in the argument *p_config, according to the specifications of the OctaFlash to be used. In the sample code, a processing to read configuration register 2 of MX25UM51245G is performed.
Arguments	uint32_t addr : The address of configuration register 2 uint8_t *p_config : The value read from configuration register 2
Return Value	None
Precautions	This function cannot be assigned to execute from the OctaFlash. This function must be assigned to an area other than the OctaFlash.

Userdef_SPIBSC_OCTAFLASH_WriteConfig2	
Outline	OctaFlash configuration register 2 write
Declaration	void Userdef_SPIBSC_OCTAFLASH_WriteConfig2(uint32_t addr, unit8_t config)
Description	Implement a processing that sets the value specified by the argument config to OctaFlash configuration register 2, according to the specifications of the OctaFlash to be used. In the sample code, a processing to write configuration register 2 of MX25UM51245G is performed.
Arguments	uint32_t addr : The address of configuration register 2 unit8_t config : Setting in configuration register 2
Return Value	None
Precautions	This function cannot be assigned to execute from the OctaFlash. This function must be assigned to an area other than the OctaFlash.

Userdef_SPIBSC_OCTAFLASH_ReadId	
Outline	OctaFlash ID information read
Declaration	void Userdef_SPIBSC_OCTAFLASH_ReadId(unit8_t *p_id)
Description	Implement a processing to read the OctaFlash ID information and to store the value read with the argument *p_id, according to the specifications of the OctaFlash to be used. In the sample code, a processing to read the ID information of MX25UM51245G is performed.
Arguments	uint8_t *p_id : Pointer to store the read value of ID information
Return Value	None
Precautions	This function cannot be assigned to execute from the OctaFlash. This function must be assigned to an area other than the OctaFlash.

Userdef_SPIBSC_OCTAFLASH_Read	
Outline	OctaFlash data read
Declaration	void Userdef_SPIBSC_OCTAFLASH_Read(uint32_t addr, unit8_t *p_read_buff, int32_t read_size, unit8_t sdr_ddr)
Description	Implement a processing to read the OctaFlash data and to store the data read with the argument *p_read_buff, according to the specifications of the OctaFlash to be used. In the sample code, a processing to read the data from MX25UM51245G is performed.
Arguments	uint32_t addr : Address of the data to be read unit8_t *p_read_buff : Pointer to store the read data int32_t read_size : Number of bytes to read unit8_t sdr_ddr : Transfer format This is not used in this function.
Return Value	None
Precautions	This function cannot be assigned to execute from the OctaFlash. This function must be assigned to an area other than the OctaFlash.

Userdef_SPIBSC_OCTAFLASH_Erase	
Outline	OctaFlash sector erase
Declaration	void Userdef_SPIBSC_OCTAFLASH_Erase(unit32_t addr)
Description	Implement a processing to erase the OctaFlash sector to which the argument addr belongs, according to the specifications of the OctaFlash to be used. In the sample code, a processing to erase the sector of MX25UM51245G is performed.
Arguments	uint32_t addr : Address of the sector to be erased
Return Value	None
Precautions	Before this function is executed, OctaFlash must be set to enable write operation. This function cannot be assigned to execute from the OctaFlash. This function must be assigned to an area other than the OctaFlash.

Userdef_SPIBSC_OCTAFLASH_Write	
Outline	OctaFlash data write
Declaration	void Userdef_SPIBSC_OCTAFLASH_Write(uint32_t addr, unit8_t *p_write_buff, int32_t write_size, unit8_t sdr_ddr)
Description	Implement a processing to program the data of the argument p_write_buff to the address of the OctaFlash indicated by the argument addr according to the specifications of the OctaFlash to be used. In the sample code, a processing to write the data to MX25UM51245G is performed.
Arguments	uint32_t addr : Address to be written unit8_t *p_write_buff : Pointer to store the read data int32_t write_size : Number of bytes to write unit8_t sdr_ddr : Transfer format This is not used in this function.
Return Value	None
Precautions	Before this function is executed, OctaFlash must be set to enable write operation. In the sample code, the Page Program command is issued to perform write processing. Therefore, specify the 256-byte boundary address for the argument addr and 256 or smaller value for the argument write_size as the number of bytes. This function cannot be assigned to execute from the OctaFlash. This function must be assigned to an area other than the OctaFlash.

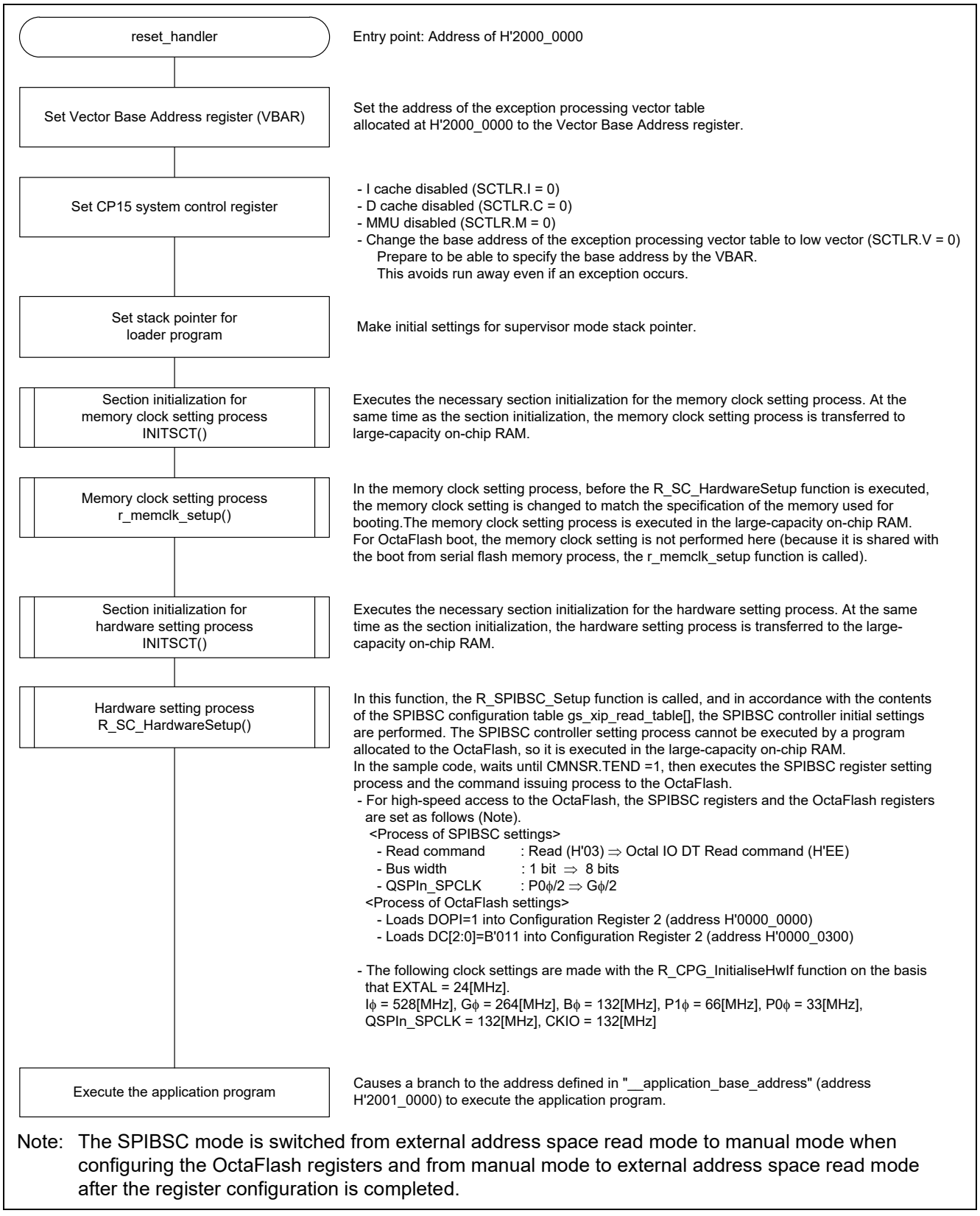
Userdef_PreHardwareSetup	
Outline	Necessary hardware initialization processing before the SPIBSC initialization process
Declaration	void Userdef_PreHardwareSetup (void)
Description	This is the user definable function to describe the hardware initialization process which is required to be executed before the SPIBSC initialization. Nothing is performed in the sample code.
Argument	None
Return Value	None
Precautions	If this function contains processes that cannot be executed from the OctaFlash, this function must be assigned to an area other than the OctaFlash.

Userdef_PostHardwareSetup	
Outline	Necessary hardware initialization processing after the SPIBSC initialization process
Declaration	void Userdef_PostHardwareSetup (void)
Description	This is the user definable function to describe the hardware initialization process which is required to be executed after the SPIBSC initialization. It is called at the end of the R_SC_HardwareSetup function. In the loader program, Make the following CPG settings, on the assumption that 24[MHz] is input from EXTAL by calling R_CPG_InitialiseHwIf function. • Iϕ = 528[MHz], Gϕ = 264[MHz], Bϕ = 132[MHz], P1ϕ = 66[MHz], P0ϕ = 33[MHz], QSPI0_SPCLK = 132[MHz]
Argument	None
Return Value	None
Precautions	If this function contains processes that cannot be executed from the OctaFlash, this function must be assigned to an area other than the OctaFlash.

5.10 Loader Program Flowcharts

5.10.1 Loader program (overall)

Figure 5.4 shows the Flowchart of loader program (overall).



Note: The SPIBSC mode is switched from external address space read mode to manual mode when configuring the OctaFlash registers and from manual mode to external address space read mode after the register configuration is completed.

Figure 5.4 Flowchart of loader program (overall)

5.10.2 Initial setting of hardware used for booting

This function performs the hardware initial setting. In order to enable high-speed access to the OctaFlash in the loader program, the R_SPIBSC_Setup function is called, and the SPIBSC and OctaFlash settings are performed.

Because a program allocated to the SPI multi-I/O bus space cannot execute the setting process of SPIBSC registers and OctaFlash registers, the program is loaded into the large-capacity on-chip RAM and executed from there.

Figure 5.5 shows the Flowchart of initial setting for hardware.

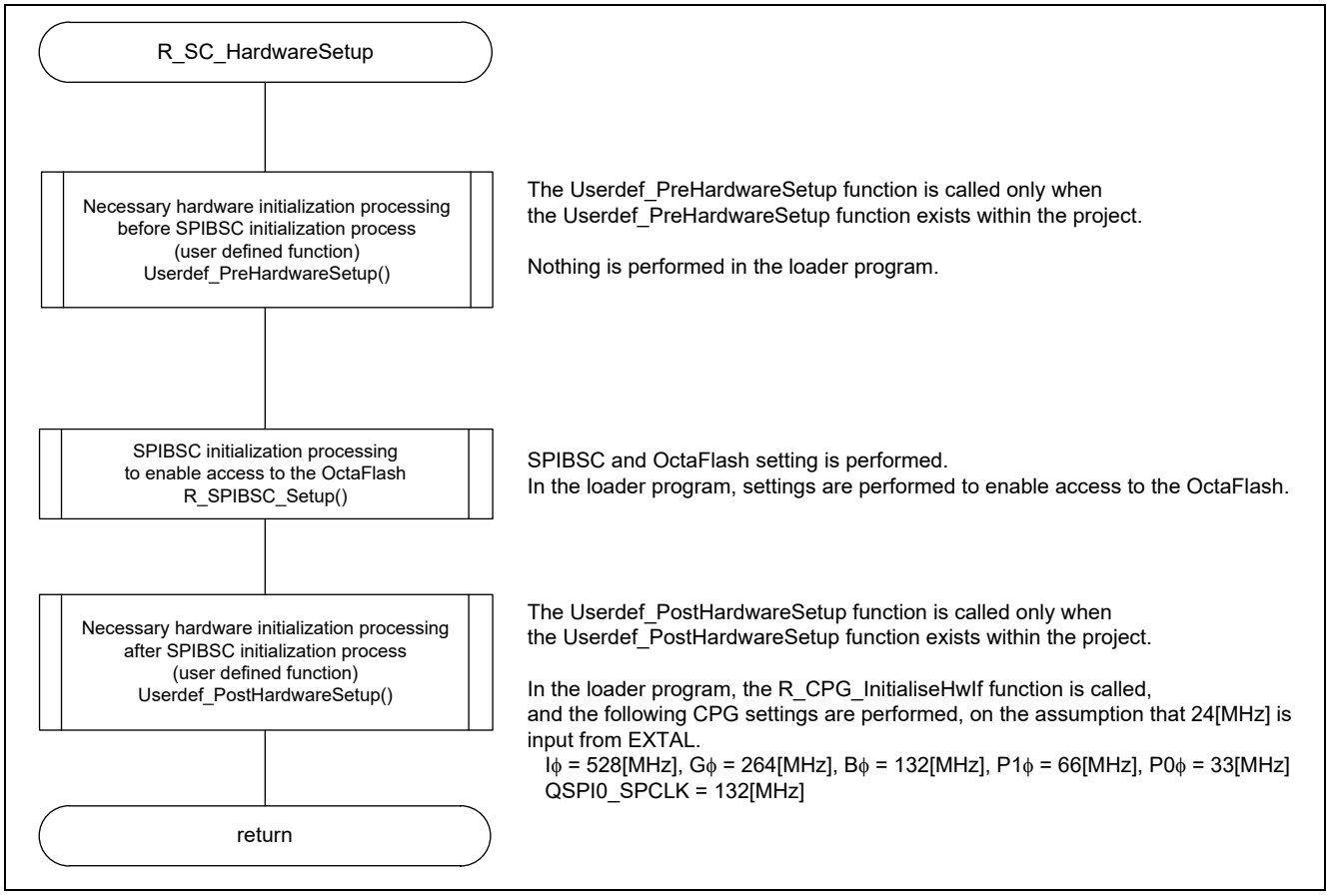


Figure 5.5 Flowchart of initial setting for hardware

5.10.3 SPIBSC and OctaFlash Initial Setting

The loader program sets up the OctaFlash registers (DOPI bit of the configuration register 2 (address H'0000_0000), and DC[2:0] bits of the configuration register 2 (address H'0000_0300)), enables the DTR OPI mode, and changes the number of dummy cycles to 14 so that the OctaFlash can be accessed at a higher speed. After setting up the OctaFlash registers, the program sets the type of read command to be issued to the OctaFlash when using the SPIBSC in external address space read mode to "Octa I/O DT Read" (H'EE) and changes the QSPIn_SPCLK clock frequency to Gϕ/2.

Since the loader program modifies the SPIBSC registers during its processing, it cannot run in the SPI multi-I/O bus space. Accordingly, it is transferred in large-capacity on-chip RAM for execution.

Figure 5.6 shows the Flowchart of SPIBSC and OctaFlash initial setting, and Figure 5.7 to Figure 5.17 show the flowcharts of the used functions.

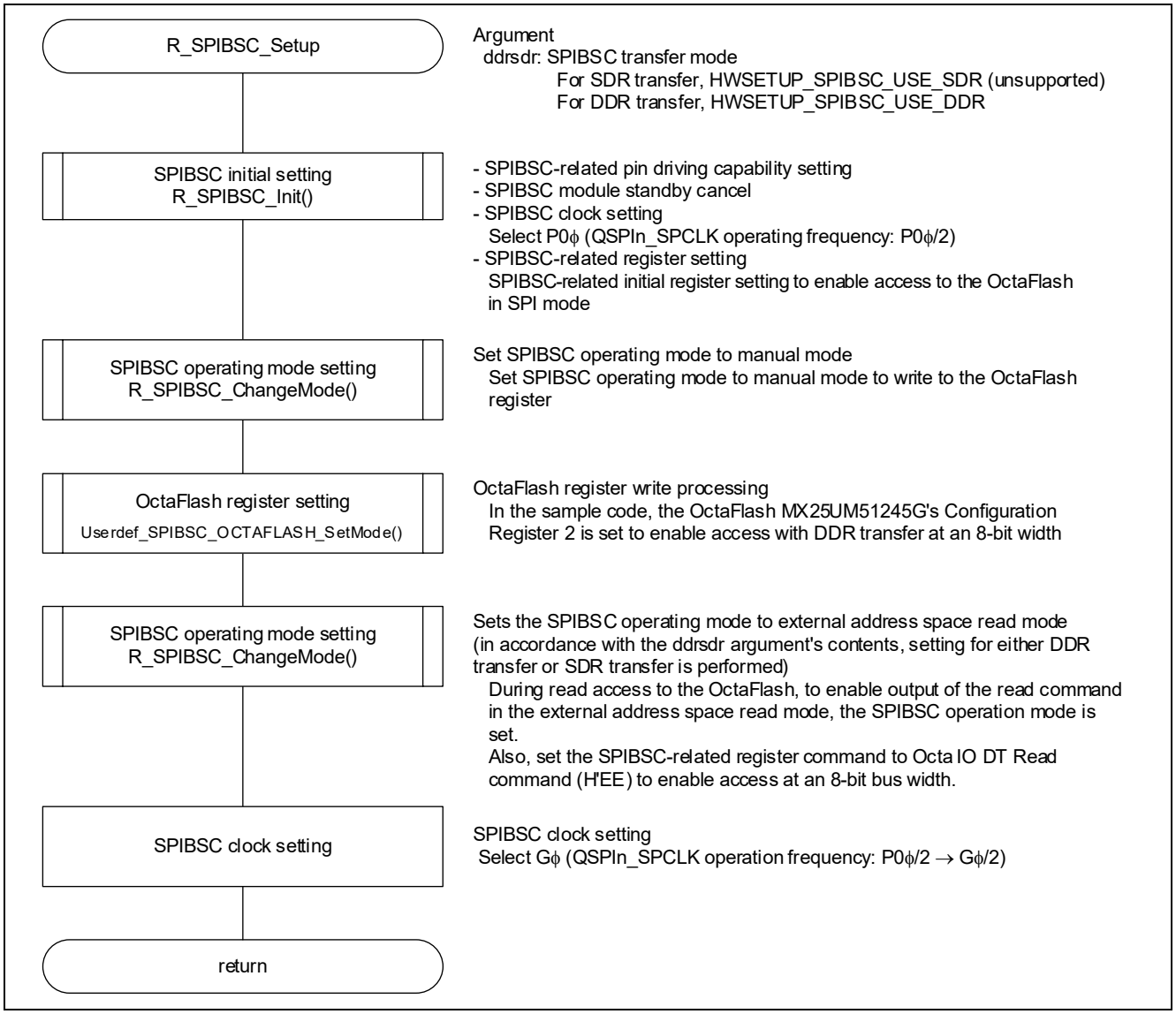


Figure 5.6 Flowchart of SPIBSC and OctaFlash initial setting

5.10.4 SPIBSC Initial Setting

Figure 5.7 and Figure 5.8 show the flowchart of the SPIBSC initial setting. The loader program performs the SPIBSC initial setting to access OctaFlash in SPI mode.

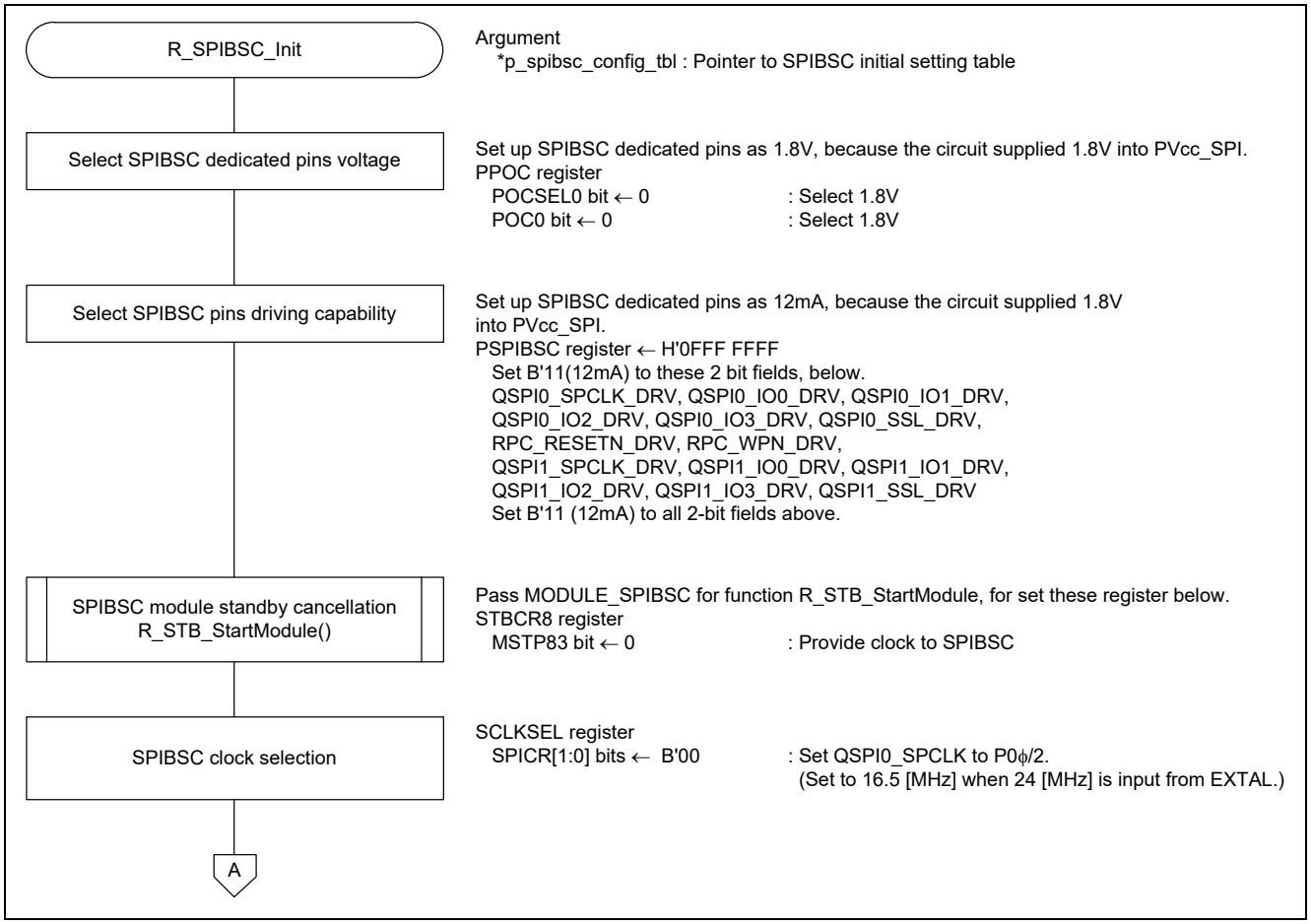


Figure 5.7 Flowchart of SPIBSC initial setting (1/2)

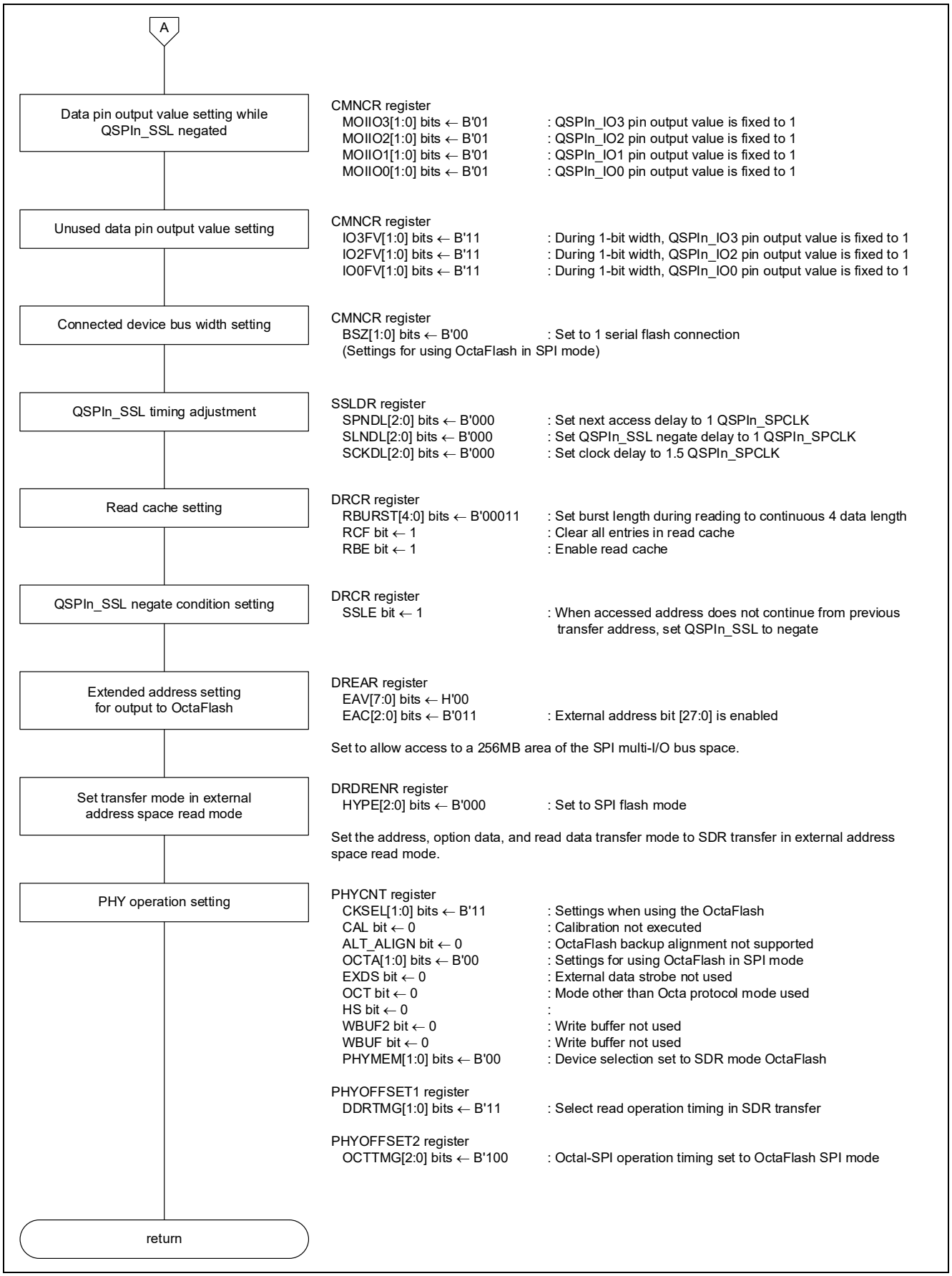


Figure 5.8 Flowchart of SPIBSC initial setting (2/2)

5.10.5 SPIBSC Operating Mode Setting

Figure 5.9 to Figure 5.11 show the SPIBSC operating mode setting.

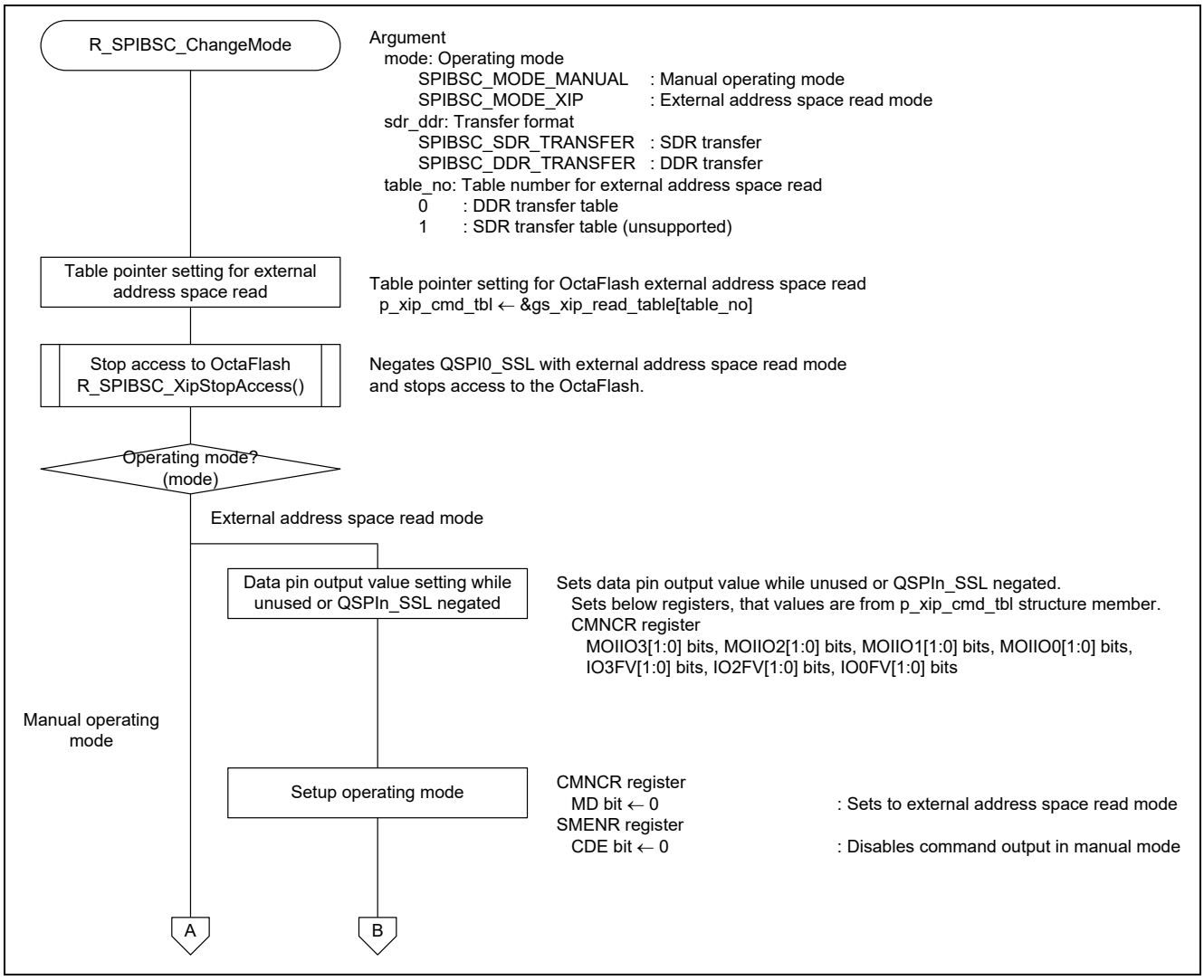


Figure 5.9 Flowchart of SPIBSC operating mode setting (1/3)

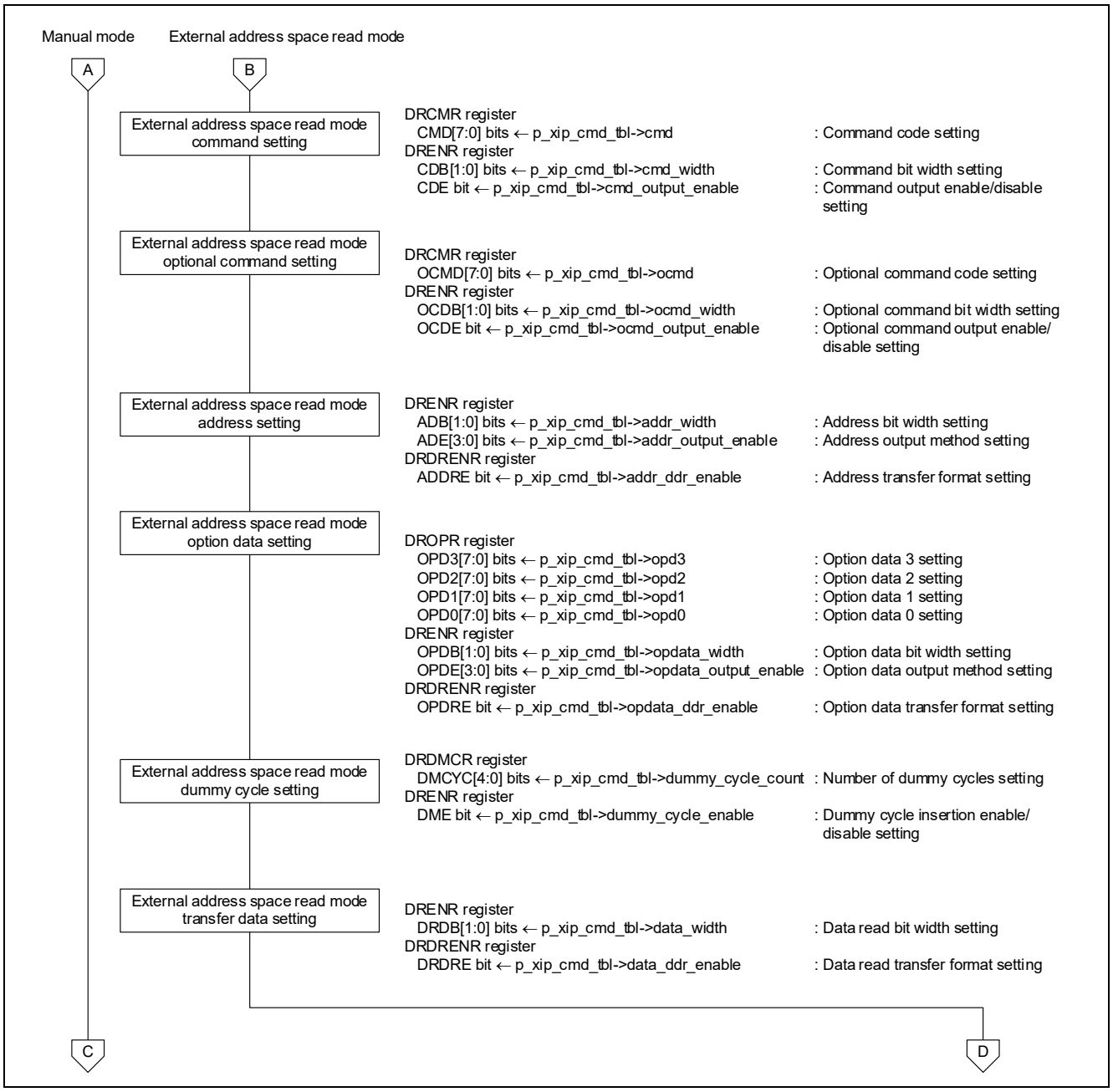


Figure 5.10 Flowchart of SPIBSC operating mode setting (2/3)

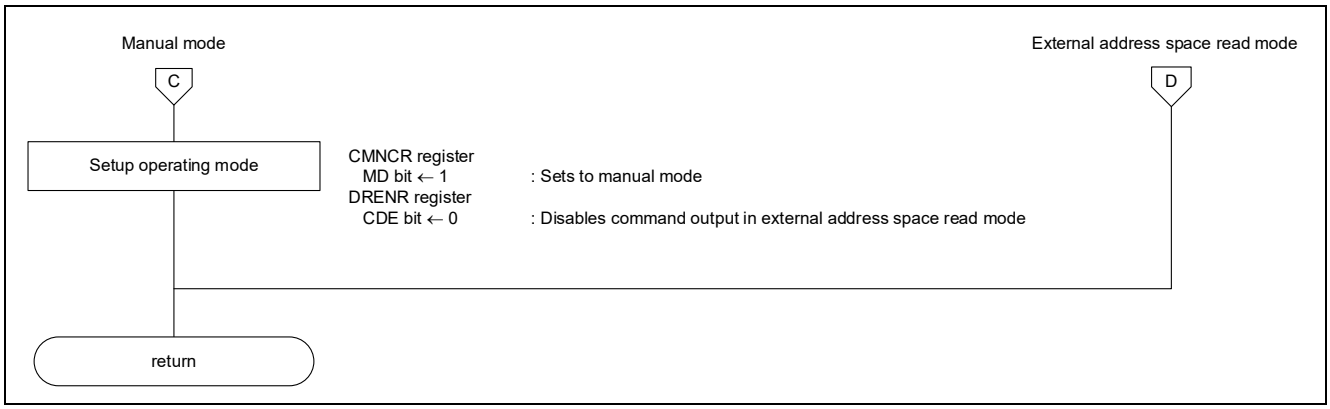


Figure 5.11 Flowchart of SPIBSC operating mode setting (3/3)

5.10.6 Issuance of SPI Command to OctaFlash

Figure 5.12 to Figure 5.17 show the Flowchart for the issuance of an SPI command to OctaFlash. Use this function in manual mode.

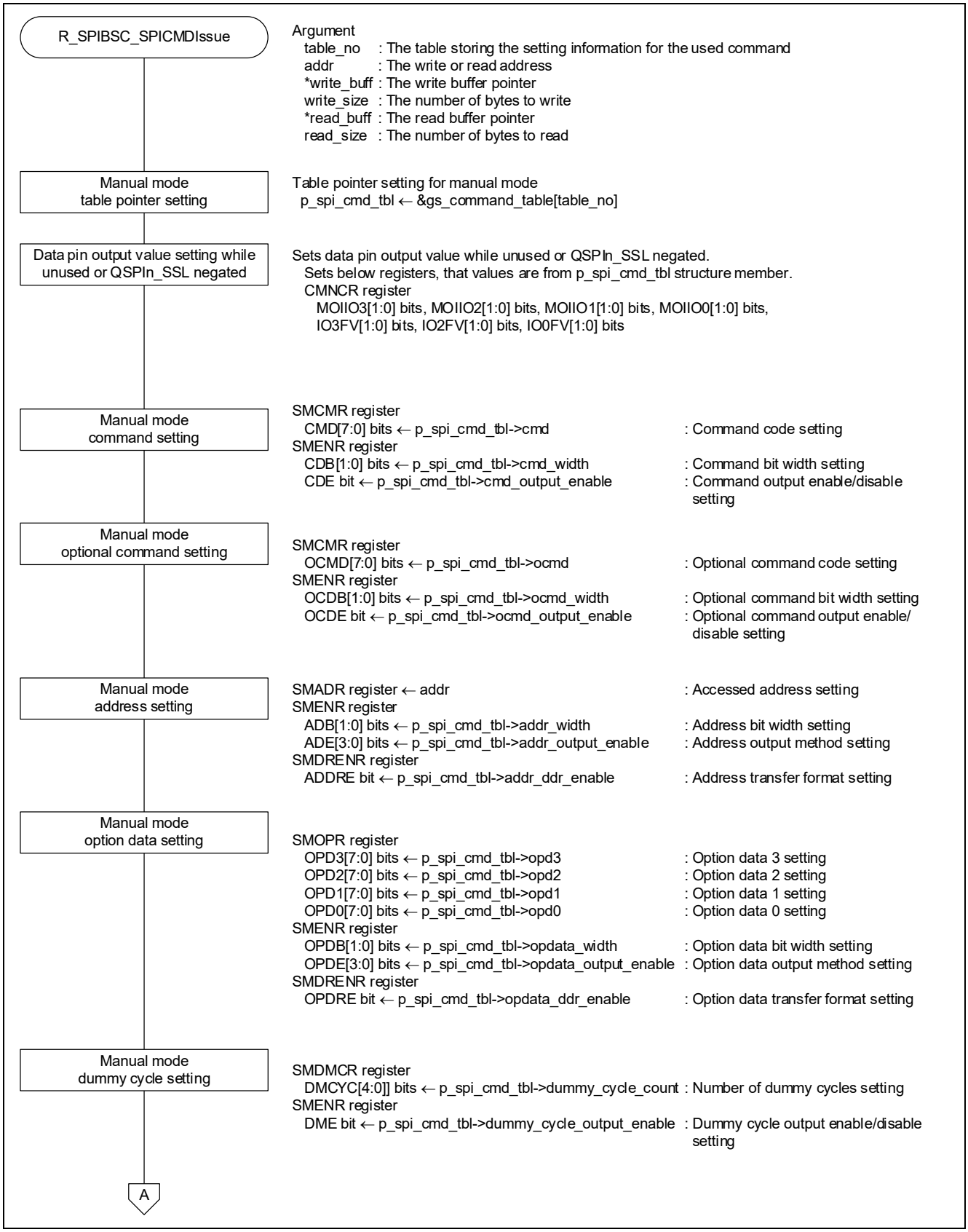


Figure 5.12 Flowchart of issuance of SPI command to OctaFlash (1/6)

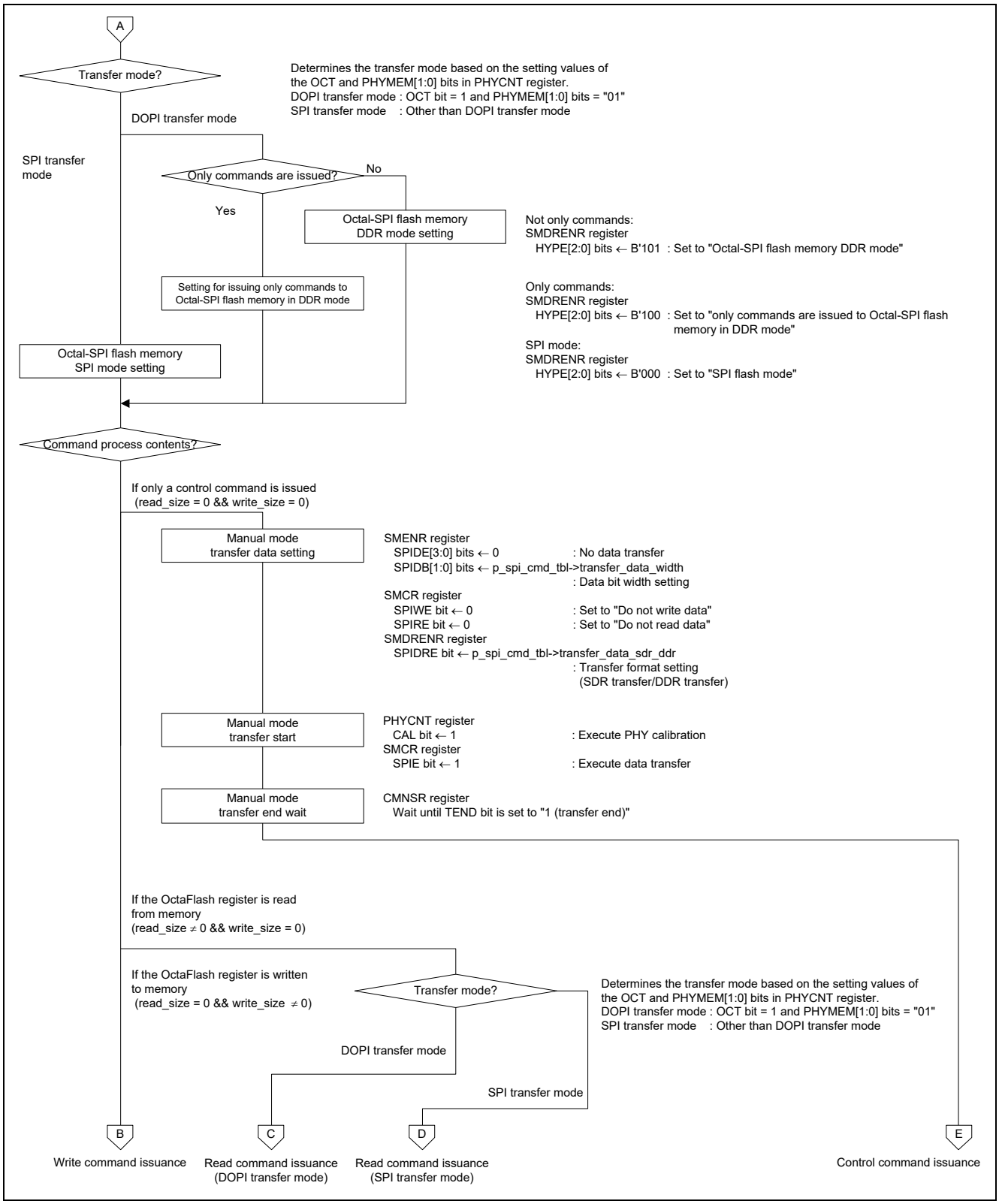


Figure 5.13 Flowchart of issuance of SPI command to OctaFlash (2/6)

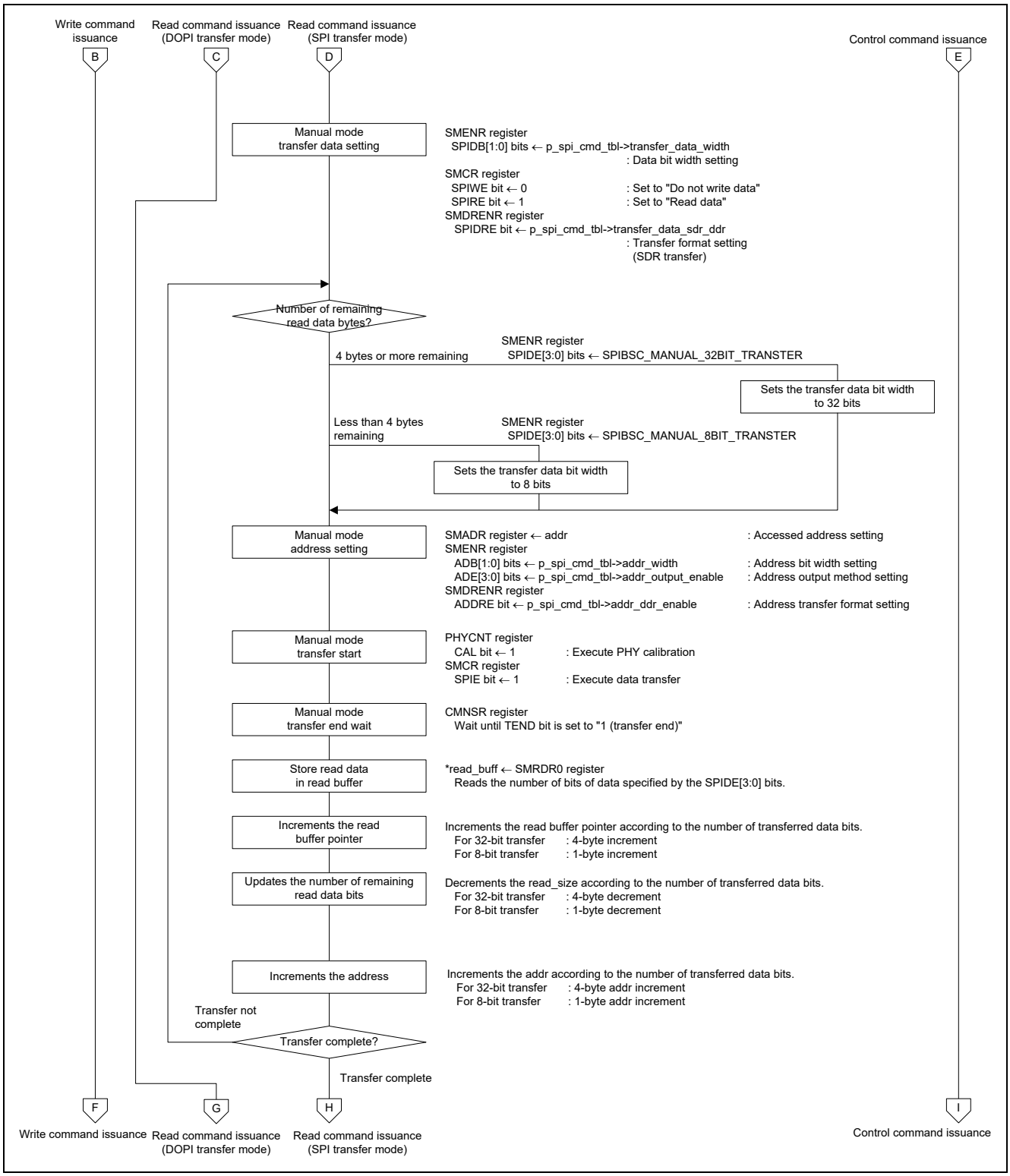


Figure 5.14 Flowchart of issuance of SPI command to OctaFlash (3/6)

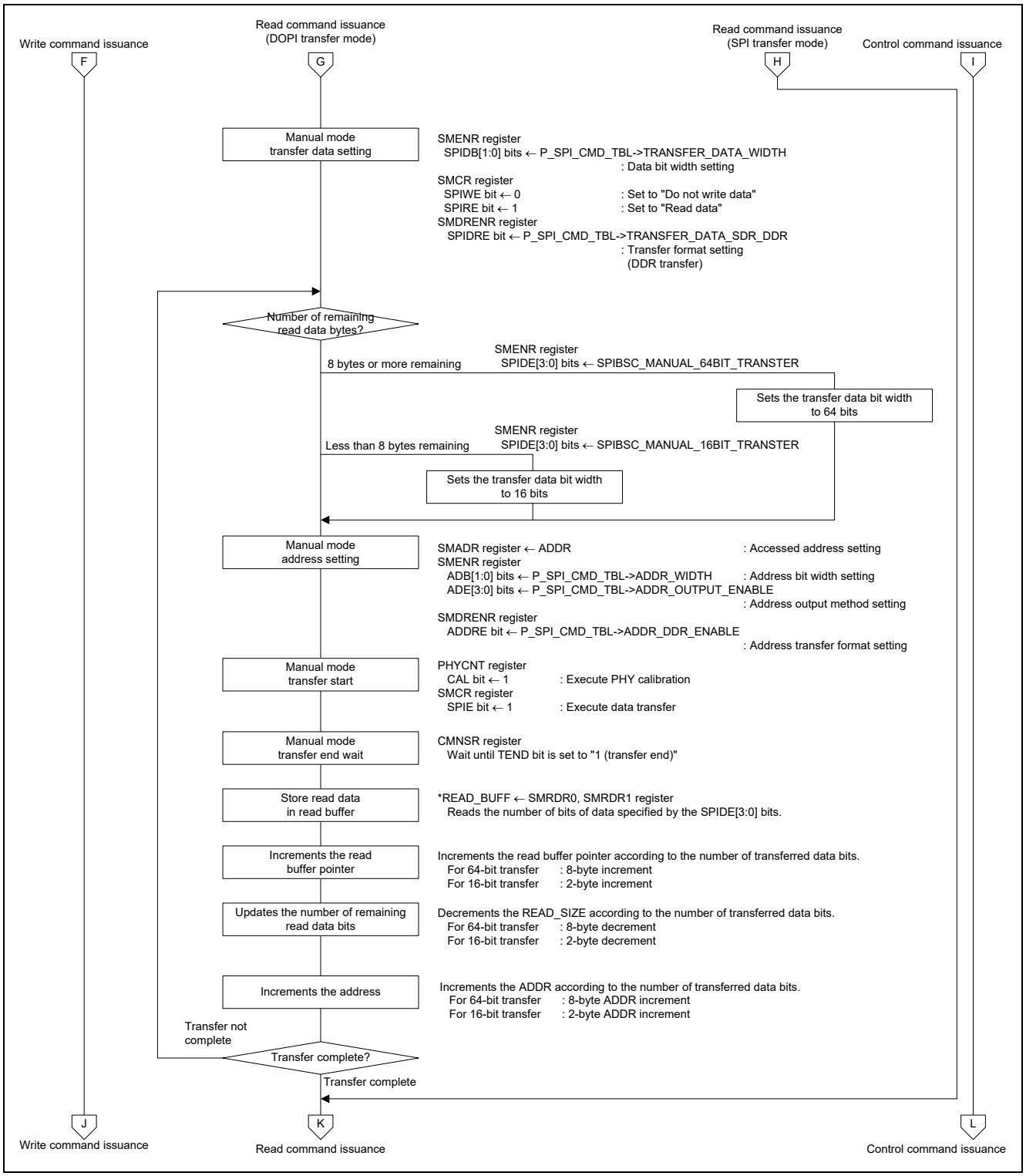


Figure 5.15 Flowchart of issuance of SPI command to OctaFlash (4/6)

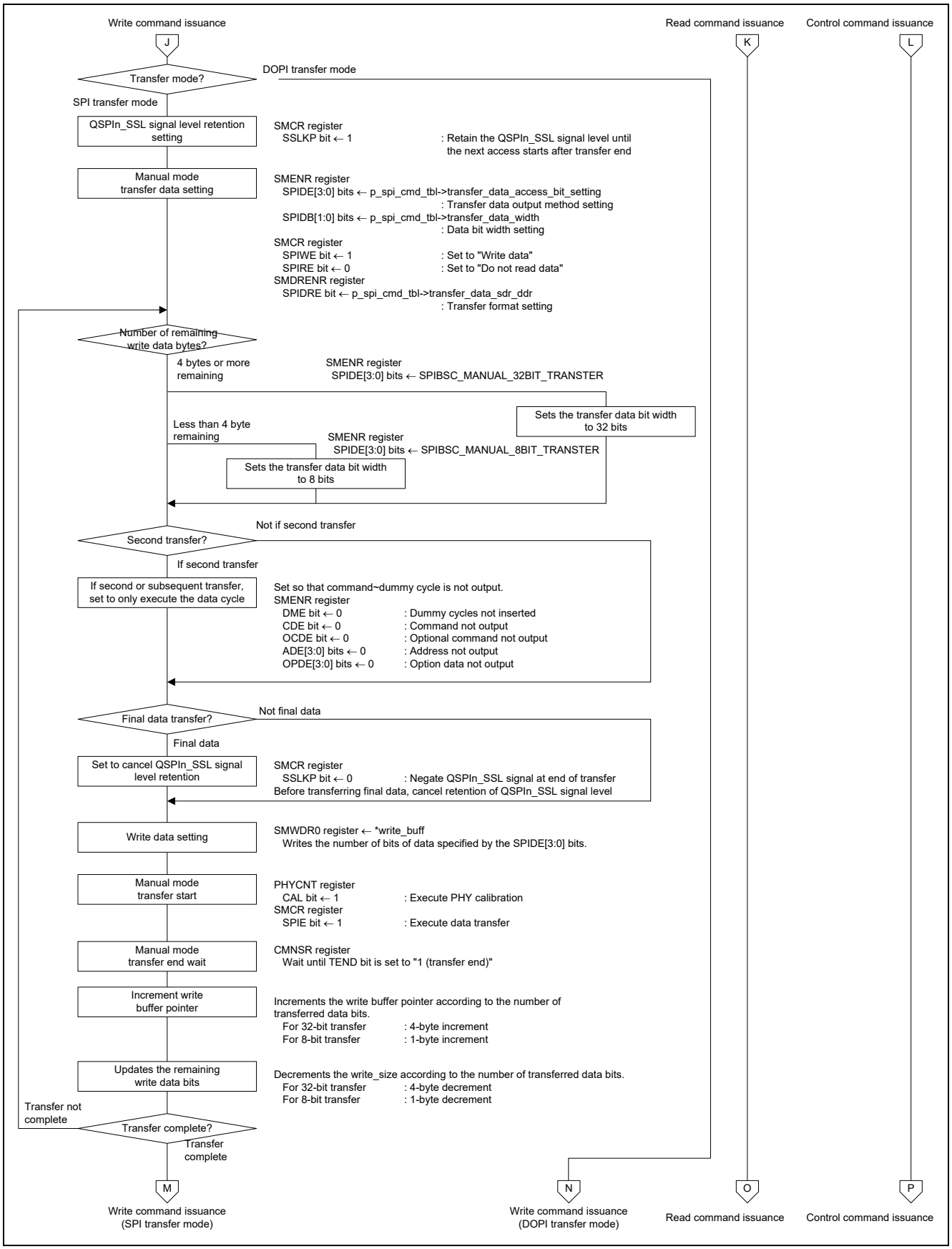


Figure 5.16 Flowchart of issuance of SPI command to OctaFlash (5/6)

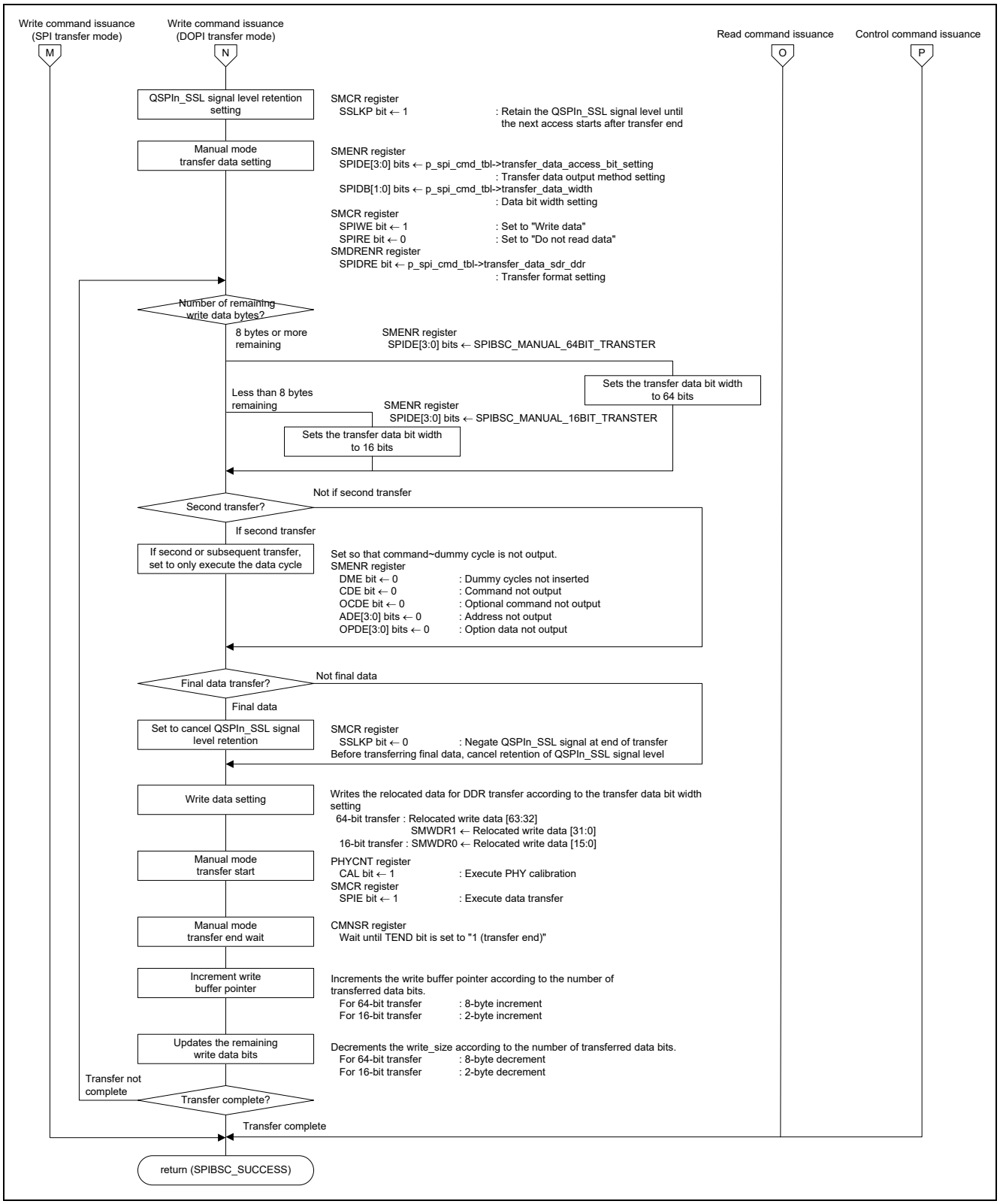


Figure 5.17 Flowchart of issuance of SPI command to OctaFlash (6/6)

6. Application Example

6.1 Operation of the Sample Code Used in its Initial State

The sample code in its initial state accesses the Macronix OctaFlash (product No.: MX25UM51245G) according to the settings that are summarized in Table 6.1.

Table 6.1 Sample Code Access Settings

Item	Setting
OctaFlash	• Macronix OctaFlash • Model name: MX25UM51245G • Read command used: H'EE (8DTRD) 8-bit bus, DTR-OPI mode Number of dummy cycles required: 14 (When running at a maximum operating frequency of 132MHz)
SPIBSC	• Device to be connected: Octal-SPI flash • Data bus width: 4 bits (8-bit width) • Number of address bytes: 4 bytes (Number of bytes to be issued when specifying an address) • Transfer format: DDR transfer

Figure 6.1 shows the Read operation in DDR transfer mode (initial state of the sample code). Table 6.2 shows the Register settings for sample code. In DOPI mode of OctaFlash, commands, optional commands, addresses, and data are transferred in DDR mode on the 8-bit bus width.

The SPIBSC starts outputting data at assertion of QSPI0_SSL and outputs data at both the falling and rising edges of the clock. MX25UM51245G starts sampling data at the rising edge of the first clock after assertion of QSPI0_SSL output from the SPIBSC and thereafter inputs data at both edges of the clock.

The MX25UM51245G starts outputting data at the rising edge of the first data strobe (DQS) and thereafter outputs data at both edges of the data strobe. The SPIBSC detects the start of data output processing at the first rising edge of the data strobe (QSPI1_SSL) and thereafter samples data at both edges.

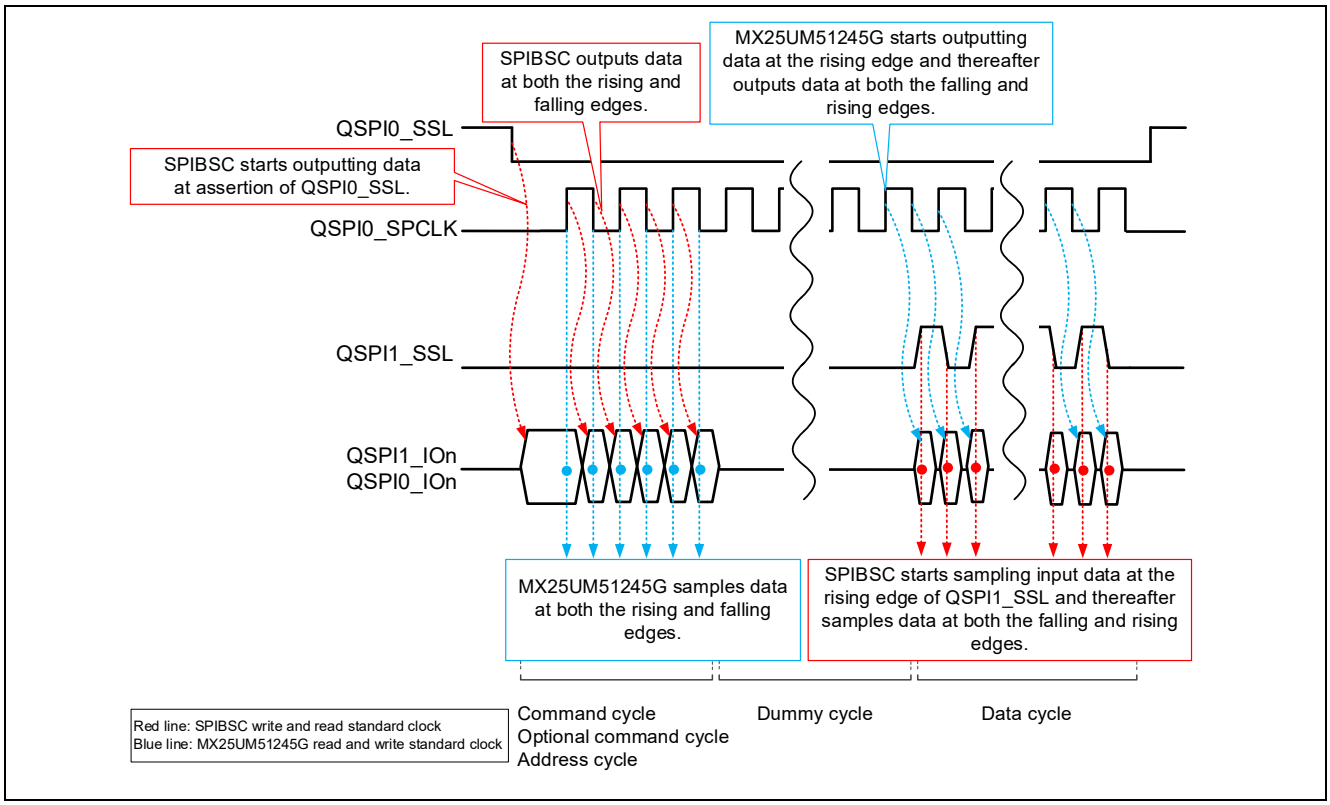


Figure 6.1 Read operation in DDR transfer mode (initial state of the sample code)

In the sample code, the settings shown in Table 6.2 are made in the SPIBSC and OctaFlash registers in the initial state, and operations in DOPI mode are performed.

Table 6.2 Register settings for sample code

Setting	Setting value for sample code
Read command setting	DRCMR.CMD[7:0] = 0xEE DRENR.CDB[1:0] = SPIBSC_8BIT_WIDTH DRENR.CDE = SPIBSC_OUTPUT_ENABLE
Optional command setting	DRCMR.OCMD[7:0] = 0x11 DRENR.OCDB[1:0] = SPIBSC_8BIT_WIDTH DRENR.OCDE = SPIBSC_OUTPUT_DISABLE
Address setting	DRENR.ADB[1:0] = SPIBSC_8BIT_WIDTH DRENR.ADE[3:0] = SPIBSC_OUTPUT_ADDR_OCTA DRDRENR.ADDRE = SPIBSC_DDR_TRANSFER
Option data setting	DRENR.OPDB[1:0] = SPIBSC_8BIT_WIDTH DRENR.OPDE[3:0] = SPIBSC_OUTPUT_DISABLE DRDRENR.OPDRE = SPIBSC_DDR_TRANSFER DROPR.OPD3[7:0] = 0x00
Dummy cycle setting	DRENR.DME = SPIBSC_OUTPUT_ENABLE DRDMCR.DMCYC[4:0] = SPIBSC_DUMMY_14CYC
Transfer data setting	DRENR.DRDB[1:0] = SPIBSC_8BIT_WIDTH DRDRENR.DRDRE = SPIBSC_DDR_TRANSFER
Configuration register 2 setting	DC[2:0] bits = b'011 (14 cycles) DOPI bit = 1 (DTR OPI enable)

The sample code calls the user-defined function Userdef_SPIBSC_OCTAFLASH_SetMode to set up the OctaFlash registers within the R_SC_HardwareSetup function which is executed during initialization, after switching to manual mode with the R_SPIBSC_ChangeMode function. The Userdef_SPIBSC_OCTAFLASH_SetMode function configures the configuration register 2 of the OctaFlash according to the specifications for the read command to be used.

Table 6.3 shows MX25UM51245G configuration register 2 (address H'0000_0000) and Table 6.4 shows MX25UM51245G configuration register 2 (address H'0000_0300).
The Userdef_SPIBSC_OCTAFLASH_SetMode function is used to set the values denoted by " " in the tables.

Table 6.3 MX25UM51245G configuration register 2 (address H'0000_0000)

Bit position	Bit name	Attribute (Note)	Description
7 to 2	Reserved	—	Reserved
1	DOPI	V	B'00 = SPI B'01 = STR OPI enable B'10 = DTR OPI enable B'11 = inhibit
0	SOPI	V	

Note: "V" in the attribute column denotes "Volatile bit".

Table 6.4 MX25UM51245G configuration register 2 (address H'0000_0300)

Bit position	Bit name	Attribute (Note 1)	Description
7 to 3	Reserved	—	Reserved
2,1,0	DC	V	Dummy cycle B'011 (number of dummy cycles: 14) (Note 2)

Note: 1. "V" in the attribute column denotes "Volatile bit".
2. As shown in Table 6.5, the number of dummy cycles differs depending on the operating frequency.

Table 6.5 shows a List of numbers of dummy cycles necessary for the maximum operating frequency of the MX25UM51245G. As shown in the table, the number of necessary dummy cycles differs depending on the operating frequency to be used. Since the sample code uses the H'EE command as the read command and sets QSPIn_SPCLK to 132 MHz, its optimum setting is DC[2:0] = B'011 which yields a dummy cycle count of 14 cycles.

Table 6.5 List of numbers of dummy cycles necessary for the maximum operating frequency of the MX25UM51245G

DC[2:0] bit	Number of Dummy Cycles	Maximum Operating Frequency (MHz)
000 (default)	20	200
001	18	166
010	16	166
011	14	133
100	12	104
101	10	104
110	8	84
111	6	66

6.2 Changing the Sample Code When Changing the OctaFlash

When changing the OctaFlash, the sample code should be changed according to the specifications of the OctaFlash to be used.

Table 6.6 lists the Points for changing sample code.

Table 6.6 Points for changing sample code

Change point	Description	Related section number
Signal Output when a Read Command is Issued in External Address Space Read Mode	Change the output signal to be sent to the OctaFlash when a read command is issued in external address space read mode according to the specifications for the OctaFlash read command to be used.	6.2.1
Signal Output When a Command is Issued in Manual Mode	Change the output signal to be sent to the OctaFlash when a command is issued in manual mode according to the OctaFlash to be used.	6.2.2
Setting up the OctaFlash Registers	The settings for the registers in the OctaFlash required to use the SPIBSC in external address space read mode are made according to the OctaFlash to be used.	6.2.3
OctaFlash Write Completion Wait	Wait for the write to the OctaFlash to be completed according to the OctaFlash to be used.	6.2.4
OctaFlash Status Register Read	Read the status registers in the OctaFlash according to the OctaFlash to be used.	6.2.5
OctaFlash Configuration Register Read	Read the configuration registers in the OctaFlash according to the OctaFlash to be used.	6.2.6
OctaFlash Configuration Register 2 Read	Read the configuration register 2 in the OctaFlash according to the OctaFlash to be used.	6.2.7
OctaFlash Write Enable	The settings for the registers in the OctaFlash are made to enable write operations according to the OctaFlash to be used. (Note)	6.2.8
OctaFlash Status/Configuration Register Write	Write the status/configuration registers in the OctaFlash according to the OctaFlash to be used.	6.2.9
OctaFlash Configuration Register 2 Write	Write the configuration register 2 in the OctaFlash according to the OctaFlash to be used.	6.2.10
OctaFlash ID Information Read	Read ID information in the OctaFlash according to the OctaFlash to be used.	6.2.11
OctaFlash Data Read	Read data in the OctaFlash according to the OctaFlash to be used.	6.2.12
OctaFlash Sector Erasure	Erase a sector in the OctaFlash according to the OctaFlash to be used.	6.2.13
OctaFlash Data Write	Program the OctaFlash according to the OctaFlash to be used.	6.2.14

Note: In some cases, it is necessary to enable write operations to the OctaFlash in order to make settings to the registers in the OctaFlash.

The settings required for OctaFlash boot in settings shown in Table 6.6 are executed by the SPIBSC and OctaFlash initial setting process (R_SPIBSC_Setup function). It can be accessed to OctaFlash registers and memory by changing the processing of the user-defined function in the sample code according to the OctaFlash to be used. Figure 6.2 shows the Hierarchical module diagram of the SPIBSC and OctaFlash settings. Subsections 6.2.1 to 6.2.14 show the outline of the processing executed by the sample program.

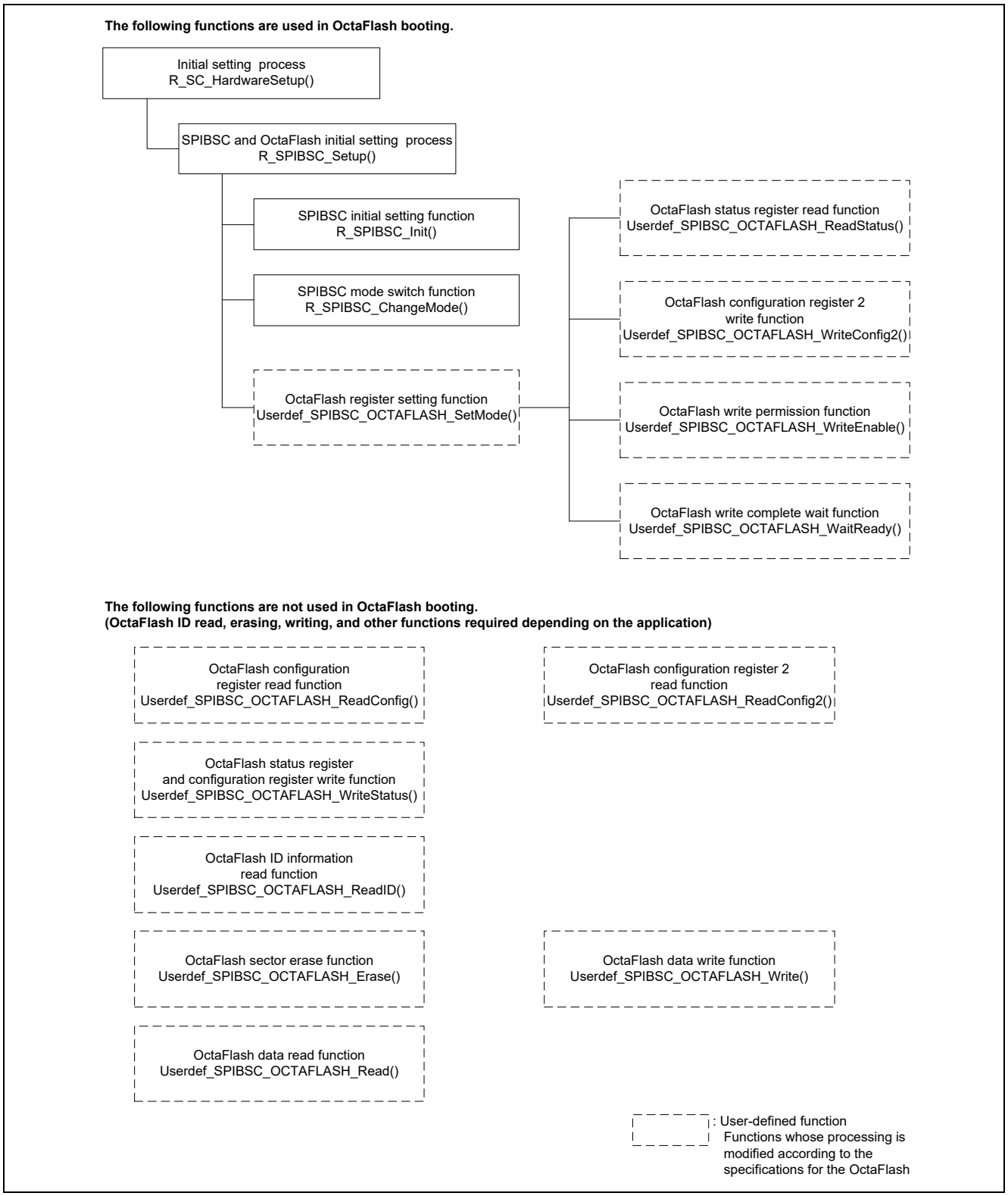


Figure 6.2 Hierarchical module diagram of the SPIBSC and OctaFlash settings

6.2.1 Signal Output when a Read Command is Issued in External Address Space Read Mode

In external address space read mode, a read access to the SPI multi-I/O bus space is initiated by sending a signal, which is converted for SPI communication, to the OctaFlash when issuing the read command. In the case of changing the OctaFlash to be used, the output signal for issuing a read command needs to be changed according to the specifications for the OctaFlash read command.

The SPIBSC allows the read command signal output to the OctaFlash to be changed by setting up the SPIBSC register in the external address space read mode.

In the sample code, the SPIBSC register settings can be changed and the output signal when a read command is issued can be changed by changing the contents of the SPIBSC external address space read mode's read command settings tables (Table 6.7). The SPIBSC register setting value specified in the read command settings tables are made by executing the SPIBSC operating mode setting function (R_SPIBSC_ChangeMode). The OctaFlash register settings related to the read command settings (number of dummy cycles, bit width, etc.) are made by executing the OctaFlash register setting function (Userdef_SPIBSC_OCTAFLASH_SetMode). Also change the implementation of the register setting process to the OctaFlash with the Userdef_SPIBSC_OCTAFLASH_SetMode function according to the specifications of the OctaFlash to be used.

Figure 6.3 shows the Correspondence between SPIBSC register settings and waveforms output to OctaFlash in external address space read mode. Refer to these example settings when changing the settings in the external address space read mode's read command settings tables (Table 6.7) to match the read command of the OctaFlash used.

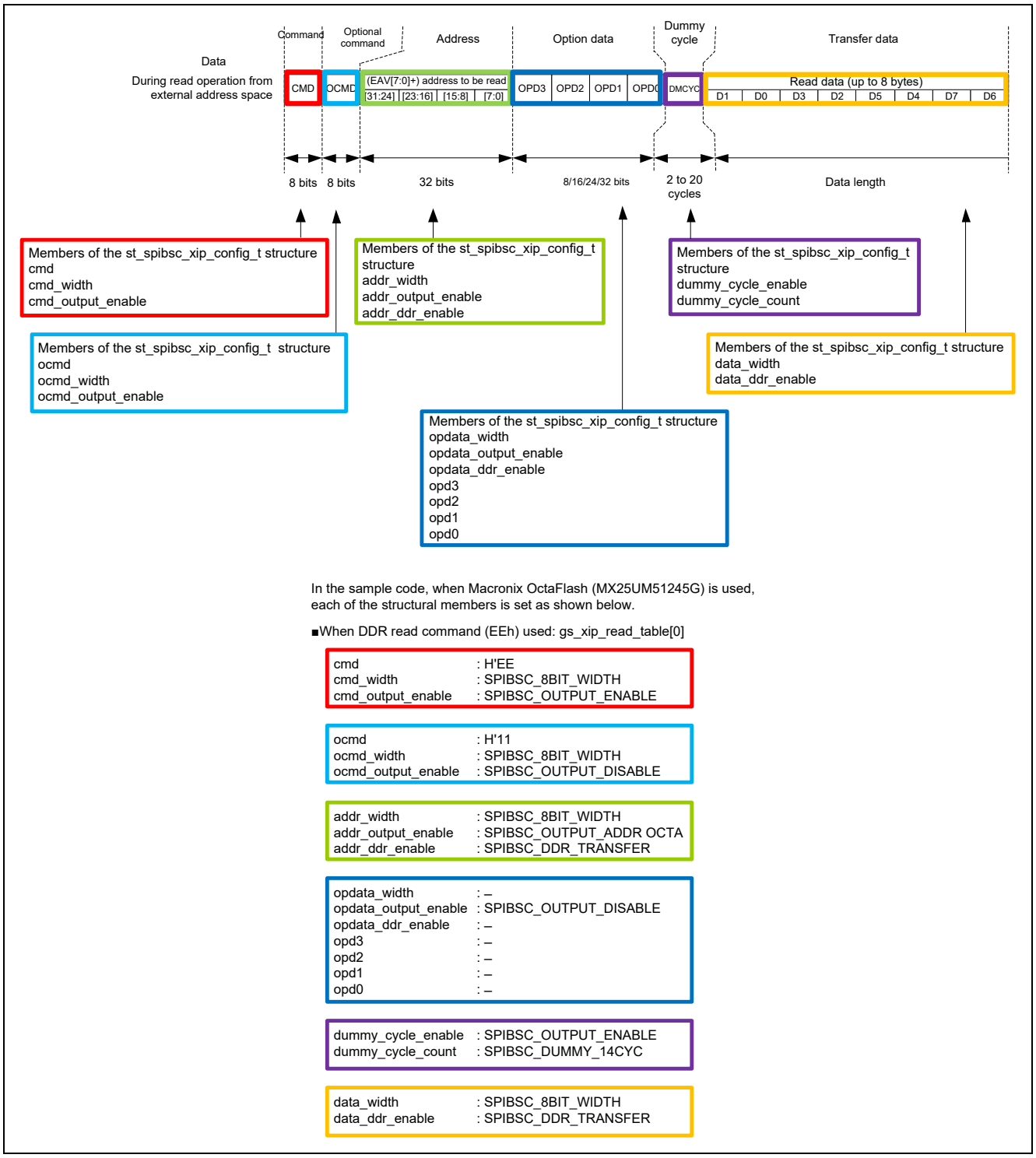


Figure 6.3 Correspondence between SPIBSC register settings and waveforms output to OctaFlash in external address space read mode

Table 6.7 Command settings table for external address space read mode gs_xip_read_table[0]

Member	Description	Setting value
uint8_t command_name[20]	Command identification character string	"OCTA_OPI_8DTRD"
uint8_t cmd	Command code	0xEE
uint8_t cmd_width	Command bit width	SPIBSC_8BIT_WIDTH
uint8_t cmd_output_enable	Command output enable/disable	SPIBSC_OUTPUT_ENABLE
uint8_t ocmd	Optional command code	0x11
uint8_t ocmd_width	Optional command bit width	SPIBSC_8BIT_WIDTH
uint8_t ocmd_output_enable	Optional command output enable/disable	SPIBSC_OUTPUT_DISABLE
uint8_t addr_width	Address bit width	SPIBSC_8BIT_WIDTH
uint8_t addr_output_enable	Address output setting	SPIBSC_OUTPUT_ADDR_OCTA
uint8_t addr_ddr_enable	Address transfer method	SPIBSC_DDR_TRANSFER
uint8_t opdata_width	Option data bit width	SPIBSC_8BIT_WIDTH
uint8_t opdata_output_enable	Option data output setting	SPIBSC_OUTPUT_DISABLE
uint8_t opdata_ddr_enable	Option data transfer method	SPIBSC_DDR_TRANSFER
uint8_t opd3	Option Data3 (8bit) setting (outputs for the first)	0x00
uint8_t opd2	Option Data2 (8bit) setting (outputs for the second)	0x00
uint8_t opd1	Option Data1 (8bit) setting (outputs for the third)	0x00
uint8_t opd0	Option Data0 (8bit) setting (outputs for the fourth)	0x00
uint8_t dummy_cycle_enable	Dummy cycle output enable/disable	SPIBSC_OUTPUT_ENABLE
uint8_t dummy_cycle_count	Number of dummy cycles	SPIBSC_DUMMY_14CYC
uint8_t data_width	Transfer data bit width	SPIBSC_8BIT_WIDTH
uint8_t data_ddr_enable	Transfer data transfer method	SPIBSC_DDR_TRANSFER

Note: CMNCR.MOIIOn (n = 0 to 3) is set to B'01 (output value is 1) and CMNCR.IOnFV (n = 0, 2, 3) is set to B'11 (output value is Hi-Z).

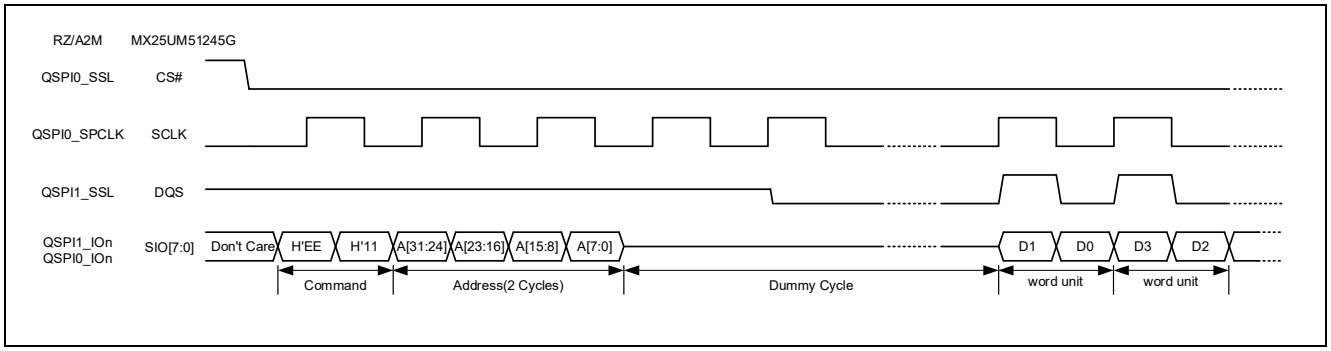


Figure 6.4 Waveform format of EEH read command (reference)

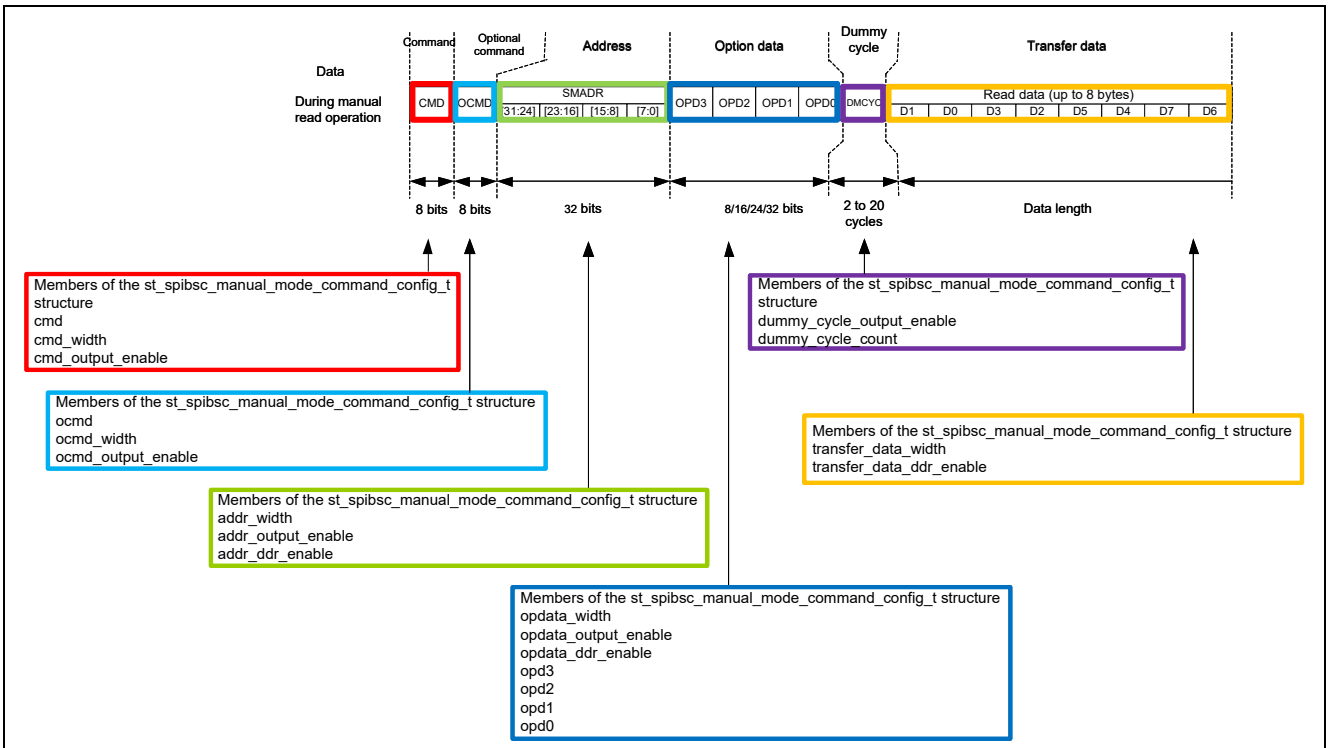
6.2.2 Signal Output When a Command is Issued in Manual Mode

In manual mode, an access to the SPI multi-I/O bus space is initiated by writing 1 to the SPI data transfer enable bit (SPIE) in the manual mode control register (SMCR). In the case of changing the OctaFlash to be used, the output signal for issuing a command needs to be changed according to the specifications of the OctaFlash command. For OctaFlash register access or data write access, commands need to be issued to OctaFlash in manual mode.

The SPIBSC allows changing the command signal output to the OctaFlash in manual mode by setting the SPIBSC register.

In the sample code, the SPIBSC register settings can be changed and the output signal for issuing a command can be changed by changing the contents of the command settings tables in SPIBSC manual mode (Table 6.8 to Table 6.25). The SPIBSC register setting value specified in the command settings tables are made each time the function for issuing the SPI command to OctaFlash (R_SPIBSC_SPICMDIssue) is executed. The OctaFlash register settings related to the command settings (number of dummy cycles, bit width, etc.) are made by the OctaFlash register setting function (Userdef_SPIBSC_OCTAFLASH_SetMode). Also change the implementation of the register setting process to the OctaFlash with the Userdef_SPIBSC_OCTAFLASH_SetMode function according to the specifications of the OctaFlash to be used.

Figure 6.5 shows the Correspondence between SPIBSC register settings and waveforms output to OctaFlash in manual mode. Refer to the sample code and change the example settings given in the command settings tables in manual mode according to the command of the OctaFlash used.



In the sample code, when Macronix OctaFlash (MX25UM51245G) is used, each of the structural members is set as shown below.

■When DDR configuration register 2 read command (71h) used :gs_command_table[9]

cmd	: H'71
cmd_width	: SPIBSC_8BIT_WIDTH
cmd_output_enable	: SPIBSC_OUTPUT_ENABLE
ocmd	: H'8E
ocmd_width	: SPIBSC_8BIT_WIDTH
ocmd_output_enable	: SPIBSC_OUTPUT_DISABLE
addr_width	: SPIBSC_8BIT_WIDTH
addr_output_enable	: SPIBSC_OUTPUT_ADDR OCTA
addr_ddr_enable	: SPIBSC_DDR_TRANSFER
opdata_width	: –
opdata_output_enable	: SPIBSC_OUTPUT_DISABLE
opdata_ddr_enable	: –
opd3	: –
opd2	: –
opd1	: –
opd0	: –
dummy_cycle_output_enable	: SPIBSC_OUTPUT_ENABLE
dummy_cycle_count	: SPIBSC_DUMMY_14CYC
data_width	: SPIBSC_8BIT_WIDTH
data_ddr_enable	: SPIBSC_DDR_TRANSFER

■When DDR configuration register 2 write command (72h) used : gs_command_table[13]

cmd	: H'72
cmd_width	: SPIBSC_8BIT_WIDTH
cmd_output_enable	: SPIBSC_OUTPUT_ENABLE
ocmd	: H'8D
ocmd_width	: SPIBSC_8BIT_WIDTH
ocmd_output_enable	: SPIBSC_OUTPUT_DISABLE
addr_width	: SPIBSC_8BIT_WIDTH
addr_output_enable	: SPIBSC_OUTPUT_ADDR OCTA
addr_ddr_enable	: SPIBSC_DDR_TRANSFER
opdata_width	: –
opdata_output_enable	: SPIBSC_OUTPUT_DISABLE
opdata_ddr_enable	: –
opd3	: –
opd2	: –
opd1	: –
opd0	: –
dummy_cycle_output_enable	: SPIBSC_OUTPUT_DISABLE
dummy_cycle_count	: 0
data_width	: SPIBSC_8BIT_WIDTH
data_ddr_enable	: SPIBSC_DDR_TRANSFER

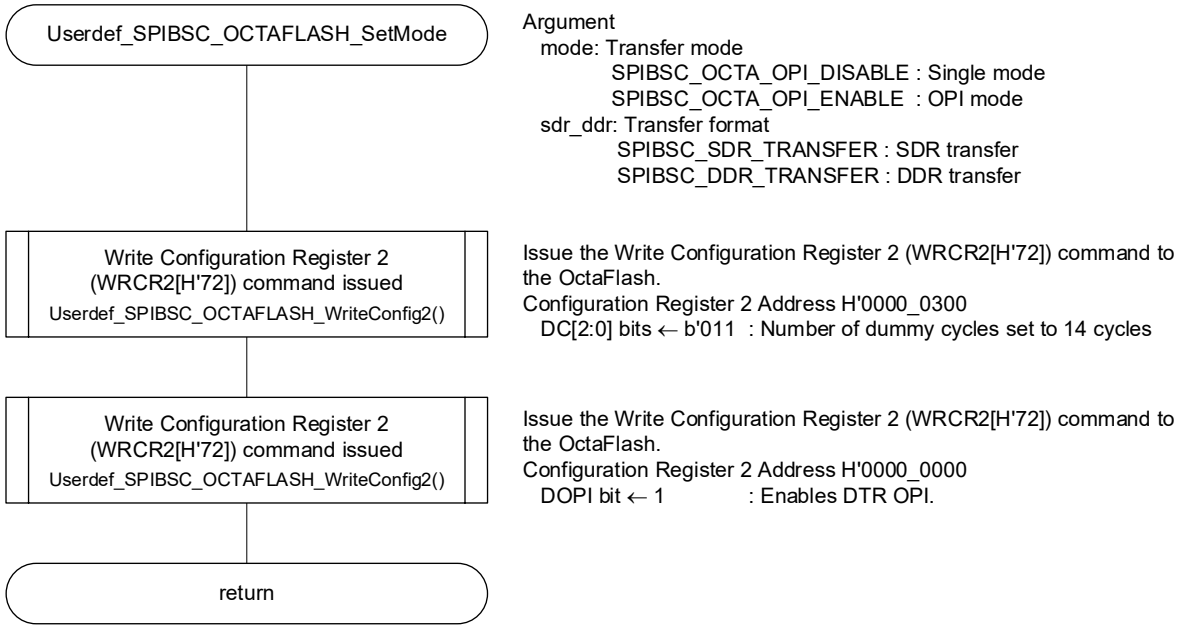
Figure 6.5 Correspondence between SPIBSC register settings and waveforms output to OctaFlash in manual mode

6.2.3 Setting up the OctaFlash Registers

In the sample code, the user-defined function Userdef_SPIBSC_OCTAFLASH_SetMode executes the processing for the OctaFlash MX25UM51245G register settings (DOPI bit at address H'0000_0000 and DC[2:0] bits at address H'0000_0300 of the configuration register 2) according to the specifications of the read command to be used.

In the sample code, because the Octa IO DT Read command (H'EE) is used as the read command, the DOPI bit of the configuration register 2 (address H'0000_0000) is set to 1 so the DDR transfer mode with the bit width of 8 bits is enabled. Also, the DC[2:0] bits of the configuration register 2 are set so that the number of inserted dummy cycles is the minimum needed for the operating frequency used (refer to Table 6.5 List of numbers of dummy cycles necessary for the maximum operating frequency of the for details). Change the implementation of the Userdef_SPIBSC_OCTAFLASH_SetMode function so that the OctaFlash's control register setting conforms to the read command specifications of the OctaFlash to be used.

Figure 6.6 shows the Userdef_SPIBSC_OCTAFLASH_SetMode function processing flow of the sample code.



Note: The OctaFlash access is changed from 1-bit width to 8-bit width, and the Configuration Register 2 is set to achieve the minimum number of dummy cycles for the read command. These register settings require the WRCR2 command to be issued to the OctaFlash after switching the SPIBSC from external address space read mode to manual mode.

Figure 6.6 Userdef_SPIBSC_OCTAFLASH_SetMode function processing flow

6.2.4 OctaFlash Write Completion Wait

The OctaFlash transits to a busy state when the OctaFlash Status Register or memory are written to. It is then necessary to wait until the written data is reflected before accessing the OctaFlash.

In the sample code, this wait processing is executed with the Userdef_SPIBSC_OCTAFLASH_WaitReady function.

Implement the Userdef_SPIBSC_OCTAFLASH_WaitReady function according to the specifications of the OctaFlash to be used so that it can wait until completion of OctaFlash writing.

In the sample code, The Status Register WIP bit is read, and wait processing is performed until writing is complete.

Figure 6.7 shows the Userdef_SPIBSC_OCTAFLASH_WaitReady function processing flow of the sample code.

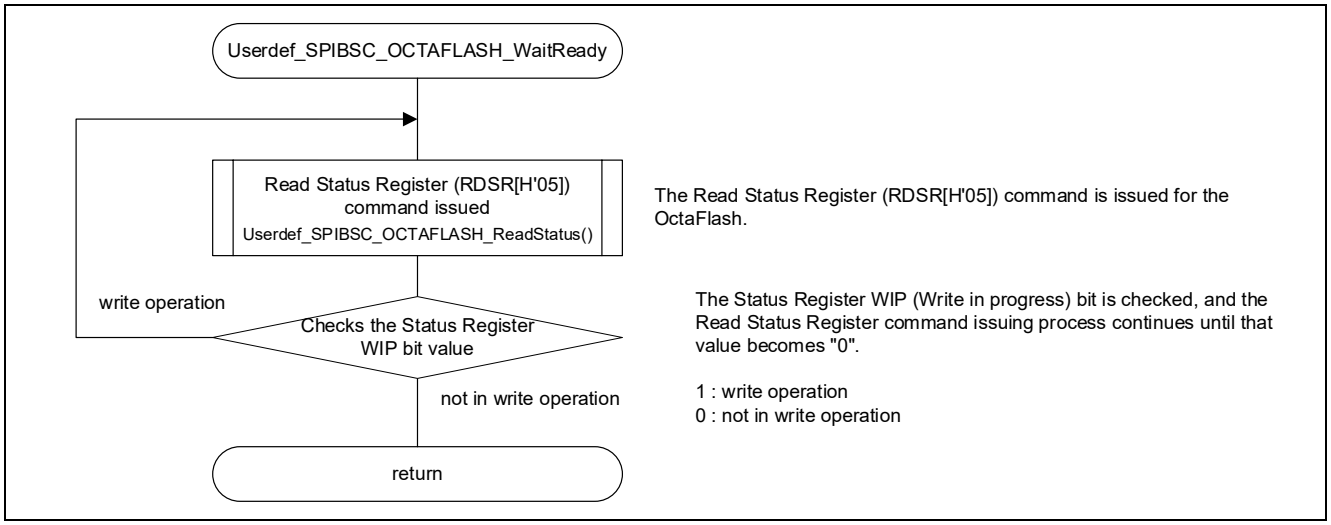


Figure 6.7 Userdef_SPIBSC_OCTAFLASH_WaitReady function processing flow

6.2.5 OctaFlash Status Register Read

In the sample code, OctaFlash Status Register reading is executed with the Userdef_SPIBSC_OCTAFLASH_ReadStatus function.

Implement the Userdef_SPIBSC_OCTAFLASH_ReadStatus function according to the specifications of the OctaFlash to be used so that it can read the OctaFlash status register.

Figure 6.8 shows the Userdef_SPIBSC_OCTAFLASH_ReadStatus function processing flow of the sample code.

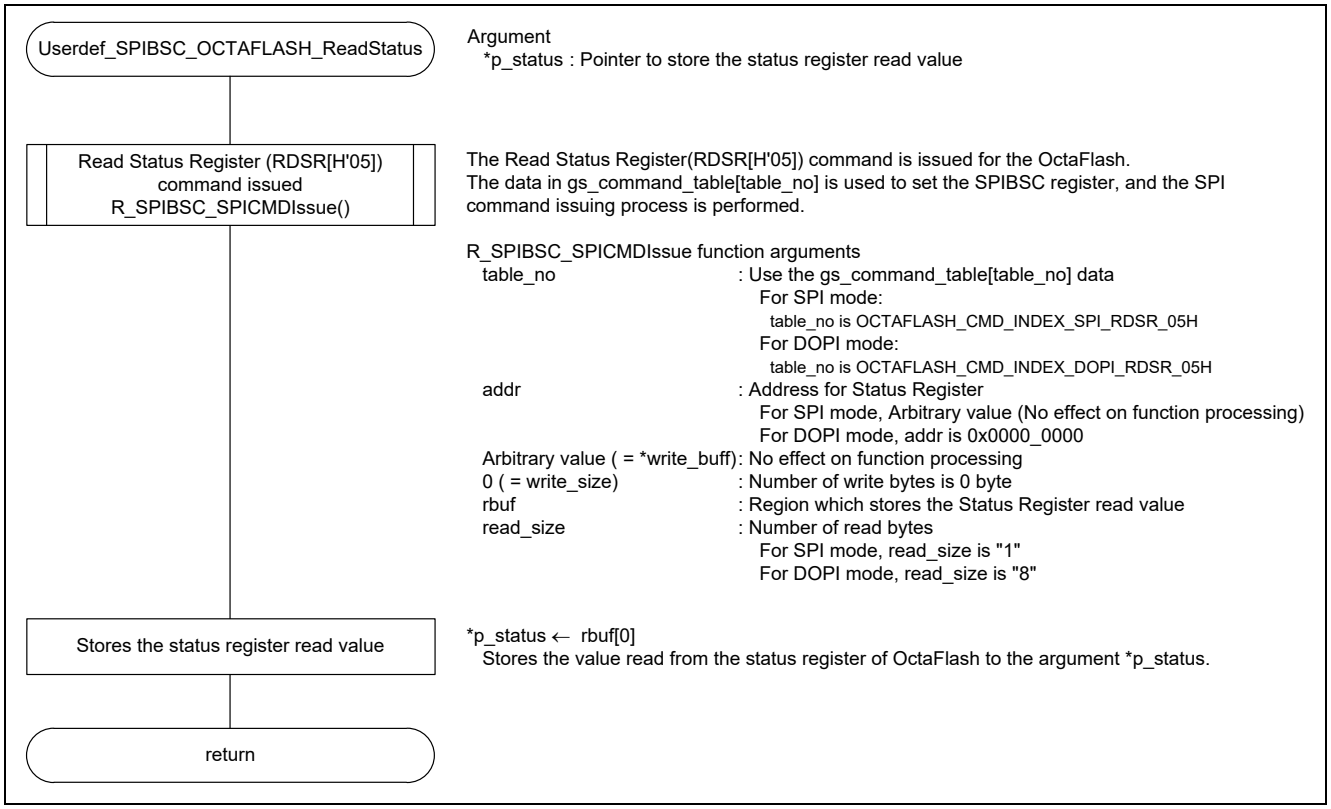


Figure 6.8 Userdef_SPIBSC_OCTAFLASH_ReadStatus function processing flow

Table 6.8 Command settings table for manual mode gs_command_table[0]: RDSR command in SPI mode

Member	Description	Setting value
uint8_t command_name[20]	Command identification character string	"SPI_RDSR"
uint8_t cmd	Command code	0x05
uint8_t cmd_width	Command bit width	SPIBSC_1BIT_WIDTH
uint8_t cmd_output_enable	Command output enable/disable	SPIBSC_OUTPUT_ENABLE
uint8_t ocmd	Optional command code	0x00
uint8_t ocmd_width	Optional command bit width	SPIBSC_1BIT_WIDTH
uint8_t ocmd_enable	Optional command output enable/disable	SPIBSC_OUTPUT_DISABLE
uint8_t addr_width	Address bit width	SPIBSC_1BIT_WIDTH
uint8_t addr_output_enable	Address output setting	SPIBSC_OUTPUT_DISABLE
uint8_t addr_sdr_ddr	Address transfer method	SPIBSC_SDR_TRANSFER
uint8_t opdata_width	Option data bit width	SPIBSC_1BIT_WIDTH
uint8_t opdata_output_enable	Option data output setting	SPIBSC_OUTPUT_DISABLE
uint8_t opdata_ddr_enable	Option data transfer method	SPIBSC_SDR_TRANSFER
uint8_t opd3	Option Data3 (8bit) setting (outputs for the first)	0x00
uint8_t opd2	Option Data2 (8bit) setting (outputs for the second)	0x00
uint8_t opd1	Option Data1 (8bit) setting (outputs for the third)	0x00
uint8_t opd0	Option Data0 (8bit) setting (outputs for the fourth)	0x00
uint8_t dummy_cycle_output_enable	Dummy cycle output enable/disable	SPIBSC_OUTPUT_DISABLE
uint8_t dummy_cycle_count	Number of dummy cycles	0x00
uint8_t transfer_data_width	Transfer data bit width	SPIBSC_1BIT_WIDTH
uint8_t transfer_data_sdr_ddr	Transfer data transfer method	SPIBSC_SDR_TRANSFER

Note: CMNCR.MOIIOn (n = 0 to 3) is set to B'01 (output value is 1) and CMNCR.IOnFV (n = 0, 2, 3) is set to B'11 (output value is Hi-Z).

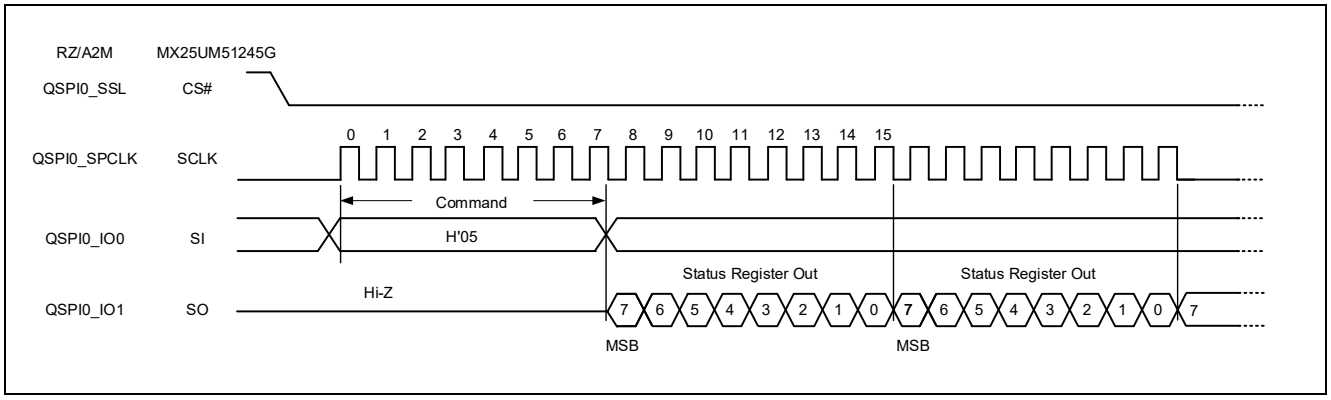


Figure 6.9 Waveform format of RDSR command in SPI mode (reference)

Table 6.9 Command settings table for manual mode gs_command_table[7]: RDSR command in DOPI mode

Member	Description	Setting value
uint8_t command_name[20]	Command identification character string	"DOPI_RDSR"
uint8_t cmd	Command code	0x05
uint8_t cmd_width	Command bit width	SPIBSC_8BIT_WIDTH
uint8_t cmd_output_enable	Command output enable/disable	SPIBSC_OUTPUT_ENABLE
uint8_t ocmd	Optional command code	0xFA
uint8_t ocmd_width	Optional command bit width	SPIBSC_8BIT_WIDTH
uint8_t ocmd_enable	Optional command output enable/disable	SPIBSC_OUTPUT_DISABLE
uint8_t addr_width	Address bit width	SPIBSC_8BIT_WIDTH
uint8_t addr_output_enable	Address output setting	SPIBSC_OUTPUT_ADDR_OCTA
uint8_t addr_sdr_ddr	Address transfer method	SPIBSC_DDR_TRANSFER
uint8_t opdata_width	Option data bit width	SPIBSC_8BIT_WIDTH
uint8_t opdata_output_enable	Option data output setting	SPIBSC_OUTPUT_DISABLE
uint8_t opdata_ddr_enable	Option data transfer method	SPIBSC_SDR_TRANSFER
uint8_t opd3	Option Data3 (8bit) setting (outputs for the first)	0x00
uint8_t opd2	Option Data2 (8bit) setting (outputs for the second)	0x00
uint8_t opd1	Option Data1 (8bit) setting (outputs for the third)	0x00
uint8_t opd0	Option Data0 (8bit) setting (outputs for the fourth)	0x00
uint8_t dummy_cycle_output_enable	Dummy cycle output enable/disable	SPIBSC_OUTPUT_ENABLE
uint8_t dummy_cycle_count	Number of dummy cycles	SPIBSC_DUMMY_14CYC
uint8_t transfer_data_width	Transfer data bit width	SPIBSC_8BIT_WIDTH
uint8_t transfer_data_sdr_ddr	Transfer data transfer method	SPIBSC_DDR_TRANSFER

Note: CMNCR.MOIIOn (n = 0 to 3) is set to B'01 (output value is 1) and CMNCR.IOnFV (n = 0, 2, 3) is set to B'11 (output value is Hi-Z).

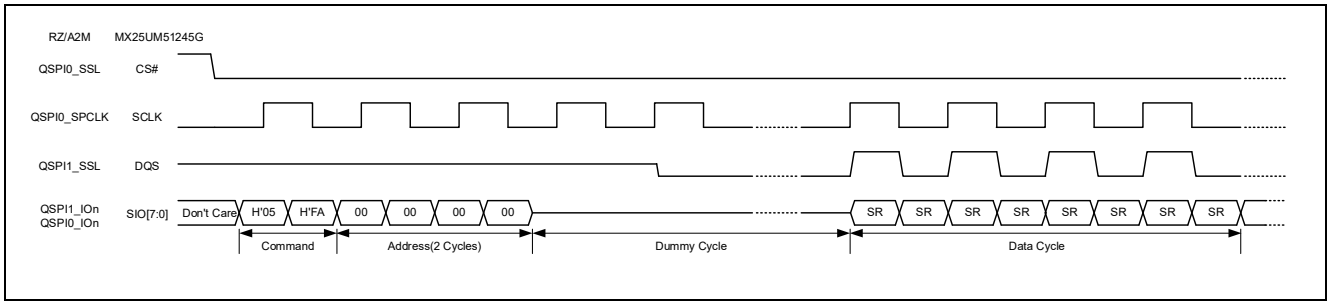


Figure 6.10 Waveform format of RDSR command in DOPI mode (reference)

6.2.6 OctaFlash Configuration Register Read

In the sample code, OctaFlash configuration register reading is executed with the Userdef_SPIBSC_OCTAFLASH_ReadConfig function.

Implement the Userdef_SPIBSC_OCTAFLASH_ReadConfig function according to the specifications of the OctaFlash to be used so that it can read the OctaFlash configuration register.

Figure 6.11 shows the Userdef_SPIBSC_OCTAFLASH_ReadConfig function processing flow of the sample code.

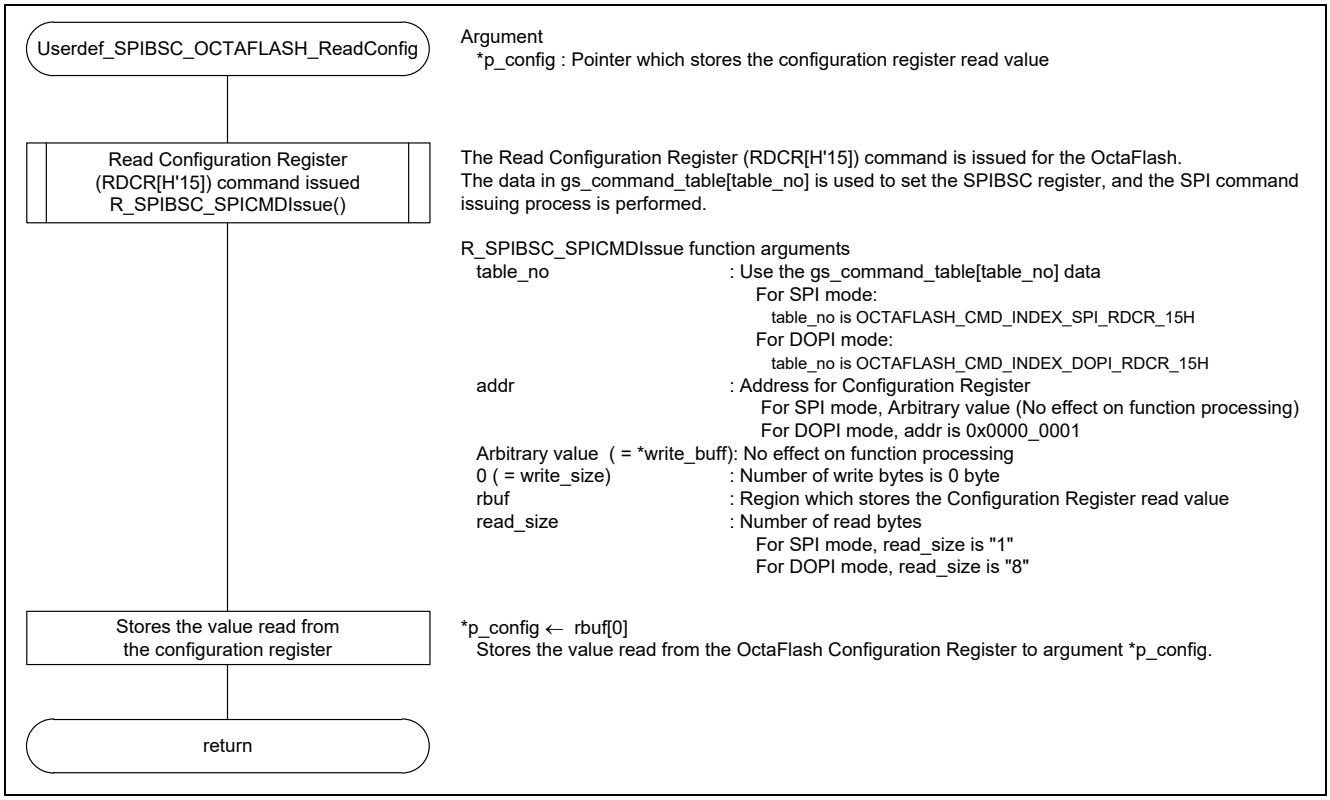


Figure 6.11 Userdef_SPIBSC_OCTAFLASH_ReadConfig function processing flow

Table 6.10 Command settings table for manual mode gs_command_table[1]: RDCR Command in SPI mode

Member	Description	Setting value
uint8_t command_name[20]	Command identification character string	"SPI_RDCR"
uint8_t cmd	Command code	0x15
uint8_t cmd_width	Command bit width	SPIBSC_1BIT_WIDTH
uint8_t cmd_output_enable	Command output enable/disable	SPIBSC_OUTPUT_ENABLE
uint8_t ocmd	Optional command code	0x00
uint8_t ocmd_width	Optional command bit width	SPIBSC_1BIT_WIDTH
uint8_t ocmd_enable	Optional command output enable/disable	SPIBSC_OUTPUT_DISABLE
uint8_t addr_width	Address bit width	SPIBSC_1BIT_WIDTH
uint8_t addr_output_enable	Address output setting	SPIBSC_OUTPUT_DISABLE
uint8_t addr_sdr_ddr	Address transfer method	SPIBSC_SDR_TRANSFER
uint8_t opdata_width	Option data bit width	SPIBSC_1BIT_WIDTH
uint8_t opdata_output_enable	Option data output setting	SPIBSC_OUTPUT_DISABLE
uint8_t opdata_ddr_enable	Option data transfer method	SPIBSC_SDR_TRANSFER
uint8_t opd3	Option Data3 (8bit) setting (outputs for the first)	0x00
uint8_t opd2	Option Data2 (8bit) setting (outputs for the second)	0x00
uint8_t opd1	Option Data1 (8bit) setting (outputs for the third)	0x00
uint8_t opd0	Option Data0 (8bit) setting (outputs for the fourth)	0x00
uint8_t dummy_cycle_output_enable	Dummy cycle output enable/disable	SPIBSC_OUTPUT_DISABLE
uint8_t dummy_cycle_count	Number of dummy cycles	0x00
uint8_t transfer_data_width	Transfer data bit width	SPIBSC_1BIT_WIDTH
uint8_t transfer_data_sdr_ddr	Transfer data transfer method	SPIBSC_SDR_TRANSFER

Note: CMNCR.MOIIOn (n = 0 to 3) is set to B'01 (output value is 1) and CMNCR.IOnFV (n = 0, 2, 3) is set to B'11 (output value is Hi-Z).

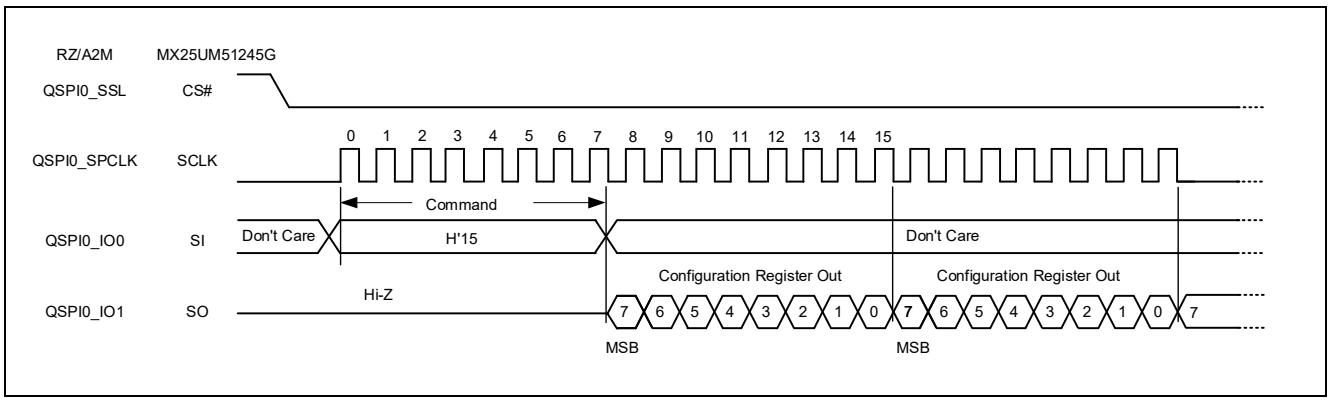


Figure 6.12 Waveform format of RDCR command in SPI mode (reference)

Table 6.11 Command settings table for manual mode gs_command_table[8]: RDCR Command in DOPI mode

Member	Description	Setting value
uint8_t command_name[20]	Command identification character string	"DOPI_RDCR"
uint8_t cmd	Command code	0x15
uint8_t cmd_width	Command bit width	SPIBSC_8BIT_WIDTH
uint8_t cmd_output_enable	Command output enable/disable	SPIBSC_OUTPUT_ENABLE
uint8_t ocmd	Optional command code	0xEA
uint8_t ocmd_width	Optional command bit width	SPIBSC_8BIT_WIDTH
uint8_t ocmd_enable	Optional command output enable/disable	SPIBSC_OUTPUT_DISABLE
uint8_t addr_width	Address bit width	SPIBSC_8BIT_WIDTH
uint8_t addr_output_enable	Address output setting	SPIBSC_OUTPUT_ADDR_OCTA
uint8_t addr_sdr_ddr	Address transfer method	SPIBSC_DDR_TRANSFER
uint8_t opdata_width	Option data bit width	SPIBSC_8BIT_WIDTH
uint8_t opdata_output_enable	Option data output setting	SPIBSC_OUTPUT_DISABLE
uint8_t opdata_ddr_enable	Option data transfer method	SPIBSC_DDR_TRANSFER
uint8_t opd3	Option Data3 (8bit) setting (outputs for the first)	0x00
uint8_t opd2	Option Data2 (8bit) setting (outputs for the second)	0x00
uint8_t opd1	Option Data1 (8bit) setting (outputs for the third)	0x00
uint8_t opd0	Option Data0 (8bit) setting (outputs for the fourth)	0x00
uint8_t dummy_cycle_output_enable	Dummy cycle output enable/disable	SPIBSC_OUTPUT_ENABLE
uint8_t dummy_cycle_count	Number of dummy cycles	SPIBSC_DUMMY_14CYC
uint8_t transfer_data_width	Transfer data bit width	SPIBSC_8BIT_WIDTH
uint8_t transfer_data_sdr_ddr	Transfer data transfer method	SPIBSC_DDR_TRANSFER

Note: CMNCR.MOIIOn (n = 0 to 3) is set to B'01 (output value is 1) and CMNCR.IOnFV (n = 0, 2, 3) is set to B'11 (output value is Hi-Z).

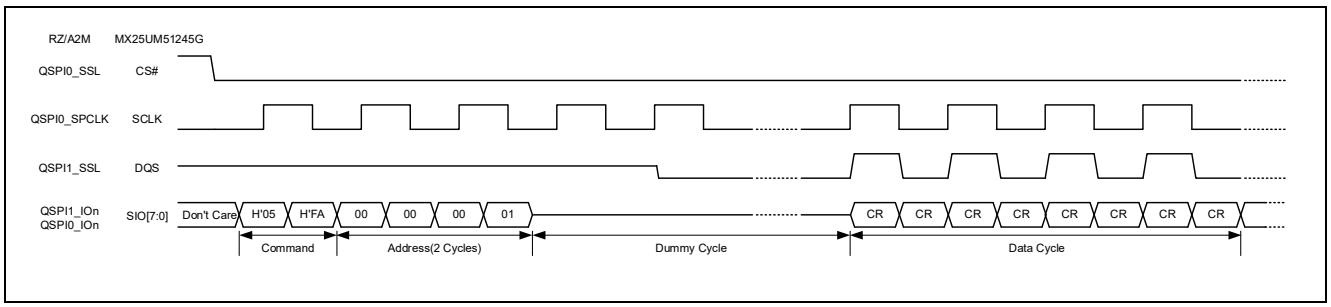


Figure 6.13 Waveform format of RDCR command in DOPI mode (reference)

6.2.7 OctaFlash Configuration Register 2 Read

Implement the Userdef_SPIBSC_OCTAFLASH_ReadConfig2 function according to the specifications of the OctaFlash to be used so that it can read the OctaFlash configuration register.

Figure 6.14 shows the Userdef_SPIBSC_OCTAFLASH_ReadConfig2 function processing flow of the sample code.

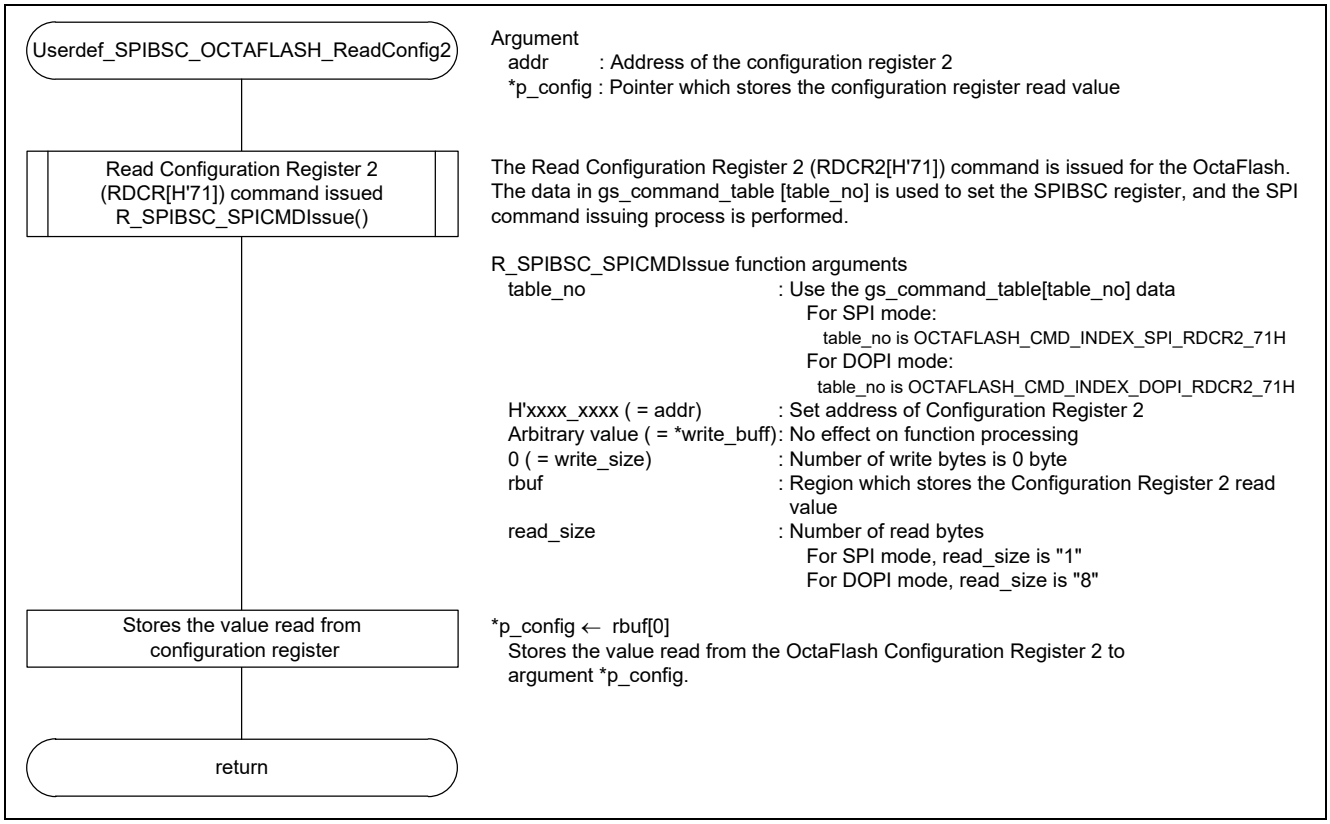


Figure 6.14 Userdef_SPIBSC_OCTAFLASH_ReadConfig2 function processing flow

Table 6.12 Command settings table for manual mode gs_command_table[2]: RDCR2 Command in SPI mode

Member	Description	Setting value
uint8_t command_name[20]	Command identification character string	"SPI_RDCR2"
uint8_t cmd	Command code	0x71
uint8_t cmd_width	Command bit width	SPIBSC_1BIT_WIDTH
uint8_t cmd_output_enable	Command output enable/disable	SPIBSC_OUTPUT_ENABLE
uint8_t ocmd	Optional command code	0x00
uint8_t ocmd_width	Optional command bit width	SPIBSC_1BIT_WIDTH
uint8_t ocmd_enable	Optional command output enable/disable	SPIBSC_OUTPUT_DISABLE
uint8_t addr_width	Address bit width	SPIBSC_1BIT_WIDTH
uint8_t addr_output_enable	Address output setting	SPIBSC_OUTPUT_ADDR_32
uint8_t addr_sdr_ddr	Address transfer method	SPIBSC_SDR_TRANSFER
uint8_t opdata_width	Option data bit width	SPIBSC_1BIT_WIDTH
uint8_t opdata_output_enable	Option data output setting	SPIBSC_OUTPUT_DISABLE
uint8_t opdata_ddr_enable	Option data transfer method	SPIBSC_SDR_TRANSFER
uint8_t opd3	Option Data3 (8bit) setting (outputs for the first)	0x00
uint8_t opd2	Option Data2 (8bit) setting (outputs for the second)	0x00
uint8_t opd1	Option Data1 (8bit) setting (outputs for the third)	0x00
uint8_t opd0	Option Data0 (8bit) setting (outputs for the fourth)	0x00
uint8_t dummy_cycle_output_enable	Dummy cycle output enable/disable	SPIBSC_OUTPUT_DISABLE
uint8_t dummy_cycle_count	Number of dummy cycles	0x00
uint8_t transfer_data_width	Transfer data bit width	SPIBSC_1BIT_WIDTH
uint8_t transfer_data_sdr_ddr	Transfer data transfer method	SPIBSC_SDR_TRANSFER

Note: CMNCR.MOIIOn (n = 0 to 3) is set to B'01 (output value is 1) and CMNCR.IOnFV (n = 0, 2, 3) is set to B'11 (output value is Hi-Z).

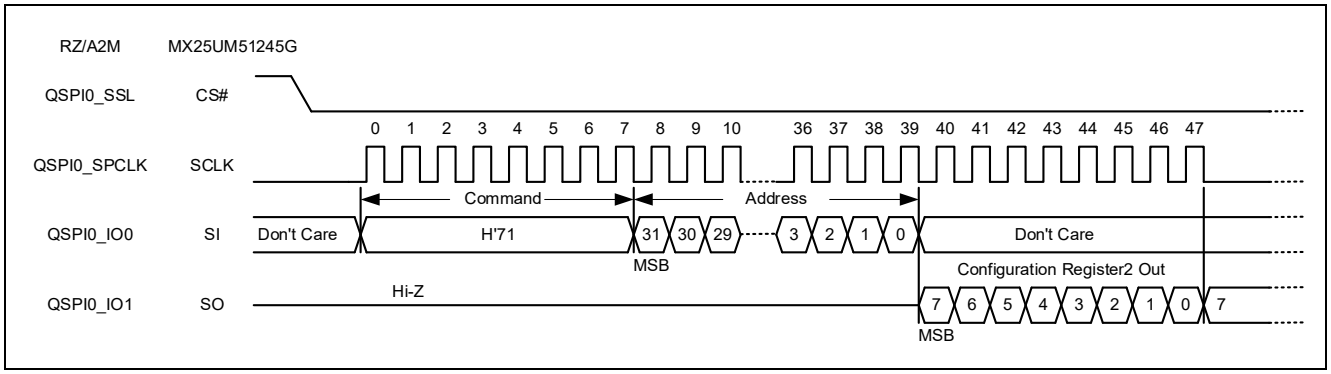


Figure 6.15 Waveform format of RDCR2 command in SPI mode (reference)

Table 6.13 Command settings table for manual mode gs_command_table[9]: RDCR2 Command in DOPI mode

Member	Description	Setting value
uint8_t command_name[20]	Command identification character string	"DOPI_RDCR2"
uint8_t cmd	Command code	0x71
uint8_t cmd_width	Command bit width	SPIBSC_8BIT_WIDTH
uint8_t cmd_output_enable	Command output enable/disable	SPIBSC_OUTPUT_ENABLE
uint8_t ocmd	Optional command code	0x8E
uint8_t ocmd_width	Optional command bit width	SPIBSC_8BIT_WIDTH
uint8_t ocmd_enable	Optional command output enable/disable	SPIBSC_OUTPUT_DISABLE
uint8_t addr_width	Address bit width	SPIBSC_8BIT_WIDTH
uint8_t addr_output_enable	Address output setting	SPIBSC_OUTPUT_ADDR_OCTA
uint8_t addr_sdr_ddr	Address transfer method	SPIBSC_DDR_TRANSFER
uint8_t opdata_width	Option data bit width	SPIBSC_8BIT_WIDTH
uint8_t opdata_output_enable	Option data output setting	SPIBSC_OUTPUT_DISABLE
uint8_t opdata_ddr_enable	Option data transfer method	SPIBSC_DDR_TRANSFER
uint8_t opd3	Option Data3 (8bit) setting (outputs for the first)	0x00
uint8_t opd2	Option Data2 (8bit) setting (outputs for the second)	0x00
uint8_t opd1	Option Data1 (8bit) setting (outputs for the third)	0x00
uint8_t opd0	Option Data0 (8bit) setting (outputs for the fourth)	0x00
uint8_t dummy_cycle_output_enable	Dummy cycle output enable/disable	SPIBSC_OUTPUT_ENABLE
uint8_t dummy_cycle_count	Number of dummy cycles	SPIBSC_DUMMY_14CYC
uint8_t transfer_data_width	Transfer data bit width	SPIBSC_8BIT_WIDTH
uint8_t transfer_data_sdr_ddr	Transfer data transfer method	SPIBSC_DDR_TRANSFER

Note: CMNCR.MOIIOn (n = 0 to 3) is set to B'01 (output value is 1) and CMNCR.IOnFV (n = 0, 2, 3) is set to B'11 (output value is Hi-Z).

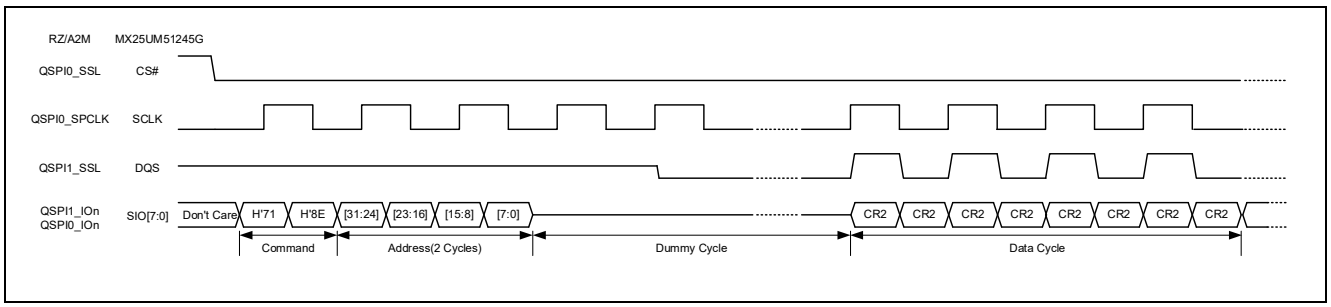


Figure 6.16 Waveform format of RDCR2 command in DOPI mode (reference)

6.2.8 OctaFlash Write Enable

It is necessary to enable the OctaFlash for writes before writing data to the registers (Status Register, Configuration Register, and Configuration Register 2) of the OctaFlash. In the sample code, this processing is executed with the Userdef_SPIBSC_OCTAFLASH_WriteEnable function.

Implement the Userdef_SPIBSC_OCTAFLASH_WriteEnable function according to the specifications for the OctaFlash to be used so that it can be enabled for writes. In the sample code, a Write Enable command (WREN [H'06]) is issued, thereby enabling writes (setting the WEL bit of the Status Register to 1).

Figure 6.17 shows the Userdef_SPIBSC_OCTAFLASH_WriteEnable function processing flow of the sample code.

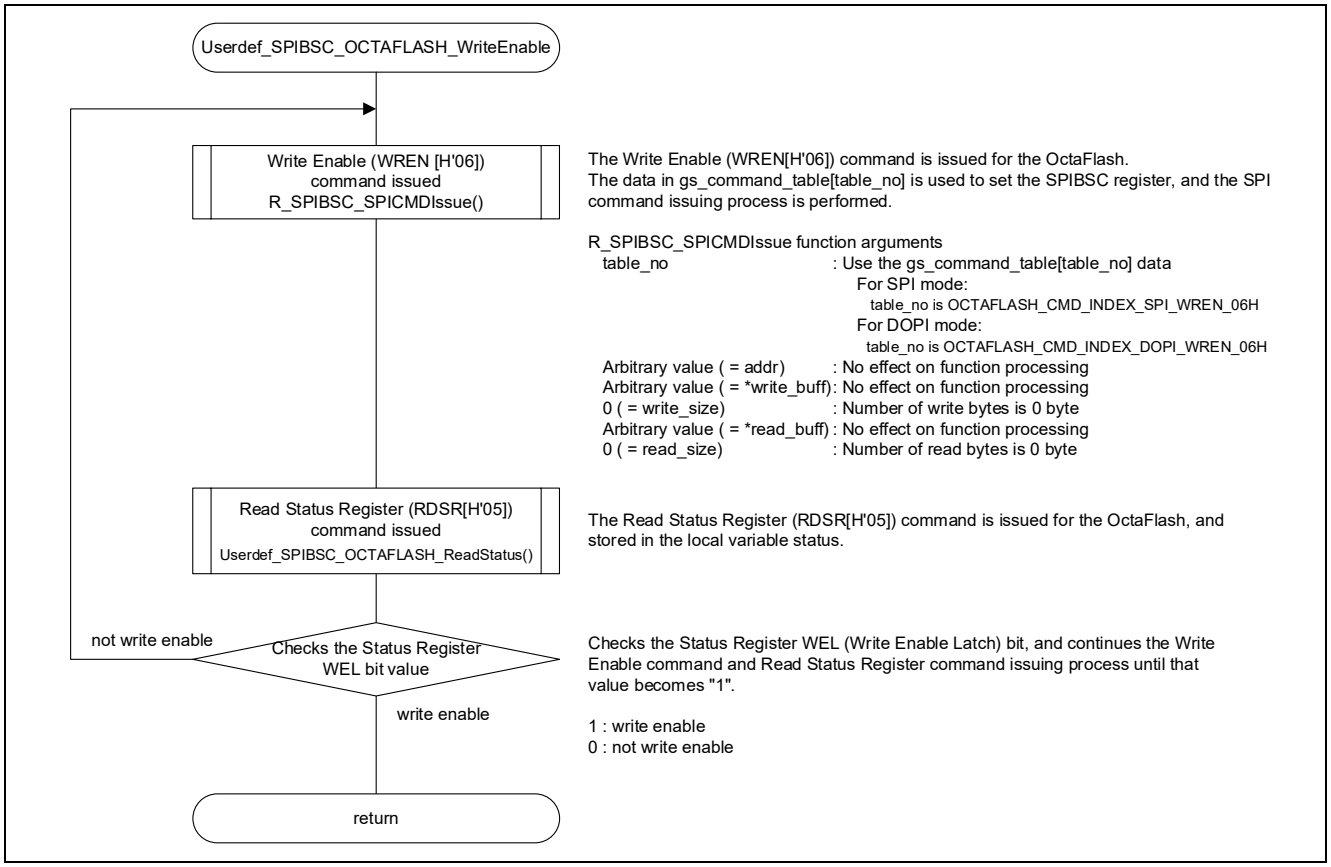


Figure 6.17 Userdef_SPIBSC_OCTAFLASH_WriteEnable function processing flow

Table 6.14 Command settings table for manual mode gs_command_table[3]: WREN command in SPI mode

Member	Description	Setting value
uint8_t command_name[20]	Command identification character string	"SPI_WREN"
uint8_t cmd	Command code	0x06
uint8_t cmd_width	Command bit width	SPIBSC_1BIT_WIDTH
uint8_t cmd_output_enable	Command output enable/disable	SPIBSC_OUTPUT_ENABLE
uint8_t ocmd	Optional command code	0x00
uint8_t ocmd_width	Optional command bit width	SPIBSC_1BIT_WIDTH
uint8_t ocmd_enable	Optional command output enable/disable	SPIBSC_OUTPUT_DISABLE
uint8_t addr_width	Address bit width	SPIBSC_1BIT_WIDTH
uint8_t addr_output_enable	Address output setting	SPIBSC_OUTPUT_DISABLE
uint8_t addr_sdr_ddr	Address transfer method	SPIBSC_SDR_TRANSFER
uint8_t opdata_width	Option data bit width	SPIBSC_1BIT_WIDTH
uint8_t opdata_output_enable	Option data output setting	SPIBSC_OUTPUT_DISABLE
uint8_t opdata_ddr_enable	Option data transfer method	SPIBSC_SDR_TRANSFER
uint8_t opd3	Option Data3 (8bit) setting (outputs for the first)	0x00
uint8_t opd2	Option Data2 (8bit) setting (outputs for the second)	0x00
uint8_t opd1	Option Data1 (8bit) setting (outputs for the third)	0x00
uint8_t opd0	Option Data0 (8bit) setting (outputs for the fourth)	0x00
uint8_t dummy_cycle_output_enable	Dummy cycle output enable/disable	SPIBSC_OUTPUT_DISABLE
uint8_t dummy_cycle_count	Number of dummy cycles	0x00
uint8_t transfer_data_width	Transfer data bit width	SPIBSC_1BIT_WIDTH
uint8_t transfer_data_sdr_ddr	Transfer data transfer method	SPIBSC_SDR_TRANSFER

Note: CMNCR.MOIIOn (n = 0 to 3) is set to B'01 (output value is 1) and CMNCR.IOnFV (n = 0, 2, 3) is set to B'11 (output value is Hi-Z).

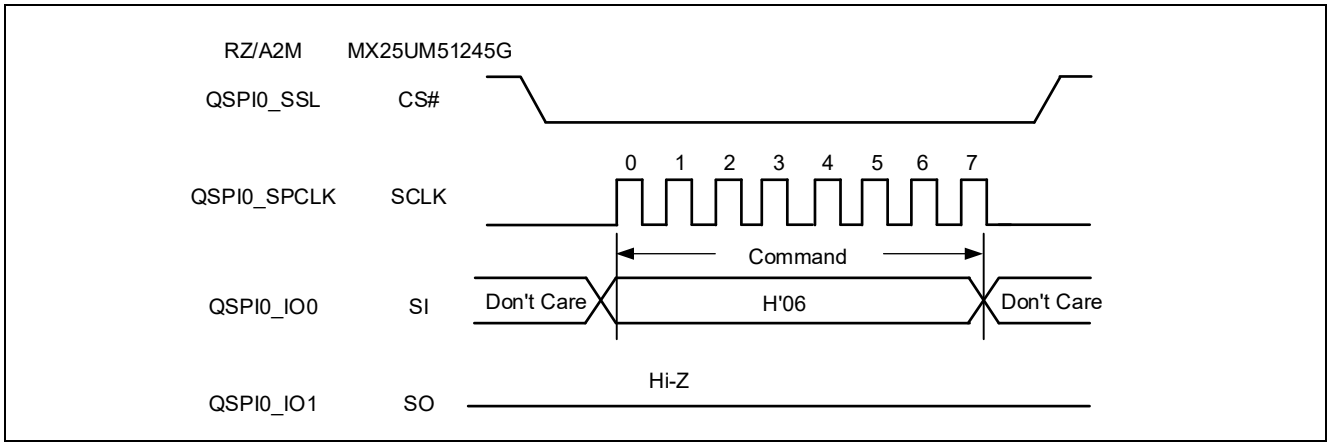


Figure 6.18 Waveform format of WREN command in SPI mode (reference)

Table 6.15 Command settings table for manual mode gs_command_table[10]: WREN command in DOPI mode

Member	Description	Setting value
uint8_t command_name[20]	Command identification character string	"DOPI_WREN"
uint8_t cmd	Command code	0x06
uint8_t cmd_width	Command bit width	SPIBSC_8BIT_WIDTH
uint8_t cmd_output_enable	Command output enable/disable	SPIBSC_OUTPUT_ENABLE
uint8_t ocmd	Optional command code	0xF9
uint8_t ocmd_width	Optional command bit width	SPIBSC_8BIT_WIDTH
uint8_t ocmd_enable	Optional command output enable/disable	SPIBSC_OUTPUT_DISABLE
uint8_t addr_width	Address bit width	SPIBSC_8BIT_WIDTH
uint8_t addr_output_enable	Address output setting	SPIBSC_OUTPUT_DISABLE
uint8_t addr_sdr_ddr	Address transfer method	SPIBSC_DDR_TRANSFER
uint8_t opdata_width	Option data bit width	SPIBSC_8BIT_WIDTH
uint8_t opdata_output_enable	Option data output setting	SPIBSC_OUTPUT_DISABLE
uint8_t opdata_ddr_enable	Option data transfer method	SPIBSC_DDR_TRANSFER
uint8_t opd3	Option Data3 (8bit) setting (outputs for the first)	0x00
uint8_t opd2	Option Data2 (8bit) setting (outputs for the second)	0x00
uint8_t opd1	Option Data1 (8bit) setting (outputs for the third)	0x00
uint8_t opd0	Option Data0 (8bit) setting (outputs for the fourth)	0x00
uint8_t dummy_cycle_output_enable	Dummy cycle output enable/disable	SPIBSC_OUTPUT_DISABLE
uint8_t dummy_cycle_count	Number of dummy cycles	0x00
uint8_t transfer_data_width	Transfer data bit width	SPIBSC_8BIT_WIDTH
uint8_t transfer_data_sdr_ddr	Transfer data transfer method	SPIBSC_DDR_TRANSFER

Note: CMNCR.MOIIOn (n = 0 to 3) is set to B'01 (output value is 1) and CMNCR.IOnFV (n = 0, 2, 3) is set to B'11 (output value is Hi-Z).

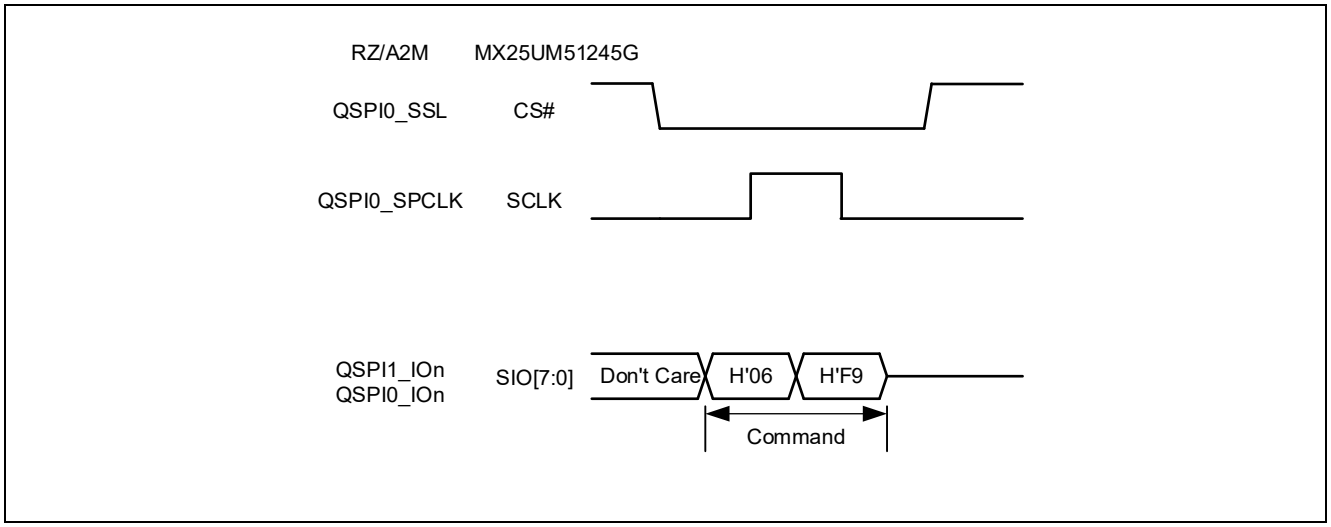


Figure 6.19 Waveform format of WREN command in DOPI mode (reference)

6.2.9 OctaFlash Status/Configuration Register Write

Implement the Userdef_SPIBSC_OCTAFLASH_WriteStatus function according to the specification of the OctaFlash to be used so that it can write the setting values for the status register and configuration register of OctaFlash.

Figure 6.20 shows the Userdef_SPIBSC_OCTAFLASH_WriteStatus function processing flow of the sample code.

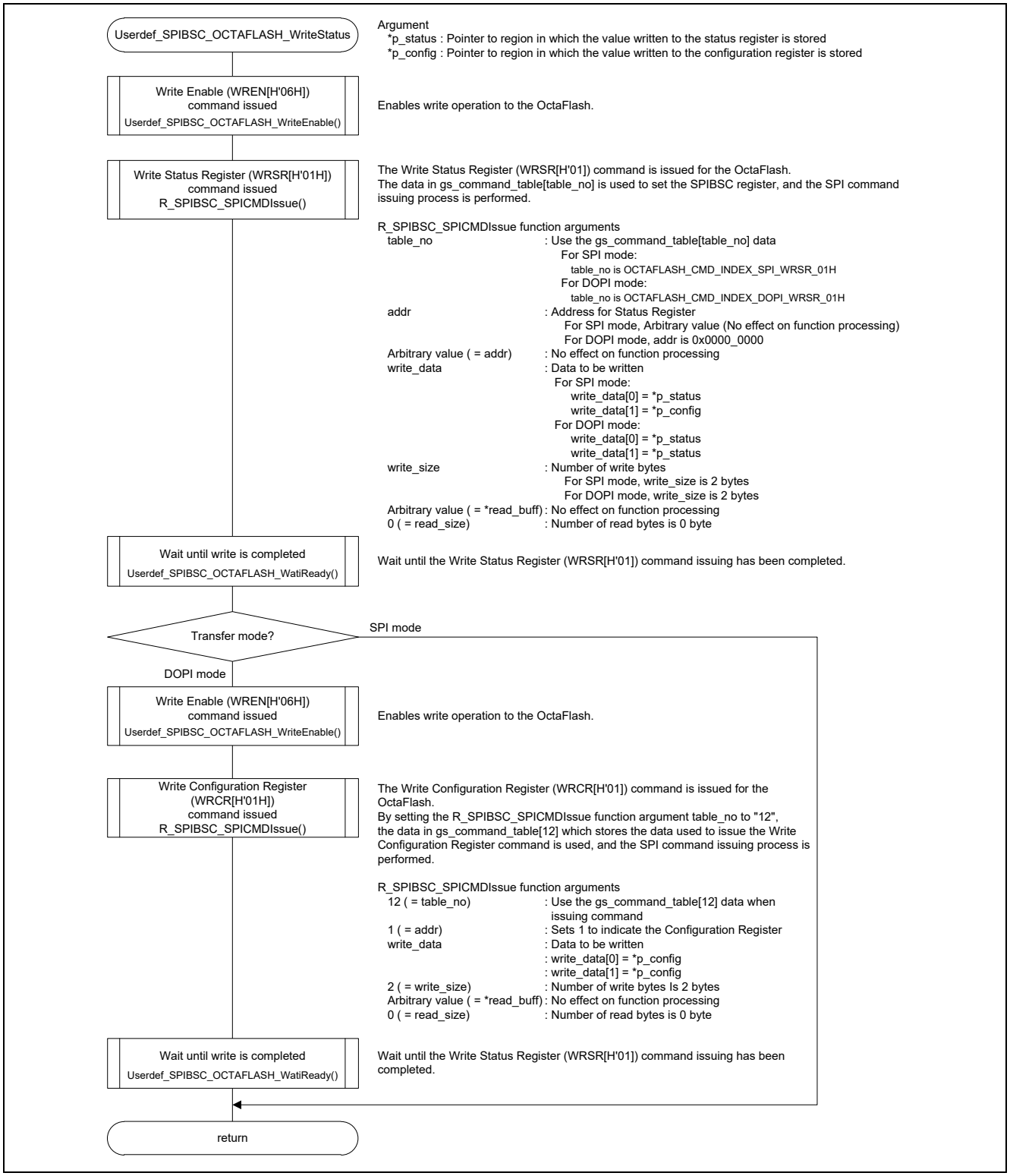


Figure 6.20 Userdef_SPIBSC_OCTAFLASH_WriteStatus function processing flow

Table 6.16 Command settings table for manual mode gs_command_table[4]: WRSR command in SPI mode

Member	Description	Setting value
uint8_t command_name[20]	Command identification character string	"SPI_WRSR"
uint8_t cmd	Command code	0x01
uint8_t cmd_width	Command bit width	SPIBSC_1BIT_WIDTH
uint8_t cmd_output_enable	Command output enable/disable	SPIBSC_OUTPUT_ENABLE
uint8_t ocmd	Optional command code	0x00
uint8_t ocmd_width	Optional command bit width	SPIBSC_1BIT_WIDTH
uint8_t ocmd_enable	Optional command output enable/disable	SPIBSC_OUTPUT_DISABLE
uint8_t addr_width	Address bit width	SPIBSC_1BIT_WIDTH
uint8_t addr_output_enable	Address output setting	SPIBSC_OUTPUT_DISABLE
uint8_t addr_sdr_ddr	Address transfer method	SPIBSC_SDR_TRANSFER
uint8_t opdata_width	Option data bit width	SPIBSC_1BIT_WIDTH
uint8_t opdata_output_enable	Option data output setting	SPIBSC_OUTPUT_DISABLE
uint8_t opdata_ddr_enable	Option data transfer method	SPIBSC_SDR_TRANSFER
uint8_t opd3	Option Data3 (8bit) setting (outputs for the first)	0x00
uint8_t opd2	Option Data2 (8bit) setting (outputs for the second)	0x00
uint8_t opd1	Option Data1 (8bit) setting (outputs for the third)	0x00
uint8_t opd0	Option Data0 (8bit) setting (outputs for the fourth)	0x00
uint8_t dummy_cycle_output_enable	Dummy cycle output enable/disable	SPIBSC_OUTPUT_DISABLE
uint8_t dummy_cycle_count	Number of dummy cycles	0x00
uint8_t transfer_data_width	Transfer data bit width	SPIBSC_1BIT_WIDTH
uint8_t transfer_data_sdr_ddr	Transfer data transfer method	SPIBSC_SDR_TRANSFER

Note: CMNCR.MOIIOn (n = 0 to 3) is set to B'01 (output value is 1) and CMNCR.IOnFV (n = 0, 2, 3) is set to B'11 (output value is Hi-Z).

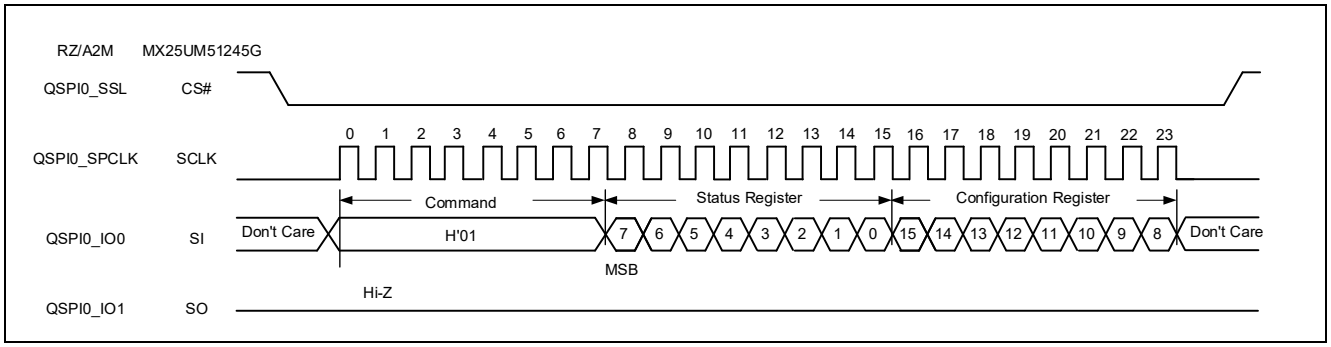


Figure 6.21 Waveform format of WRSR command in SPI mode (reference)

Table 6.17 Command settings table for manual mode gs_command_table[11]: WRSR command in DOPI mode

Member	Description	Setting value
uint8_t command_name[20]	Command identification character string	"DOPI_WRSR"
uint8_t cmd	Command code	0x01
uint8_t cmd_width	Command bit width	SPIBSC_8BIT_WIDTH
uint8_t cmd_output_enable	Command output enable/disable	SPIBSC_OUTPUT_ENABLE
uint8_t ocmd	Optional command code	0xFE
uint8_t ocmd_width	Optional command bit width	SPIBSC_8BIT_WIDTH
uint8_t ocmd_enable	Optional command output enable/disable	SPIBSC_OUTPUT_DISABLE
uint8_t addr_width	Address bit width	SPIBSC_8BIT_WIDTH
uint8_t addr_output_enable	Address output setting	SPIBSC_OUTPUT_ADDR_OCTA
uint8_t addr_sdr_ddr	Address transfer method	SPIBSC_DDR_TRANSFER
uint8_t opdata_width	Option data bit width	SPIBSC_8BIT_WIDTH
uint8_t opdata_output_enable	Option data output setting	SPIBSC_OUTPUT_DISABLE
uint8_t opdata_ddr_enable	Option data transfer method	SPIBSC_DDR_TRANSFER
uint8_t opd3	Option Data3 (8bit) setting (outputs for the first)	0x00
uint8_t opd2	Option Data2 (8bit) setting (outputs for the second)	0x00
uint8_t opd1	Option Data1 (8bit) setting (outputs for the third)	0x00
uint8_t opd0	Option Data0 (8bit) setting (outputs for the fourth)	0x00
uint8_t dummy_cycle_output_enable	Dummy cycle output enable/disable	SPIBSC_OUTPUT_DISABLE
uint8_t dummy_cycle_count	Number of dummy cycles	0x00
uint8_t transfer_data_width	Transfer data bit width	SPIBSC_8BIT_WIDTH
uint8_t transfer_data_sdr_ddr	Transfer data transfer method	SPIBSC_DDR_TRANSFER

Note: CMNCR.MOIIOn (n = 0 to 3) is set to B'01 (output value is 1) and CMNCR.IOnFV (n = 0, 2, 3) is set to B'11 (output value is Hi-Z).

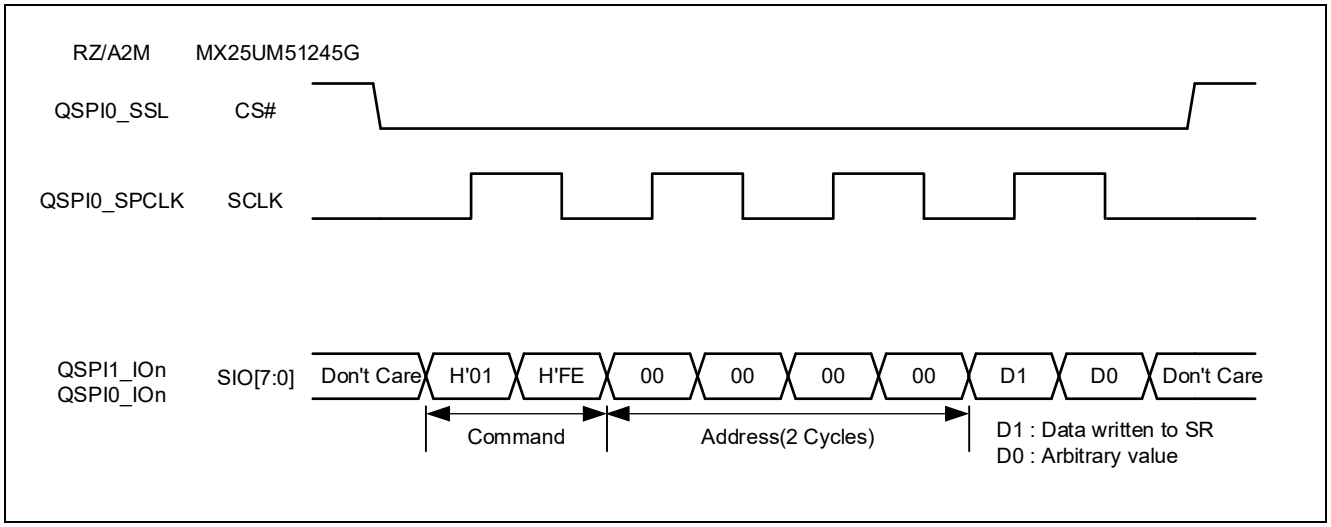


Figure 6.22 Waveform format of WRSR command in DOPI mode (reference)

Table 6.18 Command settings table for manual mode gs_command_table[12]: WRCR command in DOPI mode

Member	Description	Setting value
uint8_t command_name[20]	Command identification character string	"DOPI_WRCR"
uint8_t cmd	Command code	0x01
uint8_t cmd_width	Command bit width	SPIBSC_8BIT_WIDTH
uint8_t cmd_output_enable	Command output enable/disable	SPIBSC_OUTPUT_ENABLE
uint8_t ocmd	Optional command code	0xFE
uint8_t ocmd_width	Optional command bit width	SPIBSC_8BIT_WIDTH
uint8_t ocmd_enable	Optional command output enable/disable	SPIBSC_OUTPUT_DISABLE
uint8_t addr_width	Address bit width	SPIBSC_8BIT_WIDTH
uint8_t addr_output_enable	Address output setting	SPIBSC_OUTPUT_ADDR_OCTA
uint8_t addr_sdr_ddr	Address transfer method	SPIBSC_DDR_TRANSFER
uint8_t opdata_width	Option data bit width	SPIBSC_8BIT_WIDTH
uint8_t opdata_output_enable	Option data output setting	SPIBSC_OUTPUT_DISABLE
uint8_t opdata_ddr_enable	Option data transfer method	SPIBSC_DDR_TRANSFER
uint8_t opd3	Option Data3 (8bit) setting (outputs for the first)	0x00
uint8_t opd2	Option Data2 (8bit) setting (outputs for the second)	0x00
uint8_t opd1	Option Data1 (8bit) setting (outputs for the third)	0x00
uint8_t opd0	Option Data0 (8bit) setting (outputs for the fourth)	0x00
uint8_t dummy_cycle_output_enable	Dummy cycle output enable/disable	SPIBSC_OUTPUT_DISABLE
uint8_t dummy_cycle_count	Number of dummy cycles	0x00
uint8_t transfer_data_width	Transfer data bit width	SPIBSC_8BIT_WIDTH
uint8_t transfer_data_sdr_ddr	Transfer data transfer method	SPIBSC_DDR_TRANSFER

Note: CMNCR.MOIIOn (n = 0 to 3) is set to B'01 (output value is 1) and CMNCR.IOnFV (n = 0, 2, 3) is set to B'11 (output value is Hi-Z).

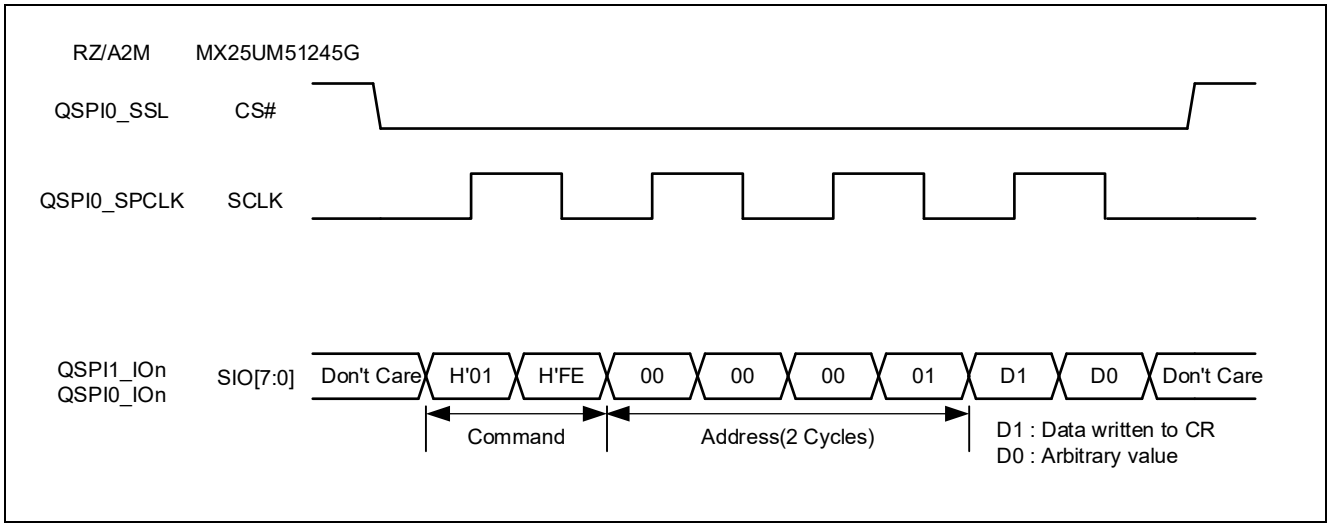


Figure 6.23 Waveform format of WRCR command in DOPI mode (reference)

6.2.10 OctaFlash Configuration Register 2 Write

Implement the Userdef_SPIBSC_OCTAFLASH_WriteConfig2 function according to the specification of the OctaFlash to be used so that it can write the setting values for the configuration register 2.

Figure 6.24 shows the Userdef_SPIBSC_OCTAFLASH_WriteConfig2 function processing flow of the sample code.

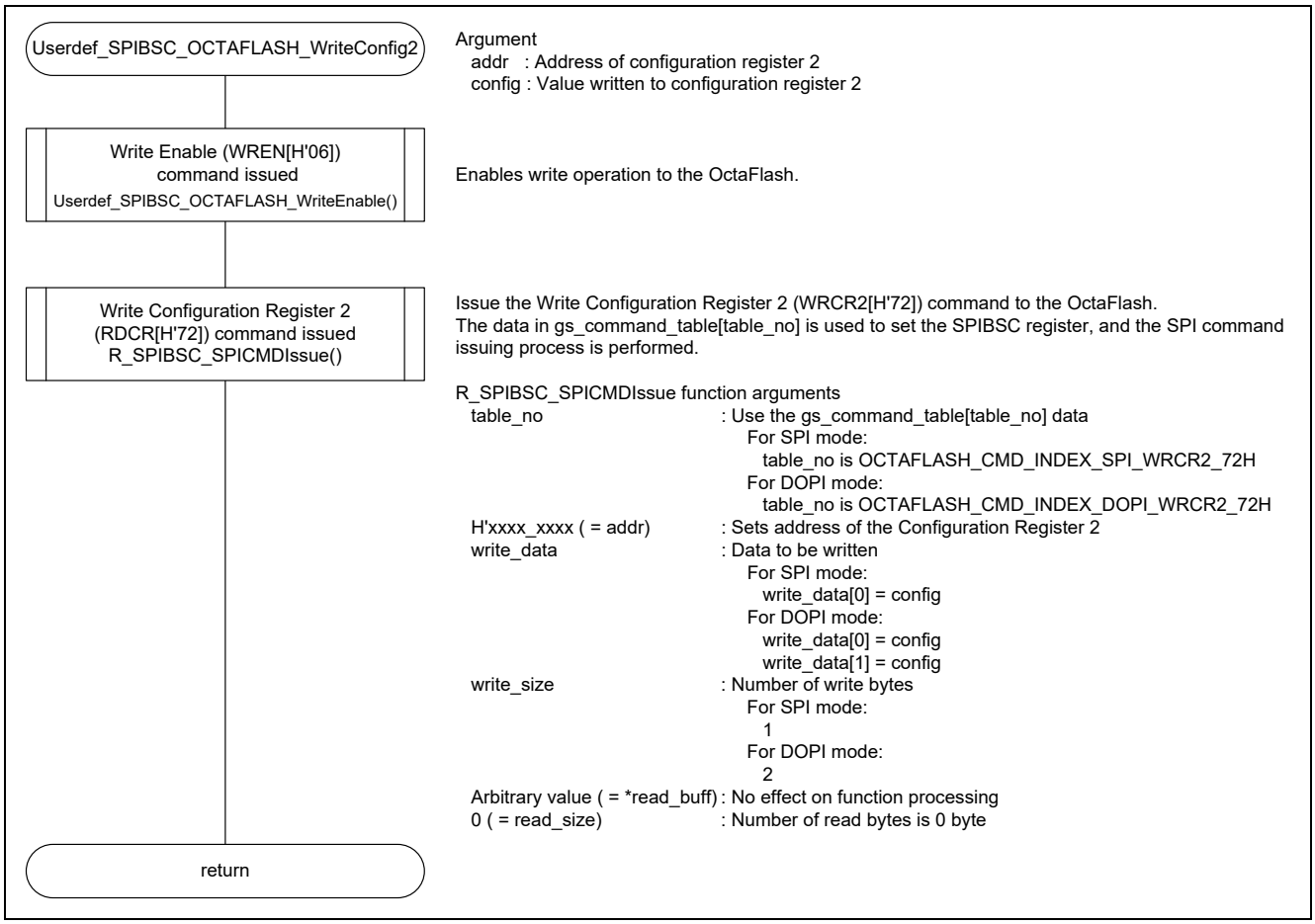


Figure 6.24 Userdef_SPIBSC_OCTAFLASH_WriteConfig2 function processing flow

Table 6.19 Command settings table for manual mode gs_command_table[5]: WRCR2 command in SPI mode

Member	Description	Setting value
uint8_t command_name[20]	Command identification character string	"SPI_WRCR2"
uint8_t cmd	Command code	0x72
uint8_t cmd_width	Command bit width	SPIBSC_1BIT_WIDTH
uint8_t cmd_output_enable	Command output enable/disable	SPIBSC_OUTPUT_ENABLE
uint8_t ocmd	Optional command code	0x00
uint8_t ocmd_width	Optional command bit width	SPIBSC_1BIT_WIDTH
uint8_t ocmd_enable	Optional command output enable/disable	SPIBSC_OUTPUT_DISABLE
uint8_t addr_width	Address bit width	SPIBSC_1BIT_WIDTH
uint8_t addr_output_enable	Address output setting	SPIBSC_OUTPUT_ADDR_32
uint8_t addr_sdr_ddr	Address transfer method	SPIBSC_SDR_TRANSFER
uint8_t opdata_width	Option data bit width	SPIBSC_1BIT_WIDTH
uint8_t opdata_output_enable	Option data output setting	SPIBSC_OUTPUT_DISABLE
uint8_t opdata_ddr_enable	Option data transfer method	SPIBSC_SDR_TRANSFER
uint8_t opd3	Option Data3 (8bit) setting (outputs for the first)	0x00
uint8_t opd2	Option Data2 (8bit) setting (outputs for the second)	0x00
uint8_t opd1	Option Data1 (8bit) setting (outputs for the third)	0x00
uint8_t opd0	Option Data0 (8bit) setting (outputs for the fourth)	0x00
uint8_t dummy_cycle_output_enable	Dummy cycle output enable/disable	SPIBSC_OUTPUT_DISABLE
uint8_t dummy_cycle_count	Number of dummy cycles	0x00
uint8_t transfer_data_width	Transfer data bit width	SPIBSC_1BIT_WIDTH
uint8_t transfer_data_sdr_ddr	Transfer data transfer method	SPIBSC_SDR_TRANSFER

Note: CMNCR.MOIIOn (n = 0 to 3) is set to B'01 (output value is 1) and CMNCR.IOnFV (n = 0, 2, 3) is set to B'11 (output value is Hi-Z).

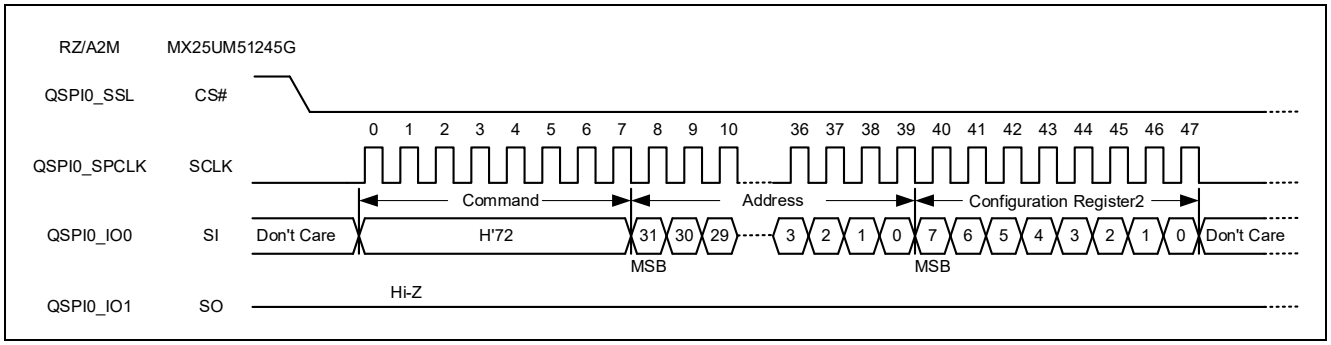


Figure 6.25 Waveform format of WRCR2 command in SPI mode (reference)

Table 6.20 Command settings table for manual mode gs_command_table[13]: WRCR2 command in DOPI mode

Member	Description	Setting value
uint8_t command_name[20]	Command identification character string	"DOPI_WRCR2"
uint8_t cmd	Command code	0x72
uint8_t cmd_width	Command bit width	SPIBSC_8BIT_WIDTH
uint8_t cmd_output_enable	Command output enable/disable	SPIBSC_OUTPUT_ENABLE
uint8_t ocmd	Optional command code	0x8D
uint8_t ocmd_width	Optional command bit width	SPIBSC_8BIT_WIDTH
uint8_t ocmd_enable	Optional command output enable/disable	SPIBSC_OUTPUT_DISABLE
uint8_t addr_width	Address bit width	SPIBSC_8BIT_WIDTH
uint8_t addr_output_enable	Address output setting	SPIBSC_OUTPUT_ADDR_OCTA
uint8_t addr_sdr_ddr	Address transfer method	SPIBSC_DDR_TRANSFER
uint8_t opdata_width	Option data bit width	SPIBSC_8BIT_WIDTH
uint8_t opdata_output_enable	Option data output setting	SPIBSC_OUTPUT_DISABLE
uint8_t opdata_ddr_enable	Option data transfer method	SPIBSC_DDR_TRANSFER
uint8_t opd3	Option Data3 (8bit) setting (outputs for the first)	0x00
uint8_t opd2	Option Data2 (8bit) setting (outputs for the second)	0x00
uint8_t opd1	Option Data1 (8bit) setting (outputs for the third)	0x00
uint8_t opd0	Option Data0 (8bit) setting (outputs for the fourth)	0x00
uint8_t dummy_cycle_output_enable	Dummy cycle output enable/disable	SPIBSC_OUTPUT_DISABLE
uint8_t dummy_cycle_count	Number of dummy cycles	0x00
uint8_t transfer_data_width	Transfer data bit width	SPIBSC_8BIT_WIDTH
uint8_t transfer_data_sdr_ddr	Transfer data transfer method	SPIBSC_DDR_TRANSFER

Note: CMNCR.MOIIOn (n = 0 to 3) is set to B'01 (output value is 1) and CMNCR.IOnFV (n = 0, 2, 3) is set to B'11 (output value is Hi-Z).

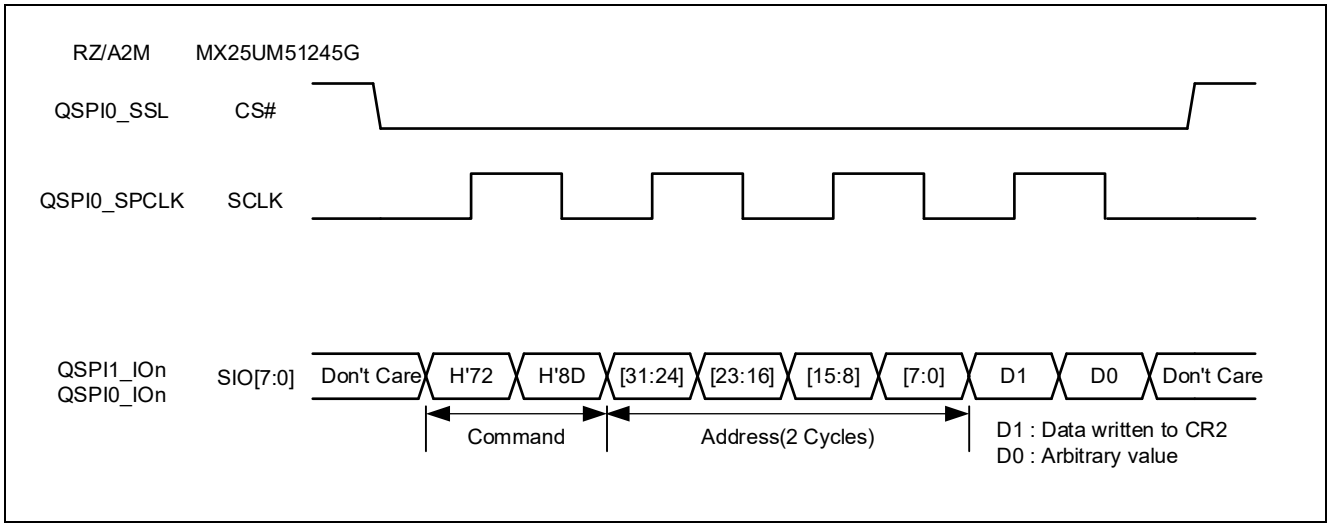


Figure 6.26 Waveform format of WRCR2 command in DOPI mode (reference)

6.2.11 OctaFlash ID Information Read

In the sample code, OctaFlash ID is read using the Userdef_SPIBSC_OCTAFLASH_ReadId function.

Implement the Userdef_SPIBSC_OCTAFLASH_ReadId function according to the specifications for the OctaFlash to be used so that it can read the OctaFlash ID.

Figure 6.27 shows the Userdef_SPIBSC_OCTAFLASH_ReadId function processing flow of the sample code.

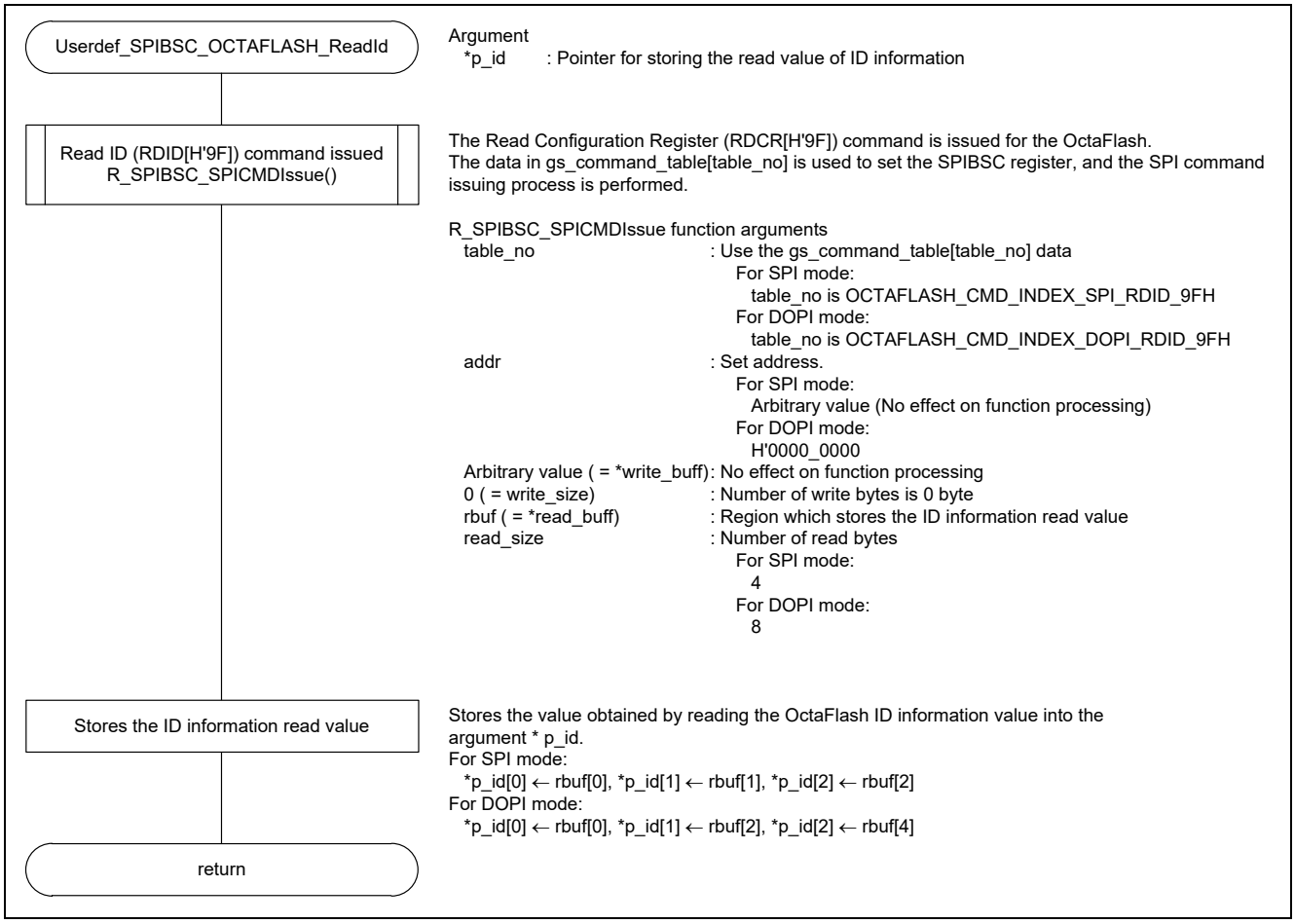


Figure 6.27 Userdef_SPIBSC_OCTAFLASH_ReadId function processing flow

Table 6.21 Command settings table for manual mode gs_command_table[6]: RDID command in SPI mode

Member	Description	Setting value
uint8_t command_name[20]	Command identification character string	"SPI_RDID"
uint8_t cmd	Command code	0x9F
uint8_t cmd_width	Command bit width	SPIBSC_1BIT_WIDTH
uint8_t cmd_output_enable	Command output enable/disable	SPIBSC_OUTPUT_ENABLE
uint8_t ocmd	Optional command code	0x00
uint8_t ocmd_width	Optional command bit width	SPIBSC_1BIT_WIDTH
uint8_t ocmd_enable	Optional command output enable/disable	SPIBSC_OUTPUT_DISABLE
uint8_t addr_width	Address bit width	SPIBSC_1BIT_WIDTH
uint8_t addr_output_enable	Address output setting	SPIBSC_OUTPUT_ADDR_32
uint8_t addr_sdr_ddr	Address transfer method	SPIBSC_SDR_TRANSFER
uint8_t opdata_width	Option data bit width	SPIBSC_1BIT_WIDTH
uint8_t opdata_output_enable	Option data output setting	SPIBSC_OUTPUT_DISABLE
uint8_t opdata_ddr_enable	Option data transfer method	SPIBSC_SDR_TRANSFER
uint8_t opd3	Option Data3 (8bit) setting (outputs for the first)	0x00
uint8_t opd2	Option Data2 (8bit) setting (outputs for the second)	0x00
uint8_t opd1	Option Data1 (8bit) setting (outputs for the third)	0x00
uint8_t opd0	Option Data0 (8bit) setting (outputs for the fourth)	0x00
uint8_t dummy_cycle_output_enable	Dummy cycle output enable/disable	SPIBSC_OUTPUT_DISABLE
uint8_t dummy_cycle_count	Number of dummy cycles	0x00
uint8_t transfer_data_width	Transfer data bit width	SPIBSC_1BIT_WIDTH
uint8_t transfer_data_sdr_ddr	Transfer data transfer method	SPIBSC_SDR_TRANSFER

Note: CMNCR.MOIIOn (n = 0 to 3) is set to B'01 (output value is 1) and CMNCR.IOnFV (n = 0, 2, 3) is set to B'11 (output value is Hi-Z).

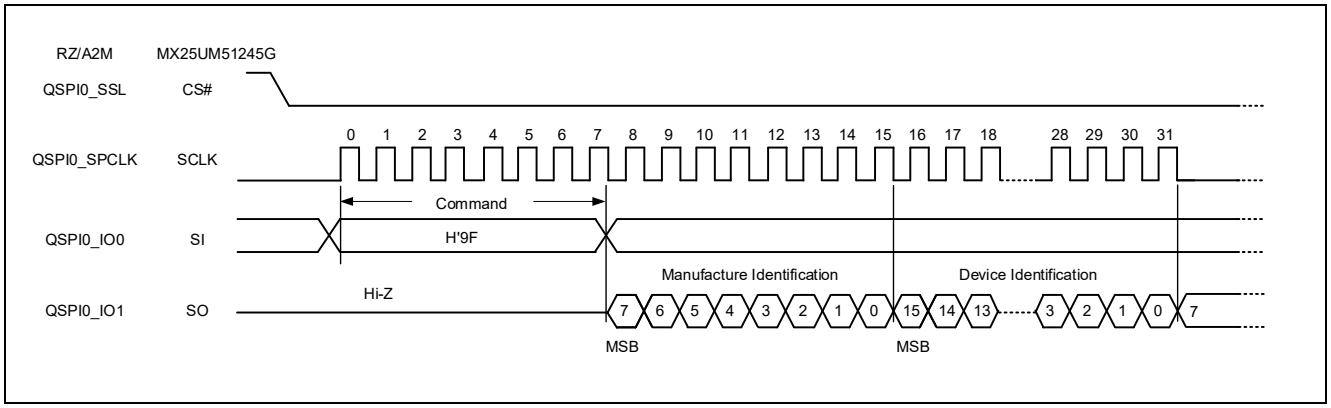


Figure 6.28 Waveform format of RDID command in SPI mode (reference)

Table 6.22 Command settings table for manual mode gs_command_table[14]: RDID command in DOPI mode

Member	Description	Setting value
uint8_t command_name[20]	Command identification character string	"DOPI_RDID"
uint8_t cmd	Command code	0x9F
uint8_t cmd_width	Command bit width	SPIBSC_8BIT_WIDTH
uint8_t cmd_output_enable	Command output enable/disable	SPIBSC_OUTPUT_ENABLE
uint8_t ocmd	Optional command code	0x60
uint8_t ocmd_width	Optional command bit width	SPIBSC_8BIT_WIDTH
uint8_t ocmd_enable	Optional command output enable/disable	SPIBSC_OUTPUT_DISABLE
uint8_t addr_width	Address bit width	SPIBSC_8BIT_WIDTH
uint8_t addr_output_enable	Address output setting	SPIBSC_OUTPUT_ADDR_OCTA
uint8_t addr_sdr_ddr	Address transfer method	SPIBSC_DDR_TRANSFER
uint8_t opdata_width	Option data bit width	SPIBSC_8BIT_WIDTH
uint8_t opdata_output_enable	Option data output setting	SPIBSC_OUTPUT_DISABLE
uint8_t opdata_ddr_enable	Option data transfer method	SPIBSC_DDR_TRANSFER
uint8_t opd3	Option Data3 (8bit) setting (outputs for the first)	0x00
uint8_t opd2	Option Data2 (8bit) setting (outputs for the second)	0x00
uint8_t opd1	Option Data1 (8bit) setting (outputs for the third)	0x00
uint8_t opd0	Option Data0 (8bit) setting (outputs for the fourth)	0x00
uint8_t dummy_cycle_output_enable	Dummy cycle output enable/disable	SPIBSC_OUTPUT_DISABLE
uint8_t dummy_cycle_count	Number of dummy cycles	SPIBSC_DUMMY_14CYC
uint8_t transfer_data_width	Transfer data bit width	SPIBSC_8BIT_WIDTH
uint8_t transfer_data_sdr_ddr	Transfer data transfer method	SPIBSC_DDR_TRANSFER

Note: CMNCR.MOIIOn (n = 0 to 3) is set to B'01 (output value is 1) and CMNCR.IOnFV (n = 0, 2, 3) is set to B'11 (output value is Hi-Z).

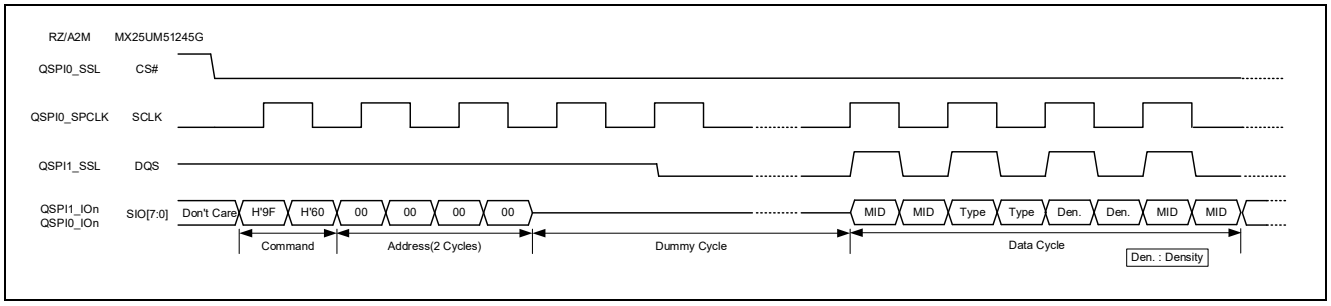


Figure 6.29 Waveform format of RDID command in DOPI mode (reference)

6.2.12 OctaFlash Data Read

In the sample code, OctaFlash data is read using the Userdef_SPIBSC_OCTAFLASH_Read function.

Implement the Userdef_SPIBSC_OCTAFLASH_Read function according to the specifications for the OctaFlash to be used so that it can read the OctaFlash data.

Figure 6.30 shows the Userdef_SPIBSC_OCTAFLASH_Read function processing flow of the sample code.

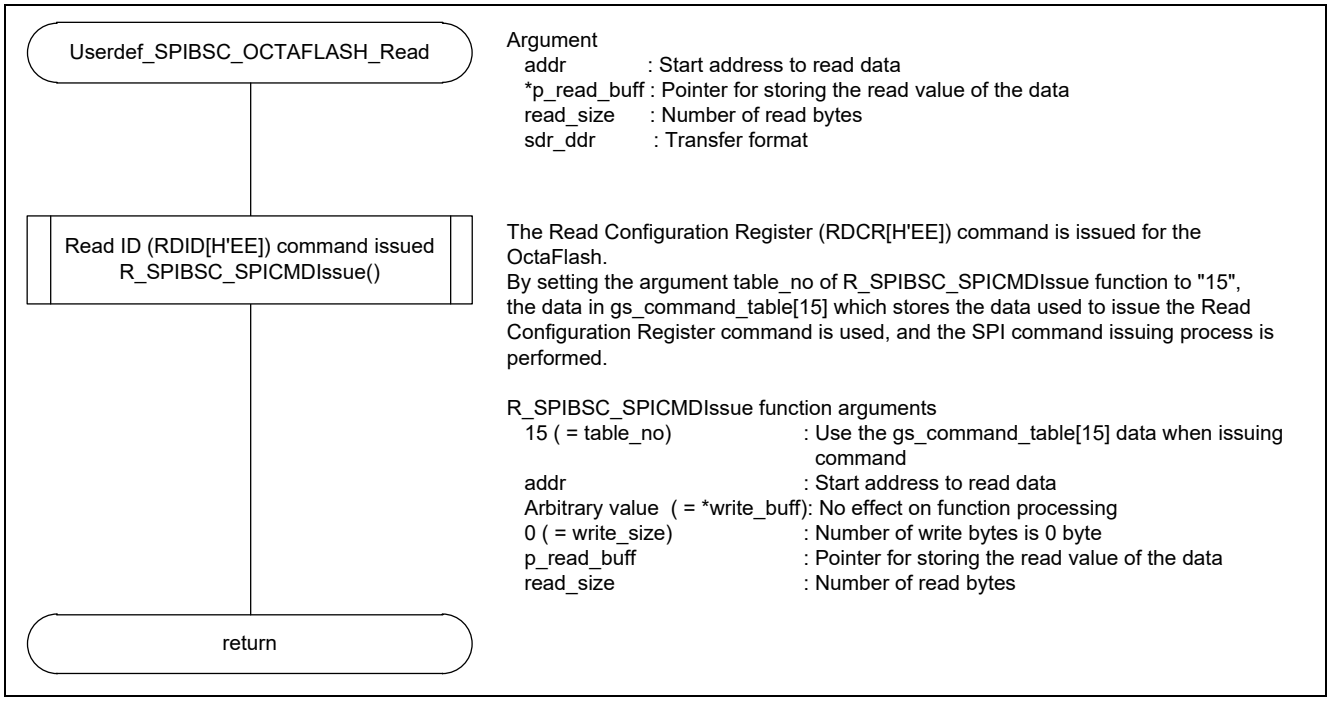


Figure 6.30 Userdef_SPIBSC_OCTAFLASH_Read function processing flow

Table 6.23 Command settings table for manual mode gs_command_table[15]: 8DTRD command in DOPI mode

Member	Description	Setting value
uint8_t command_name[20]	Command identification character string	"DOPI_8DTRD"
uint8_t cmd	Command code	0xEE
uint8_t cmd_width	Command bit width	SPIBSC_8BIT_WIDTH
uint8_t cmd_output_enable	Command output enable/disable	SPIBSC_OUTPUT_ENABLE
uint8_t ocmd	Optional command code	0x11
uint8_t ocmd_width	Optional command bit width	SPIBSC_8BIT_WIDTH
uint8_t ocmd_enable	Optional command output enable/disable	SPIBSC_OUTPUT_DISABLE
uint8_t addr_width	Address bit width	SPIBSC_8BIT_WIDTH
uint8_t addr_output_enable	Address output setting	SPIBSC_OUTPUT_ADDR_OCTA
uint8_t addr_sdr_ddr	Address transfer method	SPIBSC_DDR_TRANSFER
uint8_t opdata_width	Option data bit width	SPIBSC_8BIT_WIDTH
uint8_t opdata_output_enable	Option data output setting	SPIBSC_OUTPUT_DISABLE
uint8_t opdata_ddr_enable	Option data transfer method	SPIBSC_DDR_TRANSFER
uint8_t opd3	Option Data3 (8bit) setting (outputs for the first)	0x00
uint8_t opd2	Option Data2 (8bit) setting (outputs for the second)	0x00
uint8_t opd1	Option Data1 (8bit) setting (outputs for the third)	0x00
uint8_t opd0	Option Data0 (8bit) setting (outputs for the fourth)	0x00
uint8_t dummy_cycle_output_enable	Dummy cycle output enable/disable	SPIBSC_OUTPUT_ENABLE
uint8_t dummy_cycle_count	Number of dummy cycles	SPIBSC_DUMMY_14CYC
uint8_t transfer_data_width	Transfer data bit width	SPIBSC_8BIT_WIDTH
uint8_t transfer_data_sdr_ddr	Transfer data transfer method	SPIBSC_DDR_TRANSFER

Note: CMNCR.MOIIOn (n = 0 to 3) is set to B'01 (output value is 1) and CMNCR.IOnFV (n = 0, 2, 3) is set to B'11 (output value is Hi-Z).

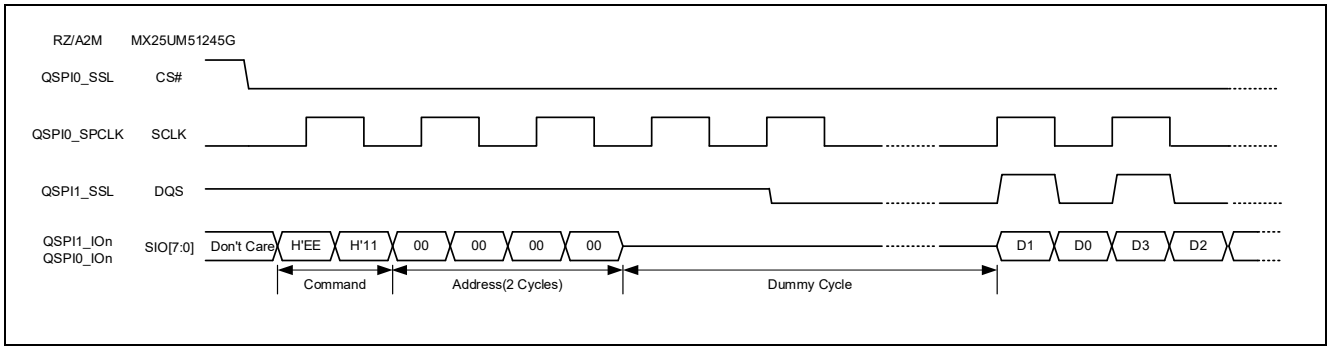


Figure 6.31 Waveform format of 8DTRD command in DOPI mode (reference)

6.2.13 OctaFlash Sector Erasure

In the sample code, OctaFlash sectors are erased using the Userdef_SPIBSC_OCTAFLASH_Erase function.

Implement the Userdef_SPIBSC_OCTAFLASH_Erase function according to the specifications of the OctaFlash to be used so that it can erase the OctaFlash sectors.

Figure 6.32 shows the Userdef_SPIBSC_OCTAFLASH_Erase function processing flow of the sample code.

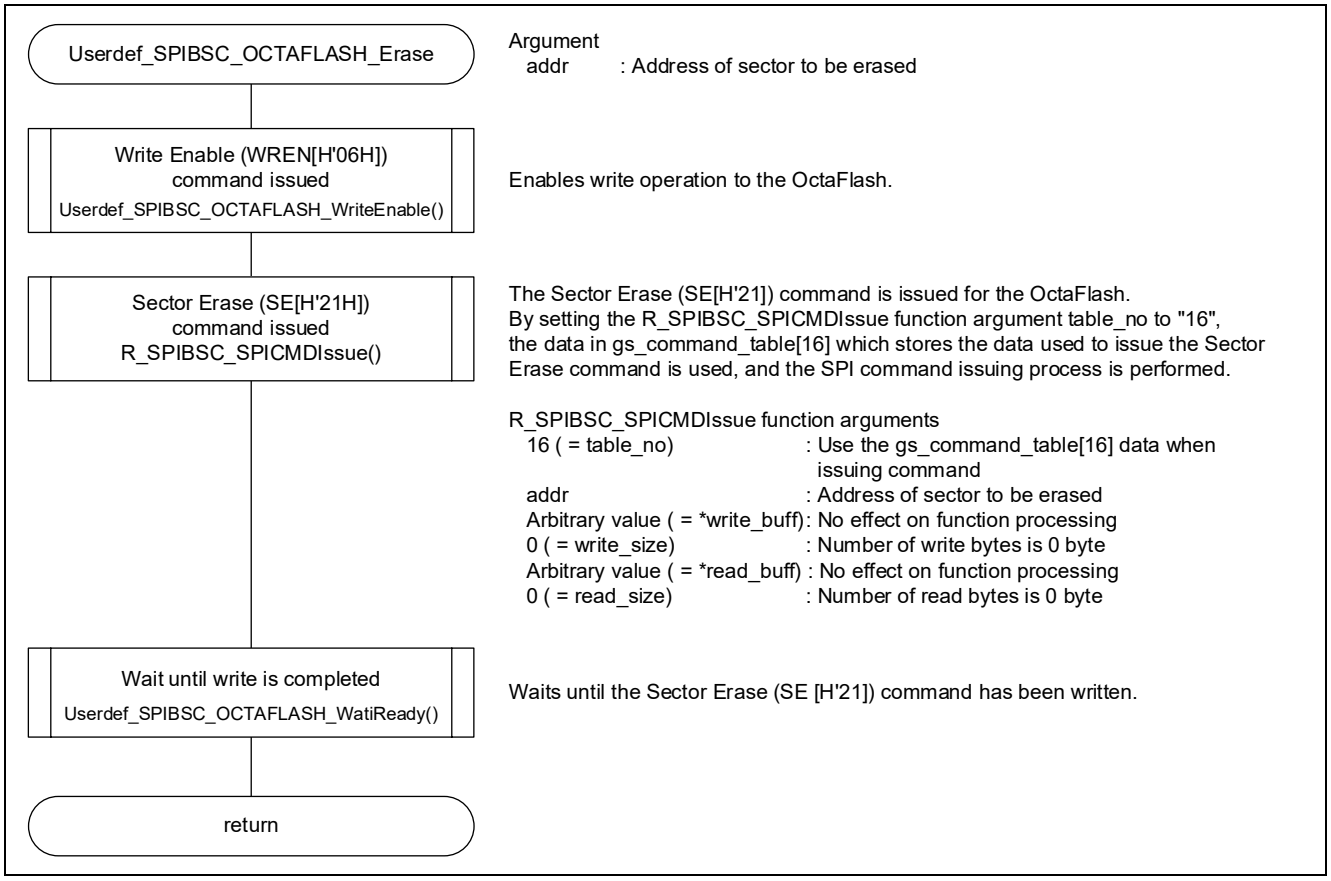


Figure 6.32 Userdef_SPIBSC_OCTAFLASH_Erase function processing flow

Table 6.24 Command settings table for manual mode gs_command_table[16]: SE command in DOPI mode

Member	Description	Setting value
uint8_t command_name[20]	Command identification character string	"DOPI_SE"
uint8_t cmd	Command code	0x21
uint8_t cmd_width	Command bit width	SPIBSC_8BIT_WIDTH
uint8_t cmd_output_enable	Command output enable/disable	SPIBSC_OUTPUT_ENABLE
uint8_t ocmd	Optional command code	0xDE
uint8_t ocmd_width	Optional command bit width	SPIBSC_8BIT_WIDTH
uint8_t ocmd_enable	Optional command output enable/disable	SPIBSC_OUTPUT_DISABLE
uint8_t addr_width	Address bit width	SPIBSC_8BIT_WIDTH
uint8_t addr_output_enable	Address output setting	SPIBSC_OUTPUT_ADDR_OCTA
uint8_t addr_sdr_ddr	Address transfer method	SPIBSC_DDR_TRANSFER
uint8_t opdata_width	Option data bit width	SPIBSC_8BIT_WIDTH
uint8_t opdata_output_enable	Option data output setting	SPIBSC_OUTPUT_DISABLE
uint8_t opdata_ddr_enable	Option data transfer method	SPIBSC_DDR_TRANSFER
uint8_t opd3	Option Data3 (8bit) setting (outputs for the first)	0x00
uint8_t opd2	Option Data2 (8bit) setting (outputs for the second)	0x00
uint8_t opd1	Option Data1 (8bit) setting (outputs for the third)	0x00
uint8_t opd0	Option Data0 (8bit) setting (outputs for the fourth)	0x00
uint8_t dummy_cycle_output_enable	Dummy cycle output enable/disable	SPIBSC_OUTPUT_DISABLE
uint8_t dummy_cycle_count	Number of dummy cycles	0x00
uint8_t transfer_data_width	Transfer data bit width	SPIBSC_8BIT_WIDTH
uint8_t transfer_data_sdr_ddr	Transfer data transfer method	SPIBSC_DDR_TRANSFER

Note: CMNCR.MOIIOn (n = 0 to 3) is set to B'01 (output value is 1) and CMNCR.IOnFV (n = 0, 2, 3) is set to B'11 (output value is Hi-Z).

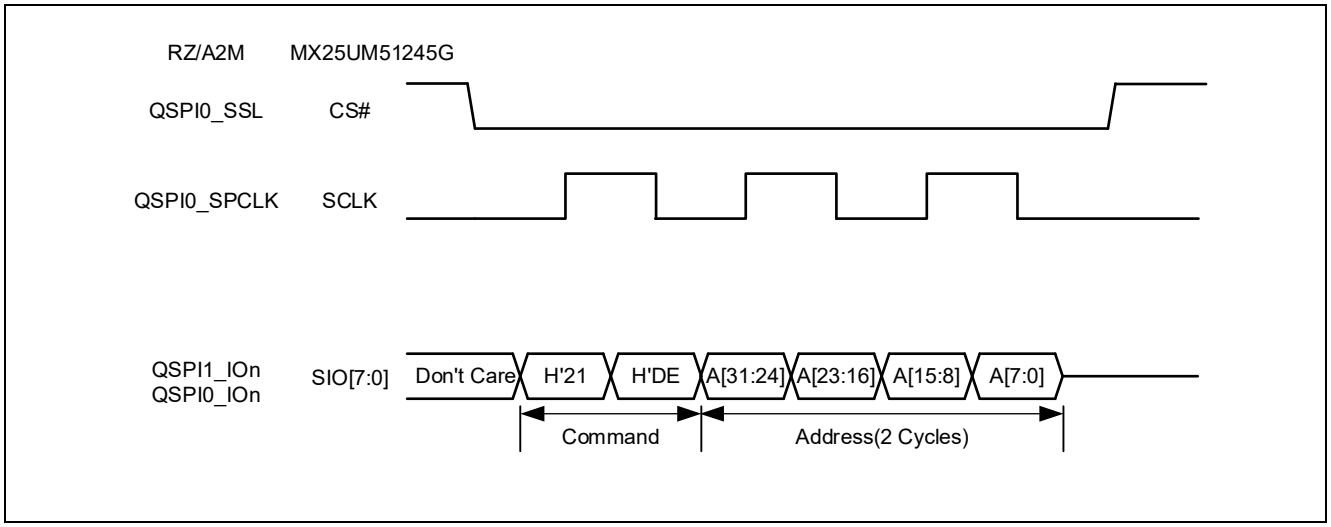


Figure 6.33 Waveform format of SE command in DOPI mode (reference)

6.2.14 OctaFlash Data Write

In the sample code, OctaFlash is programmed using the Userdef_SPIBSC_OCTAFLASH_Write function.

Implement the Userdef_SPIBSC_OCTAFLASH_Write function according to the specifications for the OctaFlash to be used so that it can program to the OctaFlash.

Figure 6.34 shows the Userdef_SPIBSC_OCTAFLASH_Write function processing flow of the sample code.

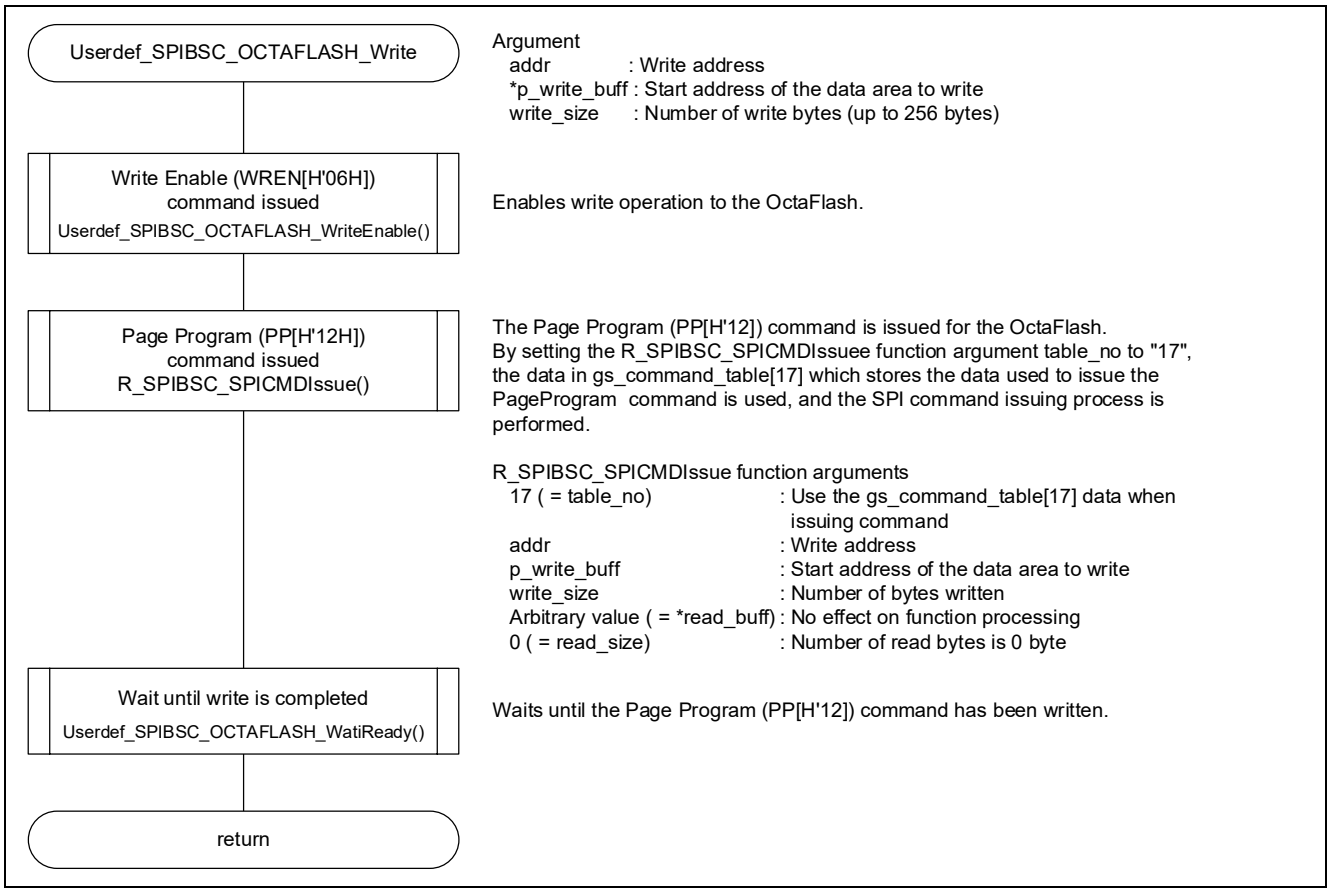


Figure 6.34 Userdef_SPIBSC_OCTAFLASH_Write function processing flow

Table 6.25 Command settings table for manual mode gs_command_table[17]: PP command in DOPI mode

Member	Description	Setting value
uint8_t command_name[20]	Command identification character string	"DOPI_PP"
uint8_t cmd	Command code	0x12
uint8_t cmd_width	Command bit width	SPIBSC_8BIT_WIDTH
uint8_t cmd_output_enable	Command output enable/disable	SPIBSC_OUTPUT_ENABLE
uint8_t ocmd	Optional command code	0xED
uint8_t ocmd_width	Optional command bit width	SPIBSC_8BIT_WIDTH
uint8_t ocmd_enable	Optional command output enable/disable	SPIBSC_OUTPUT_DISABLE
uint8_t addr_width	Address bit width	SPIBSC_8BIT_WIDTH
uint8_t addr_output_enable	Address output setting	SPIBSC_OUTPUT_ADDR_OCTA
uint8_t addr_sdr_ddr	Address transfer method	SPIBSC_DDR_TRANSFER
uint8_t opdata_width	Option data bit width	SPIBSC_8BIT_WIDTH
uint8_t opdata_output_enable	Option data output setting	SPIBSC_OUTPUT_DISABLE
uint8_t opdata_ddr_enable	Option data transfer method	SPIBSC_DDR_TRANSFER
uint8_t opd3	Option Data3 (8bit) setting (outputs for the first)	0x00
uint8_t opd2	Option Data2 (8bit) setting (outputs for the second)	0x00
uint8_t opd1	Option Data1 (8bit) setting (outputs for the third)	0x00
uint8_t opd0	Option Data0 (8bit) setting (outputs for the fourth)	0x00
uint8_t dummy_cycle_output_enable	Dummy cycle output enable/disable	SPIBSC_OUTPUT_DISABLE
uint8_t dummy_cycle_count	Number of dummy cycles	0x00
uint8_t transfer_data_width	Transfer data bit width	SPIBSC_8BIT_WIDTH
uint8_t transfer_data_sdr_ddr	Transfer data transfer method	SPIBSC_DDR_TRANSFER

Note: CMNCR.MOIIOn (n = 0 to 3) is set to B'01 (output value is 1) and CMNCR.IOnFV (n = 0, 2, 3) is set to B'11 (output value is Hi-Z).

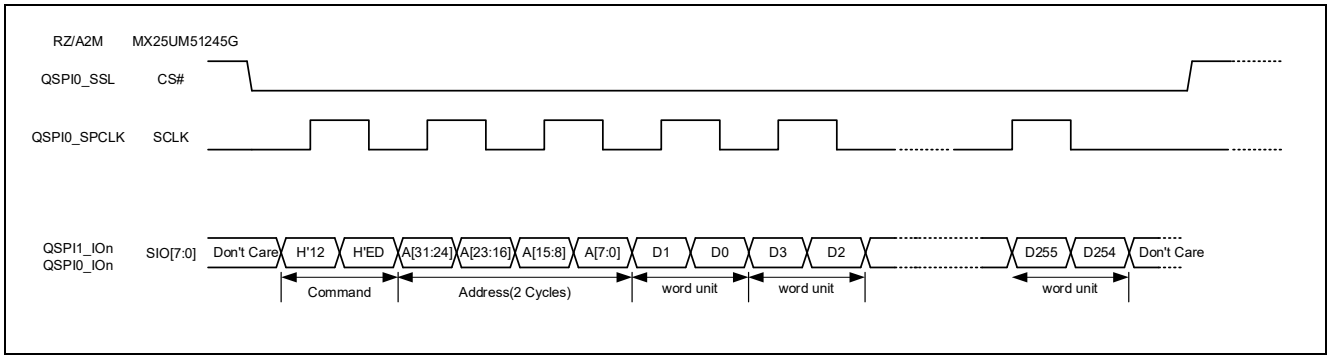


Figure 6.35 Waveform format of PP command in DOPI mode (reference)

7. Sample Code Precautions

7.1 Accessible area in external address space read mode

The accessible area in external address space read mode is a 256MB area assigned to the SPI multi-IO bus space (H'2000_0000 to H'2FFF_FFFF). The SPIBSC converts access to this area to H'0000_0000 to H'0FFF_FFFF in the OctaFlash to access it. In the sample code, a 256MB area from H'0000_0000 to H'0FFF_FFFF in the OctaFlash can be accessed. In the RZ/A2M, an area larger than 256MB can be accessed by controlling the SPIBSC data read expansion address setting register (DREAR) and changing the OctaFlash address allocated to the SPI multi-I/O bus space, but since this prevents access to the area before DREAR is controlled, access to an area larger than 256MB is not supported in the sample code. The access specifications are only for H'0000_0000 to H'0FFF_FFFF in the OctaFlash.

In manual mode, access using a 4-byte address is supported, and a 4GB area of the OctaFlash can be accessed.

7.2 Commands that can be issued to OctaFlash

Only SPI mode commands can be issued to OctaFlash in the loader program, and only DOPI mode commands can be issued in the application program. After branching to the application program, no SPI mode commands can be issued.

8. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

9. Reference Documents

User's Manual: Hardware

RZ/A2M Group User's Manual: Hardware
The latest version can be downloaded from the Renesas Electronics website.

RTK7921053C00000BE (RZ/A2M CPU board) User's Manual
The latest version can be downloaded from the Renesas Electronics website.

RTK79210XXB00000BE (RZ/A2M SUB board) User's Manual
The latest version can be downloaded from the Renesas Electronics website.

Arm Architecture Reference Manual ARMv7-A and ARMv7-R edition Issue C
The latest version can be downloaded from the Arm website.

Arm Cortex™-A9 Technical Reference Manual Revision: r4p1
The latest version can be downloaded from the Arm website.

Arm Generic Interrupt Controller Architecture Specification - Architecture version2.0
The latest version can be downloaded from the Arm website.

Arm CoreLink™ Level 2 Cache Controller L2C-310 Technical Reference Manual Revision: r3p3
The latest version can be downloaded from the Arm website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

User's Manual: Integrated Development Environment

The e^2 studio Integrated Development Environment user's manual can be downloaded from the Renesas Electronics website.
The latest version can be downloaded from the Renesas Electronics website.

Revision History

Rev.	Date	Description	
		Page	Summary
Rev.1.00	Jun.22.20	–	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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