RX66T Group, RX24T Group

Differences Between the RX66T Group and the RX24T Group

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Introduction

This application note is the reference document to show differences in peripheral modules, I/O registers, and pin functions between the RX66T Group and the RX24T Group. This document also provides the important information that needs to be taken into account when replacing the MCU.

With regard to maximum MCU specifications, this application note describes differences between RX66T Group products with 144 pins (with programmable gain amplifier (PGA), pseudo-differential input, and USB pins) and RX24T Group products with 100 pins (part numbers with suffix #31 (for orders), chip version B), unless explicitly stated otherwise. Refer to each User's Manual: Hardware for details on differences in electrical characteristics, usage notes, and setting procedures.

Target Devices

RX66T Group
RX24T Group

Contents

1. Comparison of Build-In Functions Between RX66T Group and RX24T Group

Table 1.1 lists the Comparison of Build-In Functions Between RX24T and RX66T.
For details of each function, refer to 2. Comparison of Specifications Overview as well as documents listed in 5.Reference Documents.

Table 1.1 Comparison of Build-In Functions Between RX24T and RX66T

Function	RX24T	RX66T
CPU	✦	
Operating Modes	✦	
Resets	✦	
Option-Setting Memory	✦	
Voltage Detection Circuit (LVDAb):RX24T, (LVDA):RX66T	✦	
Clock Generation Circuit	✦	
Clock Frequency Accuracy Measurement Circuit (CAC)	✓	
Low Power Consumption	✦	
Register Write Protection Function	✦	
Exception Handling	✓	
Interrupt Controller (ICUb):RX24T, (ICUC):RX66T	✦	
Buses	✦	
Memory-Protection Unit (MPU)	✓	
DMA Controller (DMACAa)	×	✓
Data Transfer Controller (DTCa)	✦	
Event Link Controller (ELC)	×	✓
I/OPorts	✦	
Multi-Function Pin Controller (MPC)	✦	
Multi-Function Timer Pulse Unit 3 (MTU3d)	✦	
Port Output Enable 3 (POE3b, POE3A):RX24T, (POE3B):RX66T	✦	
General PWM Timer (GPTB):RX24T, (GPTW):RX66T	✦	
High Resolution PWM Waveform Generation Circuit (HRPWM)	×	✓
GPTW Port Output Enable (POEG)	×	✓
8-Bit Timer (TMR)	✦	
Compare Match Timer (CMT)	✦	
Watchdog Timer (WDTA)	×	✓
Independent Watchdog Timer (IWDTa)	✦	
USB 2.0 FS Host/Function Module (USBb)	×	✓
Serial Communications Interface (SCIg):RX24T Serial Communications Interface (SCIj, SCIi, SCIh):RX66T	✦	
I2C-bus Interface (RIICa)	✦	
CAN Module (RSCAN):RX24T, (CAN)RX66T	✦	
Serial Peripheral Interface (RSPIb):RX24T, (RSPIc):RX66T	✦	
CRC Calculator (CRC):RX24T, (CRCA):RX66T	✦	
Trusted Secure IP(TSIP-Lite)	×	✓
12-Bit A/D Converter (S12ADF):RX24T, (S12ADH):RX66T	✦	
D/A Converter (DA, DAa):RX24T, 12-Bit D/A Converter (R12DAb):RX66T	✦	
Temperature Sensor (TEMPS)	×	✓

Function	RX24T	RX66T
Comparator C (CMPC)	✦	
Data Operation Circuit (DOC)	✦	
RAM	✦	
Flash Memory (ROM (Flash Memory for Code Storage), E2 DataFlash (Flash Memory for Data Storage)):RX24T Flash Memory (Code Flash Memory, Data Flash Memory):RX66T	✦	
Package	✓	

✓: Available, ×: Not available, ✦: There are differences in the function between RX24T and RX66T

2. Comparison of Specifications Overview

This section describes comparison of specifications overview including registers.

For comparison of specifications overview, red text indicates functions which are included only in either of the MCU Groups and also indicates differences in specifications for functions which are included in both Groups.

For comparison of registers, red text indicates differences in specifications for registers which are included in both Groups and **black text** indicates registers which are included only in either of the MCU Groups.

2.1 CPU

Table 2.1 lists Comparison of CPU Specifications.

Table 2.1 Comparison of CPU Specifications

Item	RX24T	RX66T
CPU	• Maximum operating frequency: 80 MHz • 32-bit RX CPU (RX v2) • Minimum instruction execution time: One instruction per clock cycle • Address space: 4-Gbyte linear • Register set - General purpose: Sixteen 32-bit registers - Control: Ten 32-bit registers - Accumulator: Two 72-bit registers • Basic instructions: 75 Variable-length instruction format • Floating-point instructions: 11 • DSP instructions: 23 • Addressing modes: 11 • Data arrangement - Instructions: Little endian - Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32-bit × 32-bit → 64-bit • On-chip divider: 32-bit ÷ 32-bit → 32-bit • Barrel shifter: 32 bits • Memory-protection unit (MPU) • ROM cache: 2 Kbytes (disabled by default)	• Maximum operating frequency: 160MHz • 32-bit RX CPU (RXv3) • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4-Gbyte linear • Register set of the CPU - General purpose: Sixteen 32-bit registers - Control: Ten 32-bit registers - Accumulator: Two 72-bit registers • Basic instructions: 77 • Single precision floating point instructions: 11 • DSP instructions: 23 • Addressing modes: 11 • Data arrangement - Instructions: Little endian - Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32/32 → 32 bits • Barrel shifter: 32 bits • Memory-protection unit (MPU) • ROM Cache: 8 KB
FPU	• Single precision (32-bit) floating point • Data types and floating-point exceptions in conformance with the IEEE754 standard	• Single-precision (32-bit) floating-point number • Data types and floating-point exceptions in conformance with the IEEE754 standard

2.2 Operating Modes

Table 2.2 lists Comparison of Specifications for Operating Modes and Table 2.3 lists Comparison of Registers for Operating Modes.

Table 2.2 Comparison of Specifications for Operating Modes

Item	RX24T	RX66T
Operating modes by the mode-setting pins	Single-chip mode	Single-chip mode
	Boot mode (SCI)	Boot mode (for the SCI interface)
	—	Boot mode (for the USB interface)
	—	Boot mode (for the FINE interface)
	—	User boot mode
Operating mode by register setting	—	Single-chip mode
		User boot mode
		On-chip ROM disabled extended mode
		On-chip ROM enabled extended mode
Selection of endian	MDE (Endian Select Register)	MDE (Endian Select Register)

Table 2.3 Comparison of Registers for Operating Modes

Register	Bit	RX24T	RX66T
MDSR	—	—	Mode Status Register
SYSCR0	—	—	System Control Register 0
SYSCR1	ECCRAME	—	ECCRAM Enable
VOLSR	—	—	Voltage level setting register

2.3 Resets

Table 2.4 lists Comparison of Specifications for Resets and Table 2.5 lists Comparison of Registers for Resets.

Table 2.4 Comparison of Specifications for Resets

Item	RX24T	RX66T
RES# pin reset	Voltage input to the RES# pin is driven low.	Voltage input to the RES# pin is driven low.
Power-on reset	VCC rises (voltage monitored: VPOR)	VCC rises (voltage detection: VPOR)
Voltage-monitoring 0 reset	VCC falls (voltage monitored: Vdet0)	VCC falls (voltage detection: Vdet0)
Voltage-monitoring 1 reset	VCC falls (voltage monitored: Vdet1)	VCC falls (voltage detection: Vdet1)
Voltage-monitoring 2 reset	VCC falls (voltage monitored: Vdet2)	VCC falls (voltage detection: Vdet2)
Deep software standby reset	—	Deep software standby mode is canceled by an interrupt.
Independent watchdog timer reset	The independent watchdog timer underflows, or a refresh error occurs.	The independent watchdog timer underflows, or a refresh error occurs.
Watchdog timer reset	—	The watchdog timer underflows, or a refresh error occurs.
Software reset	Register setting	Register setting

Table 2.5 Comparison of Registers for Resets

Register	Bit	RX24T	RX66T
RSTSR0	DPSRSTF	—	Deep Software Standby Reset Flag
RSTSR2	WDTRF	—	Watchdog Timer Reset Detect Flag

2.4 Option-Setting Memory

Table 2.6 lists Comparison of Registers for Option-Setting Memory.

Table 2.6 Comparison of Registers for Option-Setting Memory

Register	Bit	RX24T	RX66T(OFSM)
SPCC	—	—	Serial Programmer Command Control Register
OSIS	—	—	OCD/Serial Programmer ID Setting Register
OFS0	IWDTTOPS [1:0]	IWDT Timeout Period Select b3 b2 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1024 cycles (03FFh) 1 1: 2048 cycles (07FFh)	IWDT Timeout Period Select b3 b2 0 0: 1024 cycles (03FFh) 0 1: 4096 cycles (0FFFh) 1 0: 8192 cycles (1FFFh) 1 1: 16384 cycles (3FFFh)
	IWDTRSTIRQS	IWDT Reset Interrupt Request Select 0: Non-maskable interrupt request is enabled 1: Reset is enabled	IWDT Reset Interrupt Request Select 0: Non-maskable interrupt request or plain interrupt request is enabled 1: Reset is enabled
	IWDTSLCSTP	IWDT Sleep Mode Count Stop Control 0: Counting stop is disabled 1: Counting stop is enabled when entering sleep, software standby, or deep sleep mode	IWDT Sleep Mode Count Stop Control 0: Counting stop is disabled 1: Counting stop is enabled when entering sleep, software standby, deep software standby, or all-module clock stop mode
	WDTSTRT	—	WDT Start Mode Select
	WDTTOPS[1:0]	—	WDT Timeout Period Select
	WDTCKS[3:0]	—	WDT Clock Frequency Division Ratio Select
	WDTRPES[1:0]	—	WDT Window End Position Select
	WDTRPSS[1:0]	—	WDT Window Start Position Select
	WDTRSTIRQS	—	WDT Reset Interrupt Request Select
OFS1	VDSEL[1:0]	Voltage Detection 0 Level Select b1 b0 0 0: 3.84 V is selected 0 1: 2.82 V is selected 1 0: 2.51 V is selected Settings other than above are prohibited when the voltage detection 0 circuit is used.	Voltage Detection 0 Level Select b1 b0 0 0: Reserved 0 1: Reserved 1 0: Selects 2.83 V 1 1: Selects 4.22 V
TMEF	—	—	TM Enable Flag Register
TMINF	—	—	TM Identification Data Register
ROMCODE	—	—	ROM Code Protection Register

2.5 Voltage Detection Circuit

Table 2.7 lists Comparison of Specifications for Voltage Detection Circuit and Table 2.8 lists Comparison of Registers for Voltage Detection Circuit.

Also, Table 2.9 lists Comparison of Procedures for Setting up Monitoring against Vdet1, Table 2.10 lists Comparison of Procedures for Setting up Monitoring against Vdet2, Table 2.11 lists Comparison of Procedures for Setting Bits Related to the Voltage Monitoring 1 Interrupt and Voltage Monitoring 1 Reset so that Voltage Monitoring Operates and Table 2.12 lists Comparison of Procedures for Setting Bits Related to the Voltage Monitoring 2 Interrupt and Voltage Monitoring 2 Reset so that Voltage Monitoring Operates.

Table 2.7 Comparison of Specifications for Voltage Detection Circuit

Item		RX24T(LVDAb)			RX66T(LVDA)		
		Voltage Monitoring 0	Voltage Monitoring 1	Voltage Monitoring 2	Voltage Monitoring 0	Voltage Monitoring 1	Voltage Monitoring 2
VCC monitoring	Monitored voltage	Vdet0	Vdet1	Vdet2	Vdet0	Vdet1	Vdet2
	Detected event	Voltage drops past Vdet0	When voltage rises above or drops below Vdet1	When voltage rises above or drops below Vdet2	Voltage drops past Vdet0	Voltage rises or drops past Vdet1	Voltage rises or drops past Vdet2
	Detection voltage	Voltage selectable from 3 levels using OFS1	Voltage selectable from 9 levels using the LVDLVLR.LVD1LVL[3:0] bits	Voltage selectable from 4 levels using the LVDLVLR.LVD2LVL[1:0] bits	Selectable from among two different levels by using OFS1.VDSEL[1:0] bits	Selectable from among five different levels by using LVDLVLR.LVD1LVL[3:0] bits	Selectable from among five different levels by using LVDLVLR.LVD2LVL[3:0] bits
	Monitoring flag	Not available	LVD1SR.LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR.LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2	None	LVD1SR.LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR.LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2
			LVD1SR.LVD1DET flag: Vdet1 passage detection	LVD2SR.LVD2DET flag: Vdet2 passage detection		LVD1SR.LVD1DET flag: Vdet1 passage detection	LVD2SR.LVD2DET flag: Vdet2 passage detection

Item		RX24T(LVDAb)			RX66T(LVDA)		
		Voltage Monitoring 0	Voltage Monitoring 1	Voltage Monitoring 2	Voltage Monitoring 0	Voltage Monitoring 1	Voltage Monitoring 2
Process upon voltage detection	Reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset
		Reset when Vdet0 > VCC: CPU restart after specified time with VCC > Vdet0	Reset when Vdet1 > VCC: CPU restart timing selectable: after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC: CPU restart timing selectable: after specified time with VCC > Vdet2 or after specified time with Vdet2 > VCC	Reset when Vdet0 > VCC: CPU restart after specified time with VCC > Vdet0	Reset when Vdet1 > VCC: CPU restart timing selectable: after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC: CPU restart timing selectable: after specified time with VCC > Vdet2 or Vdet2 > VCC
	Interrupt	Not available	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt	No interrupt	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt
			Non-maskable or maskable interrupt is selectable	Non-maskable or maskable interrupt is selectable		Non-maskable interrupt or maskable interrupt selectable	Non-maskable interrupt or maskable interrupt selectable
			Interrupt request issued when Vdet1 > VCC and VCC > Vdet1 or either	Interrupt request issued when Vdet2 > VCC and VCC > Vdet2 or either		Interrupt request issued when Vdet1 > VCC and VCC > Vdet1 or either	Interrupt request issued when Vdet2 > VCC and VCC > Vdet2 or either
Digital filter	Enable/ Disable switching	—	—	—	Digital filter function not available	Available	Available
	Sampling time	—	—	—	—	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)
Event linking		—	—	—	None	Available Output of event signals on detection of Vdet crossings	Available Output of event signals on detection of Vdet crossings

Table 2.8 Comparison of Registers for Voltage Detection Circuit

Register	Bit	RX24T(LVDAb)	RX66T(LVDA)
LVDLVLR	LVD1LVL[3:0]	Voltage Detection 1 Level Select (Standard voltage during drop in voltage) b3 b0 0 0 0 0: 4.29V 0 0 0 1: 4.14V 0 0 1 0: 4.02V 0 0 1 1: 3.84V 0 1 0 0: 3.10V 0 1 0 1: 3.00V 0 1 1 0: 2.90V 0 1 1 1: 2.79V 1 0 0 0: 2.68V Settings other than those listed above are prohibited.	Voltage Detection 1 Level Select (Standard voltage during drop in voltage) b3 b0 0 1 0 0: 4.57 V (Vdet1_0) 0 1 0 1: 4.47 V (Vdet1_1) 0 1 1 0: 4.32 V (Vdet1_2) 1 0 1 0: 2.93 V (Vdet1_3) 1 0 1 1: 2.88 V (Vdet1_4) Settings other than above are prohibited.
	LVD2LVL[1:0] (RX24T) LVD2LVL[3:0] (RX66T)	Voltage Detection 2 Level Select (Standard voltage during drop in voltage) b5 b4 0 0: 4.29V 0 1: 4.14V 1 0: 4.02V 1 1: 3.84V	Voltage Detection 2 Level Select (Standard voltage during drop in voltage) b7 b4 0 1 0 0: 4.57 V (Vdet2_0) 0 1 0 1: 4.47 V (Vdet2_1) 0 1 1 0: 4.32 V (Vdet2_2) 1 0 1 0: 2.93 V (Vdet2_3) 1 0 1 1: 2.88 V (Vdet2_4) Settings other than above are prohibited.
LVD1CR0	LVD1DFDIS	—	Voltage Monitoring 1 Digital Filter Disable Mode Select
	LVD1FSAMP [1:0]	—	Sampling Clock Select
LVD2CR0	LVD2DFDIS	—	Voltage Monitoring 2 Digital Filter Disable Mode Select
	LVD2FSAMP [1:0]	—	Sampling Clock Select

Table 2.9 Comparison of Procedures for Setting up Monitoring against Vdet1

Item		RX24T(LVDAb)	RX66T(LVDA)
Procedures for Setting up Monitoring against Vdet1	1	Specify the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits (voltage detection 1 level select).	Select the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits.
	2	Set the LVCMPCR.LVD1E bit to 1 (voltage detection 1 circuit enabled).	Set LVCMPCR.LVD1E = 1 (enabling the voltage detection 1 circuit).
	3	Wait for Td(E-A)	Wait for at least td(E-A) (LVD operation stabilization time after LVD is enabled).
	4	— (No procedure because there is no digital filter)	• When the Digital Filter is in Use Select the sampling clock for the digital filter by setting the LVD1CR0.LVD1FSAMP[1:0] bits. • When the Digital Filter is Not in Use — (No procedure)
	5	— (No procedure because there is no digital filter)	• When the Digital Filter is in Use Set LVD1CR0.LVD1DFDIS = 0 (enabling the digital filter). • When the Digital Filter is Not in Use — (No procedure)
	6	— (No procedure because there is no digital filter)	• When the Digital Filter is in Use Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n). • When the Digital Filter is Not in Use — (No procedure)
	7	Set the LVD1CR0.LVD1CMPE bit to 1 (voltage monitoring 1 circuit comparison results output enabled).	Set LVD1CR0.LVD1CMPE = 1 (enabling output of the results of comparison by voltage monitoring 1).

Table 2.10 Comparison of Procedures for Setting up Monitoring against Vdet2

Item		RX24T(LVDAb)	RX66T(LVDA)
Procedures for Setting up Monitoring against Vdet2	1	Specify the detection voltage by setting the LVDLVLR.LVD2LVL[1:0] bits (voltage detection 2 level select).	Select the detection voltage by setting the LVDLVLR.LVD2LVL[3:0] bits.
	2	Set the LVCMPCR.LVD2E bit to 1 (voltage detection 2 circuit enabled).	Set LVCMPCR.LVD2E = 1 (enabling the voltage detection 2 circuit).
	3	Wait for Td(E-A)	Wait for at least td(E-A) (LVD operation stabilization time after LVD is enabled).
	4	— (No procedure because there is no digital filter)	• When the Digital Filter is in Use Select the sampling clock for the digital filter by setting the LVD2CR0.LVD2FSAMP[1:0] bits. • When the Digital Filter is Not in Use — (No procedure)
	5	— (No procedure because there is no digital filter)	• When the Digital Filter is in Use Set LVD2CR0.LVD2DFDIS = 0 (enabling the digital filter). • When the Digital Filter is Not in Use — (No procedure)
	6	— (No procedure because there is no digital filter)	• When the Digital Filter is in Use Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n). • When the Digital Filter is Not in Use — (No procedure)
	7	Set the LVD2CR0.LVD2CMPE bit to 1 (voltage monitoring 2 circuit comparison results output enabled).	Set LVD2CR0.LVD2CMPE = 1 (enabling output of the results of comparison by voltage monitoring 2).

Table 2.11 Comparison of Procedures for Setting Bits Related to the Voltage Monitoring 1 Interrupt and Voltage Monitoring 1 Reset so that Voltage Monitoring Operates

Item		RX24T(LVDAb)	RX66T(LVDA)
Procedures for Setting Bits Related to the Voltage Monitoring 1 Interrupt so that Voltage Monitoring Operates	1	Select the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits.	Select the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits.
	2	Set the LVD1CR0.LVD1RI bit to 0 (voltage monitoring 1 interrupt).	Set LVCMPCR.LVD1E = 1 (enabling the voltage detection 1 circuit).
	3	Select the timing of interrupt requests by setting the LVD1CR1.LVD1IDTSEL[1:0] bits. Select the type of interrupt by setting the LVD1CR1.LVD1IRQSEL bit.	Wait for at least td(E-A) (LVD operation stabilization time after LVD is enabled).
	4	— (No procedure because there is no digital filter)	• When the Digital Filter is in Use Select the sampling clock for the digital filter by setting the LVD1CR0.LVD1FSAMP[1:0] bits. • When the Digital Filter is Not in Use — (No procedure)
	5	— (No procedure because there is no digital filter)	• When the Digital Filter is in Use Set LVD1CR0.LVD1DFDIS = 0 (enabling the digital filter). • When the Digital Filter is Not in Use — (No procedure)
	6	— (No procedure because there is no digital filter)	• When the Digital Filter is in Use Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n). • When the Digital Filter is Not in Use — (No procedure)
	7	Set the LVCMPCR.LVD1E bit to 1 (voltage detection 1 circuit enabled).	Set LVD1CR0.LVD1RI = 0 (selecting the voltage monitoring 1 interrupt).
	8	Wait for at least Td(E-A).	• Select the timing of interrupt requests by setting the LVD1CR1.LVD1IDTSEL[1:0] bits. • Select the type of interrupt by setting the LVD1CR1.LVD1IRQSEL bit.
	9	Set the LVD1CR0.LVD1CMPE bit to 1 (voltage monitoring 1 circuit comparison results output enabled).	Set LVD1SR.LVD1DET = 0.
	10	Wait for at least 2 µs.	—
	11	Set the LVD1SR.LVD1DET bit to 0.	Set LVD1CR0.LVD1RIE = 1 (enabling the voltage monitoring 1 interrupt or reset).
	12	Set the LVD1CR0.LVD1RIE bit to 1 (voltage monitoring 1 interrupt/reset enabled).	Set LVD1CR0.LVD1CMPE = 1 (enabling output of the results of comparison by voltage monitoring 1).

Item		RX24T(LVDAb)	RX66T(LVDA)
Procedures for Setting Bits Related to the Voltage Monitor 1 Reset so that Voltage Monitoring Operates	1	Select the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits.	Select the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits.
	2	• Set the LVD1CR0.LVD1RI bit to 1 (voltage monitoring 1 reset). • Select the type of reset negation by setting the LVD1CR0.LVD1RN bit.	Set LVCMPCR.LVD1E = 1 (enabling the voltage detection 1 circuit).
	3	Set the LVD1CR0.LVD1RIE bit to 1 (voltage monitoring 1 interrupt/reset enabled).	Wait for at least td(E-A) (LVD operation stabilization time after LVD is enabled).
	4	— (No procedure because there is no digital filter)	• When the Digital Filter is in Use Select the sampling clock for the digital filter by setting the LVD1CR0.LVD1FSAMP[1:0] bits. • When the Digital Filter is Not in Use — (No procedure)
	5	— (No procedure because there is no digital filter)	• When the Digital Filter is in Use Set LVD1CR0.LVD1DFDIS = 0 (enabling the digital filter). • When the Digital Filter is Not in Use — (No procedure)
	6	— (No procedure because there is no digital filter)	• When the Digital Filter is in Use Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n). • When the Digital Filter is Not in Use — (No procedure)
	7	—	• Set LVD1CR0.LVD1RI = 1 (selecting the voltage monitoring 1 reset). • Select the type of the reset negation by setting the LVD1CR0.LVD1RN bit.
	8	Set the LVCMPCR.LVD1E bit to 1 (voltage detection 1 circuit enabled).	Set LVD1SR.LVD1DET = 0.
	9	Wait for at least Td(E-A).	Set LVD1CR0.LVD1RIE = 1 (enabling the voltage monitoring 1 interrupt or reset).
	10	Set the LVD1CR0.LVD1CMPE bit to 1 (voltage monitoring 1 circuit comparison results output enabled).	Set LVD1CR0.LVD1CMPE = 1 (enabling output of the results of comparison by voltage monitoring 1).

Item		RX24T(LVDAb)	RX66T(LVDA)
Procedures for Setting Bits Related to the Voltage Monitoring 1 Interrupt so that Voltage Monitoring Stops	1	Set the LVD1CR0.LVD1RIE bit to 0 (voltage monitoring 1 interrupt/reset disabled).	Set LVD1CR0.LVD1CMPE = 0 (disabling output of the results of comparison by voltage monitoring 1).
	2	— (No procedure because there is no digital filter)	• When the Digital Filter is in Use Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n). • When the Digital Filter is Not in Use — (No procedure)
	3	Set the LVD1CR0.LVD1CMPE bit to 0 (voltage monitoring 1 circuit comparison results output disabled).	Set LVD1CR0.LVD1RIE = 0 (disabling the voltage monitoring 1 interrupt or reset).
	4	— (No procedure because there is no digital filter)	• When the Digital Filter is in Use Set LVD1CR0.LVD1DFDIS = 1 (disabling the digital filter). • When the Digital Filter is Not in Use — (No procedure)
	5	Set the LVCMPCR.LVD1E bit to 0 (voltage detection 1 circuit disabled).	Set LVCMPCR.LVD1E = 0 (disabling the voltage detection 1 circuit).
	6	Modify settings of bits related to the voltage detection circuit registers other than LVCMPCR.LVD1E, LVD1CR0.LVD1RIE, and LVD1CR0.LVD1CMPE.	—

Item		RX24T(LVDAb)	RX66T(LVDA)
Procedures for Setting Bits Related to the Voltage Monitoring 1 Reset so that Voltage Monitoring Stops	1	Set the LVD1CR0.LVD1CMPE bit to 0 (voltage monitoring 1 circuit comparison results output disabled).	Set LVD1CR0.LVD1CMPE = 0 (disabling output of the results of comparison by voltage monitoring 1).
	2	— (No procedure because there is no digital filter)	• When the Digital Filter is in Use Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n). • When the Digital Filter is Not in Use — (No procedure)
	3	Set the LVCMPCR.LVD1E bit to 0 (voltage detection 1 circuit disabled).	Set LVD1CR0.LVD1RIE = 0 (disabling the voltage monitoring 1 interrupt or reset).
	4	— (No procedure because there is no digital filter)	• When the Digital Filter is in Use Set LVD1CR0.LVD1DFDIS = 1 (disabling the digital filter). • When the Digital Filter is Not in Use — (No procedure)
	5	Set the LVD1CR0.LVD1RIE bit to 0 (voltage monitoring 1 interrupt/reset disabled).	Set LVCMPCR.LVD1E = 0 (disabling the voltage detection 1 circuit).
	6	Modify settings of bits related to the voltage detection circuit registers other than LVCMPCR.LVD1E, LVD1CR0.LVD1RIE, and LVD1CR0.LVD1CMPE.	—

Table 2.12 Comparison of Procedures for Setting Bits Related to the Voltage Monitoring 2 Interrupt and Voltage Monitoring 2 Reset so that Voltage Monitoring Operates

Item		RX24T(LVDAb)	RX66T(LVDA)
Procedures for Setting Bits Related to the Voltage Monitoring 2 Interrupt so that Voltage Monitoring Operates	1	Select the detection voltage by setting the LVDLVLR.LVD2LVL[1:0] bits.	Select the detection voltage by setting the LVDLVLR.LVD2LVL[3:0] bits.
	2	Set the LVD2CR0.LVD2RI bit to 0 (voltage monitoring 2 interrupt).	Set LVCMPCR.LVD2E = 1 (enabling the voltage detection 2 circuit).
	3	• Select the timing of interrupt requests by setting the LVD2CR1.LVD2IDTSEL[1:0] bits. • Select the type of interrupt by setting the LVD2CR1.LVD2IRQSEL bit.	Wait for at least td(E-A) (LVD operation stabilization time after LVD is enabled).
	4	— (No procedure because there is no digital filter)	• When the Digital Filter is in Use Select the sampling clock for the digital filter by setting the LVD2CR0.LVD2FSAMP[1:0] bits. • When the Digital Filter is Not in Use — (No procedure)
	5	— (No procedure because there is no digital filter)	• When the Digital Filter is in Use Set LVD2CR0.LVD2DFDIS = 0 (enabling the digital filter). • When the Digital Filter is Not in Use — (No procedure)
	6	— (No procedure because there is no digital filter)	• When the Digital Filter is in Use Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n). • When the Digital Filter is Not in Use — (No procedure)
	7	Set the LVCMPCR.LVD2E bit to 1 (voltage detection 2 circuit enabled).	Set LVD2CR0.LVD2RI = 0 (selecting the voltage monitoring 2 interrupt).
	8	Wait for at least Td(E-A).	• Select the timing of interrupt requests by setting the LVD2CR1.LVD2IDTSEL[1:0] bits. • Select the type of interrupt by setting the LVD2CR1.LVD2IRQSEL bit.
	9	Set the LVD2CR0.LVD2CMPE bit to 1 (voltage monitoring 2 circuit comparison results output enabled).	Set LVD2SR.LVD2DET = 0.
	10	Wait for at least 2 µs.	—
	11	Set the LVD2SR.LVD2DET bit to 0.	Set LVD2CR0.LVD2RIE = 1 (enabling the voltage monitoring 2 interrupt or reset).
	12	Set the LVD2CR0.LVD2RIE bit to 1 (voltage monitoring 2 interrupt/reset enabled)	Set LVD2CR0.LVD2CMPE = 1 (enabling output of the results of comparison by voltage monitoring 2).

Item		RX24T(LVDAb)	RX66T(LVDA)
Procedures for Setting Bits Related to the Voltage Monitor 2 Reset so that Voltage Monitoring Operates	1	Select the detection voltage by setting the LVDLVLR.LVD2LVL[1:0] bits.	Select the detection voltage by setting the LVDLVLR.LVD2LVL[3:0] bits.
	2	• Set the LVD2CR0.LVD2RI bit to 1 (voltage monitoring 2 reset). • Select the type of reset negation by setting the LVD2CR0.LVD2RN bit.	Set LVCMPCR.LVD2E = 1 (enabling the voltage detection 2 circuit).
	3	Set the LVD2CR0.LVD2RIE bit to 1 (voltage monitoring 2 interrupt/reset enabled).	Wait for at least td(E-A) (LVD operation stabilization time after LVD is enabled).
	4	— (No procedure because there is no digital filter)	• When the Digital Filter is in Use Select the sampling clock for the digital filter by setting the LVD2CR0.LVD2FSAMP[1:0] bits. • When the Digital Filter is Not in Use — (No procedure)
	5	— (No procedure because there is no digital filter)	• When the Digital Filter is in Use Set LVD2CR0.LVD2DFDIS = 0 (enabling the digital filter). • When the Digital Filter is Not in Use — (No procedure)
	6	— (No procedure because there is no digital filter)	• When the Digital Filter is in Use Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n). • When the Digital Filter is Not in Use — (No procedure)
	7	—	• Set LVD2CR0.LVD2RI = 1 (selecting the voltage monitoring 2 reset). • Select the type of the reset negation by setting the LVD2CR0.LVD2RN bit.
	8	Set the LVCMPCR.LVD2E bit to 1 (voltage detection 2 circuit enabled).	Set LVD2SR.LVD2DET = 0.
	9	Wait for at least Td(E-A).	Set LVD2CR0.LVD2RIE = 1 (enabling the voltage monitoring 2 interrupt or reset).
	10	Set the LVD2CR0.LVD2CMPE bit to 1 (voltage monitoring 2 circuit comparison results output enabled).	Set LVD2CR0.LVD2CMPE = 1 (enabling output of the results of comparison by voltage monitoring 2).

Item		RX24T(LVDAb)	RX66T(LVDA)
Procedures for Setting Bits Related to the Voltage Monitoring 2 Interrupt so that Voltage Monitoring Stops	1	Set the LVD2CR0.LVD2RIE bit to 0 (voltage monitoring 2 interrupt/reset disabled).	Set LVD2CR0.LVD2CMPE = 0 (disabling output of the results of comparison by voltage monitoring 2).
	2	— (No procedure because there is no digital filter)	• When the Digital Filter is in Use Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n). • When the Digital Filter is Not in Use — (No procedure)
	3	Set the LVD2CR0.LVD2CMPE bit to 0 (voltage monitoring 2 circuit comparison results output disabled).	Set LVD2CR0.LVD2RIE = 0 (disabling the voltage monitoring 2 interrupt or reset).
	4	— (No procedure because there is no digital filter)	• When the Digital Filter is in Use Set LVD2CR0.LVD2DFDIS = 1 (disabling the digital filter). • When the Digital Filter is Not in Use — (No procedure)
	5	Set the LVCMPCR.LVD2E bit to 0 (voltage monitoring 2 circuit disabled).	Set LVCMPCR.LVD2E = 0 (disabling the voltage detection 2 circuit).
	6	Modify settings of bits related to the voltage detection circuit registers other than LVCMPCR.LVD2E, LVD2CR0.LVD2RIE, and LVD2CR0.LVD2CMPE.	—

Item		RX24T(LVDAb)	RX66T(LVDA)
Procedures for Setting Bits Related to the Voltage Monitoring 2 Reset so that Voltage Monitoring Stops	1	Set the LVD2CR0.LVD2CMPE bit to 0 (voltage monitoring 2 circuit comparison results output disabled).	Set LVD2CR0.LVD2CMPE = 0 (disabling output of the results of comparison by voltage monitoring 2).
	2	— (No procedure because there is no digital filter)	• When the Digital Filter is in Use Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n). • When the Digital Filter is Not in Use — (No procedure)
	3	Set the LVCMPCR.LVD2E bit to 0 (voltage monitoring 2 circuit disabled).	Set LVD2CR0.LVD2RIE = 0 (disabling the voltage monitoring 2 interrupt or reset).
	4	— (No procedure because there is no digital filter)	• When the Digital Filter is in Use Set LVD2CR0.LVD2DFDIS = 1 (disabling the digital filter). • When the Digital Filter is Not in Use — (No procedure)
	5	Set the LVD2CR0.LVD2RIE bit to 0 (voltage monitoring 2 interrupt/reset disabled).	Set LVCMPCR.LVD2E = 0 (disabling the voltage detection 2 circuit).
	6	Modify settings of bits related to the voltage detection circuit registers other than LVCMPCR.LVD2E, LVD2CR0.LVD2RIE, and LVD2CR0.LVD2CMPE.	—

2.6 Clock Generation Circuit

Table 2.13 lists Comparison of Specifications for Clock Generation Circuit and Table 2.14 lists Comparison of Registers for Clock Generation Circuit.

Table 2.13 Comparison of Specifications for Clock Generation Circuit

Item	RX24T	RX66T
Use	• Generates the system clock (ICLK) to be supplied to the CPU, DTC, ROM, and RAM. • Generates the peripheral module clocks (PCLKA, PCLKB, and PCLKD) to be supplied to peripheral modules. The peripheral module clock PCLKA is the operating clock for the MTU and GPT, the peripheral module clock PCLKD is for the S12AD, and PCLKB is for other modules. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the CAN clock (CANMCLK) to be supplied to the RSCAN • Generates the IWDT-dedicated low-speed clock (IWDTCLK) to be supplied to the IWDT.	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the RSPI, SCIi, MTU3 (internal peripheral buses), GPTW (internal peripheral buses), and HRPWM (internal peripheral buses). • Generates the peripheral module clock (PCLKB) to be supplied to peripheral modules. • Generates the counter reference clock for the peripheral module to be supplied to the MTU3 and GPTW and the reference clock (PCLKC) for the HRPWM. • Generates the peripheral module clocks (for analog conversion) (PCLKD) to be supplied to S12AD. • Generates the flash-IF clock (FCLK) to be supplied to the flash interface. • Generates the external bus clock (BCLK) to be supplied to the external bus. • Generates the USB clock (UCLK) to be supplied to the USBb. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the CAN clock (CANMCLK) to be supplied to the CAN. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT.
Operating frequency	• ICLK: 80 MHz (max) • PCLKA: 80 MHz (max) • PCLKB: 40 MHz (max) • PCLKD: 40 MHz (max) • FCLK: - 1 to 32 MHz(ROM)	• ICLK: 160 MHz (max) • PCLKA: 120 MHz (max) • PCLKB: 60 MHz (max) • PCLKC: 160 MHz (max) • PCLKD: 8 MHz to 60 MHz (for conversion with 12-bit A/D converter) • FCLK: - 4 MHz to 60 MHz (for programming and erasing the code flash memory and data flash memory) - 60 MHz (max) (for reading from the data flash memory) • BCLK: 60 MHz (max) • BCLK pin output: 40 MHz (max) • UCLK: 48 MHz (max)

Item	RX24T	RX66T
Operating frequency	• CACCLK: Same frequency as each oscillator • CANMCLK: 20 MHz (max) • IWDTCLK: 15 kHz	• CACCLK: Same as the clock from respective oscillators. • CANMCLK: 24 MHz (max) • IWDTCLK: 120 kHz
Main clock oscillator	• Resonator frequency: 1 to 20 MHz • External clock input frequency: 20 MHz (max) • Connectable resonator or additional circuit: ceramic resonator, crystal • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When main clock oscillation stop is detected, the system clock source switches to LOCO, MTU and GPT pin output stops, and a non-maskable interrupt is generated. • Drive capacity switching function	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 24 MHz (max) • Connectable resonator or additional circuit: ceramic resonator, crystal resonator • Connection pin: EXTAL, XTAL • Oscillation stop detection function: When main clock oscillation stop is detected, the system clock source switches to LOCO, MTU3 and GPTW output is driven high-impedance, and a maskable or non-maskable interrupt (selectable) is generated. • Drive capacity switching function
PLL frequency synthesizer	• Input clock source: Main clock and HOCO (32 MHz) clock divided by 4 • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 to 12.5 MHz • Frequency multiplication ratio: Selectable from 4 to 15.5 (increments of 0.5) • VCO oscillation frequency: 40 to 80 MHz	• Input clock source: Main clock, HOCO • Input pulse frequency division ratio: Selectable from 1, 2, and 3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication ratio: Selectable from 10 to 30 (increments of 0.5) • Output clock frequency of the PLL frequency synthesizer: 120 MHz to 240 MHz
High-speed on-chip oscillator (HOCO)	Oscillation frequency: 32 and 64 MHz	• Oscillation frequency: Selectable from 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 4 MHz	Oscillation frequency: 240 kHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 15 kHz	Oscillation frequency: 120 kHz
Control of output on the BCLK pin	—	• BCLK clock output or high output is selectable • BCLK or BCLK/2 is selectable
Event linking (output)	—	Detection of stopping of the main clock oscillator
Event linking (input)	—	Switching of the clock source to the low-speed on-chip oscillator

Table 2.14 Comparison of Registers for Clock Generation Circuit

Register	Bit	RX24T	RX66T
SCKCR (Note 1)	PCKC[3:0]	—	Peripheral Module Clock C (PCLKC) Select
	BCK[3:0]	—	External Bus Clock (BCLK) Select
	PSTOP1	—	BCLK Pin Output Control
PLLCR	PLIDIV[1:0]	PLL Input Frequency Division Ratio Select b1 b0 0 0: ×1 0 1: ×1/2 1 0: ×1/4 1 1: Setting prohibited	PLL Input Frequency Division Ratio Select b1 b0 0 0: ×1 0 1: ×1/2 1 0: ×1/3 1 1: Setting prohibited
	PLLSRCSEL	PLL Clock Source Selection (b2)	PLL Clock Source Select (b4)
	STC[5:0]	Frequency Multiplication Factor Select b13 b8 0 0 0 1 1 1: ×4 0 0 1 0 0 0: ×4.5 0 0 1 0 0 1: ×5 0 0 1 0 1 0: ×5.5 0 0 1 0 1 1: ×6 0 0 1 1 0 0: ×6.5 . . . 0 1 1 1 0 0: ×14.5 0 1 1 1 0 1: ×15 0 1 1 1 1 0: ×15.5 Settings other than above are prohibited.	Frequency Multiplication Factor Select b13 b8 0 1 0 0 1 1: ×10.0 0 1 0 1 0 0: ×10.5 0 1 0 1 0 1: ×11.0 0 1 0 1 1 0: ×11.5 0 1 0 1 1 1: ×12.0 0 1 1 0 0 0: ×12.5 . . . 1 1 1 0 0 1: ×29.0 1 1 1 0 1 0: ×29.5 1 1 1 0 1 1: ×30.0 Settings other than above are prohibited.
		Initial values after a reset are different.	
BCKCR	—	—	External Bus Clock Control Register
HOCOCR2	HCFRQ[1:0]	HOCO Frequency Setting b1 b0 0 0: 32 MHz 1 1: 64 MHz Settings other than above are prohibited.	HOCO Frequency Setting b1 b0 0 0: 16 MHz 0 1: 18 MHz 1 0: 20 MHz Settings other than above are prohibited.
HOCOWTCR	—	High-Speed On-Chip Oscillator Wait Control Register	—
OSCOVFSR	ILCOVF	—	IWDT-Dedicated Clock Oscillation Stabilization Flag

Register	Bit	RX24T	RX66T
MOSCWTCR	MSTS[4:0] (RX24T) MSTS[7:0] (RX66T)	Main Clock Oscillator Wait Time b4 b0 0 0 0 0 0: Wait time = 2 cycles (0.5 µs) 0 0 0 0 1: Wait time = 1024 cycles (256 µs) 0 0 0 1 0: Wait time = 2048 cycles (512 µs) 0 0 0 1 1: Wait time = 4096 cycles (1.024 ms) 0 0 1 0 0: Wait time = 8192 cycles (2.048 ms) 0 0 1 0 1: Wait time = 16384 cycles (4.096 ms) 0 0 1 1 0: Wait time = 32768 cycles (8.192 ms) 0 0 1 1 1: Wait time = 65536 cycles (16.384 ms) Settings other than above are prohibited. Wait time when LOCO = 4.0 MHz (0.25 µs, TYP.)	The waiting time until output of the signal from the main clock oscillator to the internal circuits starts. MSTS[7:0] > [tMAINOSC × (fLOCO_max) + 16] / 32 (tMAINOSC: main clock oscillation stabilization time; fLOCO_max: maximum frequency for fLOCO)
MOFCR	MODRV21 (RX24T) MODRV2 [1:0](RX66T)	Main Clock Oscillator Drive Capability Switch 0: 1 MHz or higher and lower than 10 MHz 1: 10 MHz to 20 MHz	Main Clock Oscillator Driving Ability 2 Switching b5 b4 0 0: 20.1 to 24 MHz 0 1: 16.1 to 20 MHz 1 0: 8.1 to 16 MHz 1 1: 8 MHz
MEMWAIT	MEMWAIT [1:0](RX24T) MEMWAIT (RX66T)	Memory Wait Cycle Setting b1 b0 0 0: No wait states 0 1: Wait states (ICLK ≤ 64 MHz) 1 0: Wait states (ICLK ≤ 80 MHz) Settings other than above are prohibited.	Memory Wait Cycle Setting 0: No wait 1: One wait cycle
SCKCR2	—	—	System Clock Control Register 2
HOCOPCR	—	—	High-Speed On-Chip Oscillator Power Supply Control Register

Note 1. Initial values after a reset are different.

2.7 Low Power Consumption

Table 2.15 lists Comparison of Specifications for Low Power Consumption and Table 2.16 lists Comparison of Registers for Low Power Consumption.

Table 2.15 Comparison of Specifications for Low Power Consumption

Item	RX24T	RX66T
Reducing power consumption by switching clock signals	The frequency division ratio can be set independently for the system clock (ICLK), high speed peripheral module clock (PCLKA), peripheral module clock (PCLKB), S12AD clock (PCLKD), and FlashIF clock (FCLK).	The frequency division ratio is settable independently for the system clock (ICLK), peripheral module clock (PCLKA, PCLKB, PCLKC, PCLKD), external bus clock (BCLK), and flash interface clock (FCLK).
BCLK output control function	—	• BCLK output or high-level output can be selected.
Module-stop function	Each peripheral module can be stopped independently by the module stop control register.	Functions can be stopped independently for each peripheral module.
Function for transition to low power consumption mode	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.
Low power consumption modes	• Sleep mode • — • Software standby mode • Deep sleep mode • —	• Sleep mode • All-module clock stop mode • Software standby mode • — • Deep software standby mode
Operating power control modes	• Power consumption can be reduced in normal operation, sleep mode, and deep sleep mode by selecting an appropriate operating power control mode according to the operating frequency and operating voltage. • Two operating power control modes are available High-speed operating mode Middle-speed operating mode	—

Table 2.16 Comparison of Registers for Low Power Consumption

Register	Bit	RX24T	RX66T
SBYCR	OPE	—	Output Port Enable
	SSBY	Software Standby 0: Set entry to sleep mode or deep sleep mode after the WAIT instruction is executed 1: Set entry to software standby mode after the WAIT instruction is executed	Software Standby 0: Shifts to sleep mode or all-module clock stop mode after the WAIT instruction is executed 1: Shifts to software standby mode after the WAIT instruction is executed
MSTPCRA	MSTPA7	General PWM Timer Module Stop	General PWM Timer/ High Resolution PWM/ GPTW-Dedicated Port Output Enable Module Stop
	MSTPA19	8-Bit D/A Converter Module Stop	12-bit D/A Converter Module Stop
	MSTPA24	—	Module Stop A24
	MSTPA27	—	Module Stop A27
	MSTPA28	Data Transfer Controller Module Stop	DMA Controller/Data Transfer Controller Module Stop
	MSTPA29	—	Module Stop A29
	ACSE	—	All-Module Clock Stop Mode Enable
MSTPCRB	MSTPB0	RSCAN Module Stop	CAN Module 0 Module Stop
	MSTPB4	—	Serial Communication Interface 12 Module Stop
	MSTPB9	—	Event Link Controller Module Stop
	MSTPB19	—	Universal Serial Bus 2.0 FS Interface Module Stop
MSTPCRC	MSTPC6	—	ECCRAM Module Stop
	MSTPC24	—	Serial Communications Interface 11 Module Stop
	MSTPC26	—	Serial Communications Interface 9 Module Stop
	MSTPC27	—	Serial Communications Interface 8 Module Stop
	DSLPE	Deep Sleep Mode Enable	—
MSTPCRD	—	—	Module Stop Control Register D
RSTCKCR	—	—	Sleep Mode Return Clock Source Switching Register
DPSBYCR	—	—	Deep Standby Control Register
DPSIER0	—	—	Deep Standby Interrupt Enable Register 0
DPSIER1	—	—	Deep Standby Interrupt Enable Register 1
DPSIER2	—	—	Deep Standby Interrupt Enable Register 2
DPSIFR0	—	—	Deep Standby Interrupt Flag Register 0
DPSIFR1	—	—	Deep Standby Interrupt Flag Register 1

Register	Bit	RX24T	RX66T
DPSIFR2	—	—	Deep Standby Interrupt Flag Register 2
DPSIEGR0	—	—	Deep Standby Interrupt Edge Register 0
DPSIEGR1	—	—	Deep Standby Interrupt Edge Register 1
DPSIEGR2	—	—	Deep Standby Interrupt Edge Register 2
DPSBKRy	—	—	Deep Standby Backup Register (y = 0 to 31)
OPCCR	—	Operating Power Control Register	—

2.8 Register Write Protection Function

Table 2.17 lists Comparison of Specifications for Register Write Protection Function and Table 2.18 lists Comparison of Registers for Register Write Protection Function.

Table 2.17 Comparison of Specifications for Register Write Protection Function

Item	RX24T	RX66T
PRC0	• Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, MOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOCOCR2, OSTDCR, OSTDSR, MEMWAIT	• Registers related to the clock generation circuit: SCKCR, SCKCR2, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOCOCR2, OSTDCR, OSTDSR
PRC1	• Register related to the operating modes: SYSCR1 • Registers related to low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, OPCCR • Registers related to the clock generation circuit: MOFCR, MOSCWTCR • Software reset register: SWRR	• Registers related to the operating modes: SYSCR0, SYSCR1, VOLSR • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, RSTCKCR, DPSBYCR, DPSIER0, DPSIER1, DPSIER2, DPSIFR0, DPSIFR1, DPSIFR2, DPSIEGR0, DPSIEGR1, DPSIEGR2 • Registers related to clock generation circuit: MOSCWTCR, MOFCR, HOCOPCR • Software reset register: SWRR
PRC2	• Register related to the clock generation circuit: HOCOWTCR	—
PRC3	• Registers related to the LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR	• Registers related to the LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

Table 2.18 Comparison of Registers for Register Write Protection Function

Register	Bit	RX24T	RX66T
PRCR	PRC2	Protect Bit 2	—

2.9 Interrupt Controller

Table 2.19 lists Comparison of Specifications for Interrupt Controller and Table 2.20 lists Comparison of Registers for Interrupt Controller.

Table 2.19 Comparison of Specifications for Interrupt Controller

Item		RX24T(ICUb)	RX66T(ICUC)
Interrupts	Peripheral interrupts	• Interrupts from peripheral modules • Number of sources: 163 • Interrupt detection: Edge detection/level detection Edge detection or level detection is fixed for each source of connected peripheral modules.	• Interrupts from peripheral modules • Number of sources: 256 • Interrupt detection method: Edge detection/level detection (fixed for each interrupt source) • Group interrupt: Multiple interrupt sources are grouped together and treated as an interrupt source. - Group BE0 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (edge detection) - Group BL0/BL1 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (level detection) - Group AL0 interrupt: Interrupt sources of peripheral modules that use PCLKA as the operating clock (level detection) • Software configurable interrupt A: Any of the interrupt sources for peripheral modules that use PCLKA as the operating clock can be assigned to interrupt vector numbers 208 to 255.
	External pin interrupt	• Interrupts from pins IRQ0 to IRQ7 • Number of sources: 8 • Interrupt detection: Low level/falling edge/rising edge/rising and falling edges One of these detection methods can be set for each source. • Digital filter function: Supported	• Interrupt by the input signal to the IRQi pin (i = 0 to 15) • Number of sources: 16 • Interrupt detection method: Detection of low level, falling edge, rising edge, rising and falling edges One of these detection methods can be set for each source. • Digital filter can be used to remove noise.
	Software interrupt	• Interrupt generated by writing to a register • One interrupt source	• Interrupt request can be generated by writing to a register. • Two interrupt sources
	Interrupt priority	Specified by registers.	Priority level can be set with interrupt source priority register r (IPRr) (r = 000 to 255).
	Fast interrupt function	Faster interrupt processing of the CPU can be set only for a single interrupt source.	CPU interrupt response time can be reduced. This function can be used for only one interrupt source.

Item		RX24T(ICUb)	RX66T(ICUC)
Interrupts	DTC control	• Interrupt sources can be used to start the DTC. • Number of DTC activating sources: 118 (109 peripheral function interrupts + 8 external pin interrupts + 1 software interrupt)	• Interrupt sources can be used to start the DTC. • Number of DTC activating sources: 129 (111 peripheral function interrupts + 16 external pin interrupts + 2 software interrupt)
	DMAC control	—	Interrupt sources can be used to start the DMAC.
Non-maskable interrupts	NMI pin interrupt	• Interrupt from the NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter function: Supported	• Interrupt by the input signal to the NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter can be used to remove noise.
	Oscillation stop detection interrupt	Interrupt on detection of oscillation having stopped	This interrupt occurs when the main clock oscillator stop is detected.
	WDT underflow/refresh error interrupt	—	This interrupt occurs when the watchdog timer (WDT) underflows or a refresh error occurs.
	IWDT underflow/refresh error interrupt	Interrupt on an underflow of the down counter or occurrence of a refresh error	This interrupt occurs when the independent watchdog timer (IWDT) underflows or a refresh error occurs.
	Voltage monitoring 1 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 1 (LVD1)	Interrupt from voltage detection circuit 1 (LVD1)
	Voltage monitoring 2 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 2 (LVD2)	Interrupt from voltage detection circuit 2 (LVD2)
	RAM error interrupt	—	This interrupt occurs when a parity check error is detected in the RAM or an ECC error is detected in the ECCRAM.
Return from low power consumption state	Sleep mode	Return is initiated by non-maskable interrupts or any other interrupt source.	Exit sleep mode by any interrupt source.
	All-module clock stop mode	—	Exit all-module clock stop mode by the NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, oscillation stop detection interrupt, USB resume, IWDT, TMR0 to TMR3).
	Deep sleep mode	Return is initiated by non-maskable interrupts or any other interrupt source.	—
	Software standby mode	Return is initiated by non-maskable interrupts, IRQ0 to IRQ7 interrupts, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, IWDT).	Exit software standby mode by the NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB resume, IWDT).
	Deep software standby mode	—	Exit deep software standby mode by the NMI pin interrupt, specific external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2).

Table 2.20 Comparison of Registers for Interrupt Controller

Register	Bit	RX24T(ICUb)	RX66T(ICUC)
IPRn	—	Interrupt Source Priority Register n (n = 000 to 249)	Interrupt Source Priority Register n (n = 000 to 255)
SWINT2R	—	—	Software Interrupt 2 Generation Register
DTCERn	—	DTC Transfer Request Enable Register n (n = 27 to 248)	DTC Transfer Request Enable Register n (n = 26 to 255)
DMRSRm	—	—	DMAC trigger Select Register m (m = 0 to 7)
IRQCRi	—	IRQ Control Register i (i = 0 to 7)	IRQ Control Register i (i = 0 to 15)
IRQFLTE1	—	—	IRQ Pin Digital Filter Enable Register 1
IRQFLTC1	—	—	IRQ Pin Digital Filter Setting Register 1
NMISR	WDTST	—	WDT Underflow/Refresh Error Status Flag
	RAMST	—	RAM Error Interrupt Status Flag
NMIER	WDTEN	—	WDT Underflow/Refresh Error Enable
	RAMEN	—	RAM Error Interrupt Enable
NMICLR	WDTCLR	—	WDT Clear
GRPBE0, GRPBL0/ GRPBL1, GRPAL0	—	—	Group BE0, BL0/1, AL0 Interrupt Request Register
GENBE0, GENBL0/ GENBL1, GENAL0	—	—	Group BE0, BL0/1, AL0 Interrupt Request Enable Register
GCRBE0	—	—	Group BE0 Interrupt Clear Register
PIARk	—	—	Software Configurable Interrupt A Request Register k (k = 0h to 12h)
SLIARn	—	—	Software Configurable Interrupt A Source Select Register n (n = 208 to 255)
SLIPRCR	—	—	Software Configurable Interrupt Source Select Register Write Protect Register

2.10 Buses

Table 2.21 lists Comparison of Specifications for Buses, Table 2.22 lists Comparison of Specifications for External Bus and Table 2.23 lists Comparison of Registers for Buses.

Table 2.21 Comparison of Specifications for Buses

Item		RX24T	RX66T
CPU bus	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
Memory bus	Memory bus 1	Connected to RAM	Connected to RAM
	Memory bus 2	Connected to ROM	Connected to code flash memory
	Memory bus 3	—	Connected to ECCRAM
Internal main bus	Internal main bus 1	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to the DTC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the DMAC and DTC • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
Internal peripheral bus	Internal peripheral bus 1	• Connected to peripheral modules (DTC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (DTC, DMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)
	Internal peripheral bus 2	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, and 4) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 3	• Connected to peripheral modules (RSCAN, CMPC) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (USBb and CMPC) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 4	• Connected to peripheral modules (MTU, GPT) • Operates in synchronization with the peripheral-module clock (PCLKA)	• Connected to peripheral modules (MTU3, GPTW, HRPWM, RSPI and SCIi) • Operates in synchronization with the peripheral-module clock (PCLKA)
	Internal peripheral bus 5	—	Reserved area
	Internal peripheral bus 6	• Connected to the flash control module and E2 DataFlash • Operates in synchronization with the FlashIF clock (FCLK)	• Connected to code flash (in P/E) and data flash memory • Operates in synchronization with the FlashIF clock (FCLK)
External bus	CS area	—	• Connected to the external devices • Operates in synchronization with the external-bus clock (BCLK: 40 MHz (max.))

Table 2.22 Comparison of Specifications for External Bus

Item	RX24T	RX66T
External address space	—	• An external address space is divided into four CS areas (CS0: 2 Mbytes, CS1: 2 Mbytes, CS2: 2 Mbytes, CS3: 2 Mbytes) for management. • Chip select signals can be output for each area. • Bus width can be set for each area. - Separate bus: An 8 or 16-bit bus space is selectable. - Address/data multiplexed bus: An 8 or 16-bit bus space is selectable. • An endian mode can be specified for each area.
CS area controller	—	• Recovery cycles can be inserted. - Read recovery: Up to 15 cycles - Write recovery: Up to 15 cycles • Cycle wait function: Wait for up to 31 cycles (page access: up to 7 cycles) • Wait control can be used to set up the following. - Timing of assertion and negation for chip-select signals (CS0# to CS3#) - The timing of assertion of the read signal (RD#) and write signals (WR0#/WR# and WR1#) - The timing with which data output starts and ends • Write access mode: Single write strobe mode/byte strobe mode • Separate bus or address/data multiplexed bus can be set for each area.
Write buffer function	—	When write data from the bus master has been written to the write buffer, write access by the bus master is completed.
Frequency	—	• The CS area controller (CSC) operates in synchronization with the external-bus clock (BCLK).
Address bus	—	A20 to A0

Table 2.23 Comparison of Registers for Buses

Register	Bit	RX24T	RX66T
CSnCR	—	—	CSn Control Register (n = 0 to 3)
CSnREC	—	—	CSn Recovery Cycle Register (n = 0 to 3)
CSRECEN	—	—	CS Recovery Cycle Insertion Enable Register
CSnMOD	—	—	CSn Mode Register (n = 0 to 3)
CSnWCR1	—	—	CSn Wait Control Register 1 (n = 0 to 3)
CSnWCR2	—	—	CSn Wait Control Register 2 (n = 0 to 3)
BUSPRI	BPRA[1:0]	Memory Bus 1 (RAM) Priority Control	Memory Bus 1 and 3 (RAM/ECCRAM) Priority Control
	BPEB[1:0]	—	External Bus Priority Control

2.11 Data Transfer Controller

Table 2.24 lists Comparison of Specifications for Data Transfer Controller.

Table 2.24 Comparison of Specifications for Data Transfer Controller

Item	RX24T(DTCa)	RX66T(DTCa)
Transfer modes	• Normal transfer mode A single transfer request leads to a single data transfer. • Repeat transfer mode - A single transfer request leads to a single data transfer. - The transfer address is returned to the transfer start address after the number of data transfers corresponding to “repeat size”. - The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, 1024 bytes. • Block transfer mode - A single transfer request leads to the transfer of a single block. - The maximum block size is 256 × 32 bits = 1024 bytes.	• Normal transfer mode A single transfer request leads to a single data transfer. • Repeat transfer mode - A single transfer request leads to a single data transfer. - The transfer address is returned to the transfer start address after the number of data transfers corresponding to “repeat size”. - The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, 1024 bytes. • Block transfer mode - A single transfer request leads to the transfer of a single block. - The maximum block size is 256 × 32 bits = 1024 bytes.
Number of transfer channels	The same number as all interrupt sources that can start the DTC transfer.	The same number as all interrupt sources that can start the DTC transfer.
Chain transfer	• Multiple types of data transfers can sequentially be executed in response to a single request. • Either “performed only when the transfer counter becomes 0” or “every time” can be selected.	• Multiple types of data transfers can sequentially be executed in response to a single request. • Either “performed only when the transfer counter becomes 0” or “every time” can be selected.
Transfer space	• In short-address mode: 16 Mbytes (Areas from 0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh except reserved areas) • In full-address mode: 4 Gbytes (Area from 0000 0000h to FFFF FFFFh except reserved areas)	• In short-address mode: 16 Mbytes (Areas from 0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh except reserved areas) • In full-address mode: 4 Gbytes (Area from 0000 0000h to FFFF FFFFh except reserved areas)
Data transfer units	• Single data: 1 byte (8 bits), 1 word (16 bits), 1 longword (32 bits) • Single block size: 1 to 256 data	• Single data: 1 byte (8 bits), 1 word (16 bits), 1 longword (32 bits) • Single block size: 1 to 256 data
CPU interrupt source	• An interrupt request can be generated to the CPU on a request source for a data transfer. • An interrupt request can be generated to the CPU after a single data transfer. • An interrupt request can be generated to the CPU after data transfer of specified volume.	• An interrupt request can be generated to the CPU on a request source for a data transfer. • An interrupt request can be generated to the CPU after a single data transfer. • An interrupt request can be generated to the CPU after data transfer of specified volume.
Event link function	—	An event link request is generated after one data transfer (for block, after one block transfer).
Read skip	Reading of the transfer information can be skipped when the same transfer is repeated.	Reading of the transfer information can be skipped when the same transfer is repeated.

Item	RX24T(DTCa)	RX66T(DTCa)
Write-back skip	Write-back of the transferred data that is not updated can be skipped when the address of the transfer source or destination is fixed.	Write-back of the transferred data that is not updated can be skipped when the address of the transfer source or destination is fixed.
Low power consumption function	Module stop state can be set.	Module stop state can be set.

2.12 I/O Ports

Table 2.25 to Table 2.28 list the comparison of I/O ports specifications for each package and Table 2.29 lists the Comparison of Registers for I/O Ports.

Table 2.25 Comparison of Specifications for I/O Ports in 100-Pin Packages

(RX66T: with PGA pseudo-differential input)

Item	RX24T(100 Pins) (Common to Chip Version A and B)	RX66T(100 Pins)	
		with PGA pseudo-differential input and with USB pin	with PGA pseudo-differential input and without USB pin
PORT0	P00 to P02	P00, P01	P00, P01
PORT1	P10, P11	P10, P11	P10, P11
PORT2	P20 to P24	P20 to P24, P27	P20 to P24, P27
PORT3	P30 to P33, P36, P37	P30 to P33, P36, P37	P30 to P33, P36, P37
PORT4	P40 to P47	P40 to P47	P40 to P47
PORT5	P50 to P55	P52 to P55	P52 to P55
PORT6	P60 to P65	P60 to P65	P60 to P65
PORT7	P70 to P76	P70 to P76	P70 to P76
PORT8	P80 to P82	P80 to P82	P80 to P82
PORT9	P90 to P96	P90 to P96	P90 to P96
PORTA	PA0 to PA5	PA0 to PA5	PA0 to PA5
PORTB	PB0 to PB7	PB0 to PB6	PB0 to PB7
PORTC	—	—	—
PORTD	PD0 to PD7	PD2 to PD7	PD0 to PD7
PORTE	PE0 to PE5	PE0 to PE5	PE0 to PE5
PORTF	—	—	—
PORTG	—	—	—
PORTH	—	PH0, PH4	PH0, PH4
PORTK	—	—	—

Table 2.26 Comparison of Specifications for I/O Ports in 100-Pin Packages

(RX66T: without PGA pseudo-differential input)

Item	RX24T(100 Pins) (Common to Chip Version A and B)	RX66T(100 Pins) (without PGA pseudo-differential input and without USB pin)
PORT0	P00 to P02	P00, P01
PORT1	P10, P11	P10, P11
PORT2	P20 to P24	P20 to P24
PORT3	P30 to P33, P36, P37	P30 to P33, P36, P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P55	P50 to P55
PORT6	P60 to P65	P60 to P65
PORT7	P70 to P76	P70 to P76
PORT8	P80 to P82	P80 to P82
PORT9	P90 to P96	P90 to P96
PORTA	PA0 to PA5	PA0 to PA5
PORTB	PB0 to PB7	PB0 to PB7
PORTC	—	—
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE5	PE0 to PE5
PORTF	—	—
PORTG	—	—
PORTH	—	—
PORTK	—	—

Table 2.27 Comparison of Specifications for I/O Ports in 80-Pin Packages

Item	RX24T(80 Pins)	RX66T(80 Pins) (with PGA pseudo-differential input and without USB pin)
PORT0	P00 to P02	P00, P01
PORT1	P10, P11	P10, P11
PORT2	P20 to P24	P20 to P22, P27
PORT3	P30, P31, P36, P37	P30, P31, P36, P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P55	P52 to P55
PORT6	P62	P62, P64, P65
PORT7	P70 to P76	P70 to P76
PORT8	—	—
PORT9	P90 to P96	P90 to P96
PORTA	PA3, PA5	PA3, PA5
PORTB	PB0 to PB6	PB0 to PB6
PORTC	—	—
PORTD	PD2 to PD7	PD2 to PD7
PORTE	PE2 to PE4	PE2 to PE4
PORTF	—	—
PORTG	—	—
PORTH	—	PH0, PH4
PORTK	—	—

Table 2.28 Comparison of Specifications for I/O Ports in 64-Pin Packages

Item	RX24T(64 Pins)	RX66T(64 Pins) (with PGA pseudo-differential input and without USB pin)
PORT0	P00 to P02	P00, P01
PORT1	P11	P11
PORT2	P21 to P24	P20 to P22
PORT3	P30, P31, P36, P37	P36, P37
PORT4	P40 to P42, P44 to P46	P40 to P42, P44 to P46
PORT5	P50 to P54	P52 to P54
PORT6	—	P64, P65
PORT7	P70 to P76	P70 to P76
PORT8	—	—
PORT9	P90 to P96	P90 to P96
PORTA	—	—
PORTB	PB1 to PB6	PB0 to PB6
PORTC	—	—
PORTD	PD3 to PD7	PD3 to PD7
PORTE	PE2	PE2
PORTF	—	—
PORTG	—	—
PORTH	—	PH0, PH4
PORTK	—	—

Table 2.29 Comparison of Registers for I/O Ports

Register	Bit	RX24T	RX66T
PDR	—	Pm0 to 7 I/O Select (m = 0 to 9, A, B, D, E)	Pm0 to 7 I/O Select (m = 0 to 9, A to H, K)
PODR	—	Pm0 to 7 Output Data Store (m = 0 to 9, A, B, D, E)	Pm0 to 7 Output Data Store (m = 0 to 9, A to H, K)
PIDR	—	Pm0 to 7 (m = 0 to 9, A, B, D, E)	Pm0 to 7 (m = 0 to 9, A to H, K)
PMR	—	Pm0 to 7 Pin Mode Control (m = 0 to 3, 7 to 9, A, B, D, E)	Pm0 to 7 Pin Mode Control (m = 0 to 9, A to H, K)
ODR0	B0	Pm0 Output Type Select (m = 0 to 3, 7 to 9, A, B, D, E)	Pm0 Output Type Select (m = 0 to 9, A to H, K)
	B2	Pm1 Output Type Select (m = 0 to 3, 7 to 9, A, B, D, E)	Pm1 Output Type Select (m = 0 to 9, A to H, K)
	B4	Pm2 Output Type Select (m = 0 to 3, 7 to 9, A, B, D, E)	Pm2 Output Type Select (m = 0 to 9, A to H, K)
	B6	Pm3 Output Type Select (m = 0 to 3, 7 to 9, A, B, D, E)	Pm3 Output Type Select (m = 0 to 9, A to H, K)
ODR1	B0	Pm4 Output Type Select (m = 2, 7, 9, A, B, D, E)	Pm4 Output Type Select (m = 1 to 7, 9, A to E, H)
	B2	Pm5 Output Type Select (m = 2, 7, 9, A, B, D, E)	Pm5 Output Type Select (m = 1 to 7, 9, A to E, H)
	B4	Pm6 Output Type Select (m = 2, 7, 9, A, B, D, E)	Pm6 Output Type Select (m = 1 to 7, 9, A to E, H)
	B6	Pm7 Output Type Select (m = 2, 7, 9, A, B, D, E)	Pm7 Output Type Select (m = 1 to 7, 9, A to E, H)
PCR	—	Pm0 to 7 Input Pull-Up Resistor Control (m = 0 to 9, A, B, D, E)	Pm0 to 7 Input Pull-Up Resistor Control (m = 0 to 9, A to H, K)
DSCR	—	Pm0 to 7 Drive Capacity Control (m = 0 to 3, 7 to 9, A, B, D, E)	Pm0 to 7 Drive Capacity Control (m = 0 to 3, 7 to 9, A to G, K)
DSCR2	—	—	Drive Capacity Control Register 2

2.13 Multi-Function Pin Controller

Table 2.30 lists Comparison of Registers for Multi-Function Pin Controller.

Table 2.30 Comparison of Registers for Multi-Function Pin Controller

Register	Bit	RX24T(MPC)	RX66T(MPC)
PmnPFS	—	Refer to the user's manual for descriptions of the pin function control registers.	
PFCSE	—	—	CS Output Enable Register
PFCSS0	—	—	CS Output Pin Select Register 0
PFAOE0	—	—	Address Output Enable Register 0
PFAOE1	—	—	Address Output Enable Register 1
PFBCR0	—	—	External Bus Control Register 0
PFBCR1	—	—	External Bus Control Register 1
PFBCR2	—	—	External Bus Control Register 2
PFBCR3	—	—	External Bus Control Register 3
PFBCR4	—	—	External Bus Control Register 4

2.14 Multi-Function Timer Pulse Unit 3

Table 2.31 lists Comparison of Specifications for Multi-Function Timer Pulse Unit 3 and Table 2.32 lists Comparison of Registers for Multi-Function Timer Pulse Unit 3.

Table 2.31 Comparison of Specifications for Multi-Function Timer Pulse Unit 3

Item	RX24T(MTU3d)	RX66T(MTU3d)
Pulse input/output	28 lines max.	28 lines max.
Pulse input	3 lines	3 lines
Count clock	11 clocks for each channel (14 clocks for MTU0 and MTU9, 12 clocks for MTU2, 10 clocks for MTU5, and four clocks for MTU1 & MTU2 (LWA = 1))	11 clocks for each channel (14 clocks for MTU0 and MTU9, 12 clocks for MTU2, 10 clocks for MTU5, and four clocks for MTU1 & MTU2 (LWA = 1))
Operating frequency	Up to 80 MHz	Up to 160 MHz
Available operations	[MTU0 to MTU4, MTU6, MTU7, MTU9] • Waveform output on compare match • Input capture function (noise filter setting available) • Counter-clearing operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing on compare match or input capture • Simultaneous input and output to registers in synchronization with counter operations • Up to 14-phase PWM output in combination with synchronous operation	[MTU0 to MTU4, MTU6, MTU7, MTU9] • Waveform output on compare match • Input capture function (noise filter setting available) • Counter-clearing operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing on compare match or input capture • Simultaneous input and output to registers in synchronization with counter operations • Up to 14-phase PWM output in combination with synchronous operation
	[MTU0, MTU3, MTU4, MTU6, MTU7, MTU9] Buffer operation specifiable	[MTU0, MTU3, MTU4, MTU6, MTU7, and MTU9] Buffer operation specifiable
	[MTU3, MTU4, MTU6, MTU7] • Through interlocked operation of MTU3/4 and MTU6/7, the positive and negative signals in six phases (12 phases in total) can be output in complementary PWM and reset PWM operation. • In complementary PWM mode, transfer of values from buffer registers to temporary registers on peaks or troughs of the timer-counter values or writing to the buffer registers (MTU4.TGRD and MTU7.TGRD) • Double-buffering selectable in complementary PWM mode	[MTU3, MTU4, MTU6, MTU7] • Through interlocked operation of MTU3/4 and MTU6/7, the positive and negative signals in six phases (12 phases in total) can be output in complementary PWM and reset-synchronized PWM operation. • In complementary PWM mode, transfer of values from buffer registers to temporary registers on crests or troughs of the timer-counter values or writing to the buffer registers (MTU4.TGRD and MTU7.TGRD) • Double-buffering selectable in complementary PWM mode
	[MTU1, MTU2] • Phase counting mode can be specified independently • 32-bit phase counting mode can be specified for interlocked operation of MTU1 and MTU2 (when TMDR3.LWA = 1) • Cascade connection operation available	[MTU1, MTU2] • Phase counting mode can be specified independently • 32-bit phase counting mode can be specified for interlocked operation of MTU1 and MTU2 (when TMDR3.LWA = 1) • Cascade connection operation available

Item	RX24T(MTU3d)	RX66T(MTU3d)
Available operations	[MTU3, MTU4] • Through interlocking with MTU0, a mode for driving AC synchronous motors (brushless DC motors) by using complementary PWM output and reset PWM output is settable and allows the selection of two types of waveform output (chopping or level)	[MTU3, MTU4] • Through interlocking with MTU0, a mode for driving AC synchronous motors (brushless DC motors) by using complementary PWM output and reset-synchronized PWM output is settable and allows the selection of two types of waveform output (chopping or level)
	[MTU5] • Capable of operation as a dead-time compensation counter	[MTU5] • Capable of operation as a dead-time compensation counter
	[MTU6, MTU7] • Through interlocking with MTU9, a mode for driving AC synchronous motors (brushless DC motors) by using complementary PWM output and reset PWM output is settable and allows the selection of two types of waveform output (chopping or level)	[MTU6, MTU7] • Through interlocking with MTU9, a mode for driving AC synchronous motors (brushless DC motors) by using complementary PWM output and reset-synchronized PWM output is settable and allows the selection of two types of waveform output (chopping or level)
Interrupt skipping function	In complementary PWM mode, interrupts on crests and troughs of counter values and triggers to start conversion by the A/D converter can be skipped	In complementary PWM mode, interrupts on crests and troughs of counter values and triggers to start conversion by the A/D converter can be skipped
Interrupt sources	45 sources	45 sources
Buffer operation	Automatic transfer of register data (transfer from the buffer register to the timer register)	Automatic transfer of register data (transfer from the buffer register to the timer register)
Trigger generation	A/D converter start triggers can be generated	A/D converter start triggers can be generated
	A/D converter start request delaying function enables A/D converter to be started with any desired timing and to be synchronized with PWM output	A/D converter start request delaying function enables A/D converter to be started with any desired timing and to be synchronized with PWM output
Low power consumption function	Module stop mode can be set	Module stop mode can be set

Table 2.32 Comparison of Registers for Multi-Function Timer Pulse Unit 3

Register	Bit	RX24T(MTU3d)	RX66T(MTU3d)
TADSTRGR0	TADSMEN0	—	ADSM0 Pin Output Enable
TADSTRGR1	TADSMEN1	—	ADSM1 Pin Output Enable

2.15 Port Output Enable 3

Table 2.33 lists Comparison of Specifications for Port Output Enable 3 and Table 2.34 lists Comparison of Registers for Port Output Enable 3.

Table 2.33 Comparison of Specifications for Port Output Enable 3

Item	RX24T(POE3b, POE3A)	RX66T(POE3B)
Function	• Each of the POE0#, POE4#, POE8#, POE10#, POE11#, and POE12# input pins can be set for falling edge, PCLK/8 × 16, PCLK/16 × 16, or PCLK/128 × 16 low-level sampling.	• Each of the POE0#, POE4#, POE8#, POE9#, POE10#, POE11#, POE12#, POE13#, and POE14# pins can be set for falling-edge or low-level detection. When setting a low-level detection, a sampling clock can be selected from PCLK/1, PCLK/2, PCLK/4, PCLK/8, PCLK/16, and PCLK/128, while the number of samples can be selected from four, eight, or 16.
	• The outputs of the target pins can be disabled by falling-edge or low-level sampling of the POE0#, POE4#, POE8#, POE10#, POE11#, or POE12# pin.	• The outputs of the target pins can be disabled by detecting falling-edge or low-level of input to the POE0#, POE4#, POE8#, POE9#, POE10#, POE11#, POE12#, POE13#, and POE14# pins.
	• The outputs of the target pins can be disabled when oscillation stop is detected by the oscillation stop detection function of the clock generator.	• The outputs of the target pins can be disabled when oscillation stop is detected by the oscillation stop detection function of the clock generator.
	• The MTU complementary PWM outputs can be disabled when output levels of the MTU complementary PWM output pins are compared and simultaneous active-level output continues for one cycle or more.	• The MTU complementary PWM outputs can be disabled when output levels of the MTU complementary PWM output pins are compared and simultaneous active-level output continues for one cycle or more.
	• The GPT outputs can be disabled when output levels of the GPT output pins (GPT0, GPT1, and GPT2) are compared and simultaneous active-level output continues for one cycle or more.	• The GPTW outputs can be disabled when output levels of the GPTW output pins (GPTW0 to GPTW2, GPTW4 to GPTW6, and GPTW7 to GPTW9 pins) are compared and simultaneous active-level output continues for one cycle or more.
	• The outputs of the target pins can be disabled in response to comparator C (CMPC) output detection.	• The outputs of the target pins can be disabled in response to comparator C (CMPC) output detection.
	• The outputs of the target pins can be disabled by modifying the settings of the POE registers.	• The outputs of the target pins can be disabled by modifying the settings of the POE registers.
	• Interrupts can be generated by input-level sampling or output-level comparison results.	• Interrupts can be generated by input-level sampling or output-level comparison results.
Pin status while output is disabled	• High-impedance • General I/O port (available only for chip version B)	• High-impedance • General I/O port

Item	RX24T(POE3b, POE3A)	RX66T(POE3B)
Target pins for switching to disabling of signal output	• MTU output pins - MTU0 pins (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) - MTU3 pins (MTIOC3B, MTIOC3D) - MTU4 pins (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D) - MTU6 pins (MTIOC6B, MTIOC6D) - MTU7 pins (MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D) - MTU9 pins (MTIOC9A, MTIOC9B, MTIOC9C, MTIOC9D) • GPT output pins (available only for chip version B) - GPT0 pins (GTIOC0A, GTIOC0B) - GPT1 pins (GTIOC1A, GTIOC1B) - GPT2 pins (GTIOC2A, GTIOC2B) - GPT3 pins (GTIOC3A, GTIOC3B)	• MTU output pins - MTU0 pins (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) - MTU3 pins (MTIOC3B, MTIOC3D) - MTU4 pins (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D) - MTU6 pins (MTIOC6B, MTIOC6D) - MTU7 pins (MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D) - MTU9 pins (MTIOC9A, MTIOC9B, MTIOC9C, MTIOC9D) • GPTW output pins - GPTW0 pins (GTIOC0A, GTIOC0B) - GPTW1 pins (GTIOC1A, GTIOC1B) - GPTW2 pins (GTIOC2A, GTIOC2B) - GPTW3 pins (GTIOC3A, GTIOC3B) - GPTW4 pins (GTIOC4A, GTIOC4B) - GPTW5 pins (GTIOC5A, GTIOC5B) - GPTW6 pins (GTIOC6A, GTIOC6B) - GPTW7 pins (GTIOC7A, GTIOC7B) - GPTW8 pins (GTIOC8A, GTIOC8B) - GPTW9 pins (GTIOC9A, GTIOC9B)

Item	RX24T(POE3b, POE3A)	RX66T(POE3B)
Generating conditions of request for switching to disable output	• Input signal detection: Detection of the POE0#, POE4#, POE8#, POE10#, POE11#, and POE12# signal level. • Simultaneous conduction between output pins: A match (simultaneous conduction) between the output signal levels at the active level over one or more cycles on the following combination of pins MTU Complementary PWM Output Pins - MTIOC3B and MTIOC3D - MTIOC4A and MTIOC4C - MTIOC4B and MTIOC4D - MTIOC6B and MTIOC6D - MTIOC7A and MTIOC7C - MTIOC7B and MTIOC7D GPT Output Pins - GTIOC0A and GTIOC0B - GTIOC1A and GTIOC1B - GTIOC2A and GTIOC2B • Register setting to disable output being made • Detection that the main clock oscillator had stopped oscillating • Comparator output detection in the comparator C (CMPC)	• Input signal detection: Detection of the POE0#, POE4#, POE8#, POE9#, POE10#, POE11#, POE12#, POE13#, and POE14# signal level. • Simultaneous conduction between output pins: A match (simultaneous conduction) between the output signal levels at the active level over one or more cycles on the following combination of pins MTU Complementary PWM Output Pins - MTIOC3B and MTIOC3D - MTIOC4A and MTIOC4C - MTIOC4B and MTIOC4D - MTIOC6B and MTIOC6D - MTIOC7A and MTIOC7C - MTIOC7B and MTIOC7D GPTW Output Pins - GTIOC0A and GTIOC0B - GTIOC1A and GTIOC1B - GTIOC2A and GTIOC2B - GTIOC4A and GTIOC4B - GTIOC5A and GTIOC5B - GTIOC6A and GTIOC6B - GTIOC7A and GTIOC7B - GTIOC8A and GTIOC8B - GTIOC9A and GTIOC9B • SPOER register setting being made • Detection that the main clock oscillator had stopped oscillating • Comparator output detection in the comparator C (CMPC) outputs

Table 2.34 Comparison of Registers for Port Output Enable 3

Register	Bit	RX24T(POE3b, POE3A)	RX66T(POE3B)
ICSR1	POE0M[1:0](RX24T) POE0M[3:0](RX66T)	POE0 Mode Select b1 b0 0 0: Accepts a request on the falling edge of POE0# pin input. 0 1: Accepts a request when POE0# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when POE0# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when POE0# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	POE0 Mode Select b3 b0 0 0 0 0: Accepts a request on the falling edge of POE0# pin input. 0 0 0 1: Samples the level of the POE0# pin input by PCLK/8, and accepts a request when consecutive low-level results are detected for the specified times. 0 0 1 0: Samples the level of the POE0# pin input by PCLK/16, and accepts a request when consecutive low-level results are detected for the specified times. 0 0 1 1: Samples the level of the POE0# pin input by PCLK/128, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 0 0: Samples the level of the POE0# pin input by PCLK, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 0 1: Samples the level of the POE0# pin input by PCLK/2, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 1 0: Samples the level of the POE0# pin input by PCLK/4, and accepts a request when consecutive low-level results are detected for the specified times. Settings other than above are prohibited.
	POE0M2[3:0]	—	POE0 Sampling Count Select
	POE0F	POE0 Flag [Setting condition] When the input set by the POE0M[1:0] bits occurs at the POE0# pin [Clearing condition] By writing 0 to the POE0F flag after reading POE0F = 1 When low-level sampling is set by the POE0M[1:0] bits, the high level needs to be input to the POE0# pin to write 0 to this flag.	POE0 Flag [Setting condition] When the input set by the POE0M[3:0] and POE0M2[3:0] bits occurs at the POE0# pin [Clearing condition] By writing 0 to the POE0F flag after reading POE0F = 1 When low-level sampling is set by the POE0M[3:0] bits, the high level needs to be input to the POE0# pin to write 0 to this flag.

Register	Bit	RX24T(POE3b, POE3A)	RX66T(POE3B)
ICSR2	POE4M[1:0](RX24T) POE4M[3:0](RX66T)	POE4 Mode Select b1 b0 0 0: Accepts a request on the falling edge of POE4# pin input. 0 1: Accepts a request when POE4# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when POE4# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when POE4# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	POE4 Mode Select b3 b0 0 0 0 0: Accepts a request on the falling edge of POE4# pin input. 0 0 0 1: Samples the level of the POE4# pin input by PCLK/8, and accepts a request when consecutive low-level results are detected for the specified times. 0 0 1 0: Samples the level of the POE4# pin input by PCLK/16, and accepts a request when consecutive low-level results are detected for the specified times. 0 0 1 1: Samples the level of the POE4# pin input by PCLK/128, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 0 0: Samples the level of the POE4# pin input by PCLK, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 0 1: Samples the level of the POE4# pin input by PCLK/2, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 1 0: Samples the level of the POE4# pin input by PCLK/4, and accepts a request when consecutive low-level results are detected for the specified times. Settings other than above are prohibited.
	POE4M2[3:0]	—	POE4 Sampling Count Select
	POE4F	POE4 Flag [Setting condition] When the input set by POE4M[1:0] occurs at the POE4# pin [Clearing condition] By writing 0 to POE4F after reading POE4F = 1 When low-level sampling is set by the POE4M[1:0] bits, the high level needs to be input to the POE4# pin to write 0 to this flag.	POE4 Flag [Setting condition] When the input set by the POE4M[3:0] and POE4M2[3:0] bits occurs at the POE4# pin [Clearing condition] By writing 0 to the POE4F after reading POE4F = 1 When low-level sampling is set by the POE4M[3:0] bits, the high level needs to be input to the POE4# pin to write 0 to this flag.

Register	Bit	RX24T(POE3b, POE3A)	RX66T(POE3B)
ICSR3	POE8M[1:0](RX24T) POE8M[3:0](RX66T)	POE8 Mode Select b1 b0 0 0: Accepts a request on the falling edge of POE8# pin input. 0 1: Accepts a request when POE8# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when POE8# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when POE8# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	POE8 Mode Select b3 b0 0 0 0 0: Accepts a request on the falling edge of POE8# pin input. 0 0 0 1: Samples the level of the POE8# pin input by PCLK/8, and accepts a request when consecutive low-level results are detected for the specified times. 0 0 1 0: Samples the level of the POE8# pin input by PCLK/16, and accepts a request when consecutive low-level results are detected for the specified times. 0 0 1 1: Samples the level of the POE8# pin input by PCLK/128, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 0 0: Samples the level of the POE8# pin input by PCLK, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 0 1: Samples the level of the POE8# pin input by PCLK/2, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 1 0: Samples the level of the POE8# pin input by PCLK/4, and accepts a request when consecutive low-level results are detected for the specified times. Settings other than above are prohibited.
	POE8M2[3:0]	—	POE8 Sampling Count Select
	POE8F	POE8 Flag [Setting condition] When the input set by the POE8M[1:0] bits occurs at the POE8# pin [Clearing condition] By writing 0 to the POE8F flag after reading POE8F = 1 When low-level sampling is set by the POE8M[1:0] bits, the high level needs to be input to the POE8# pin to write 0 to this flag.	POE8 Flag [Setting condition] When the input set by the POE8M[3:0] and POE8M2[3:0] bits occurs at the POE8# pin [Clearing condition] By writing 0 to the POE8F flag after reading POE8F = 1 When low-level sampling is set by the POE8M[3:0] bits, the high level needs to be input to the POE8# pin to write 0 to this flag.

Register	Bit	RX24T(POE3b, POE3A)	RX66T(POE3B)
ICSR4	POE10M[1:0](RX24T) POE10M[3:0](RX66T)	POE10 Mode Select b1 b0 0 0: Accepts a request on the falling edge of POE10# pin input. 0 1: Accepts a request when POE10# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when POE10# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when POE10# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	POE10 Mode Select b3 b0 0 0 0 0: Accepts a request on the falling edge of POE10# pin input. 0 0 0 1: Samples the level of the POE10# pin input by PCLK/8, and accepts a request when consecutive low-level results are detected for the specified times. 0 0 1 0: Samples the level of the POE10# pin input by PCLK/16, and accepts a request when consecutive low-level results are detected for the specified times. 0 0 1 1: Samples the level of the POE10# pin input by PCLK/128, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 0 0: Samples the level of the POE10# pin input by PCLK, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 0 1: Samples the level of the POE10# pin input by PCLK/2, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 1 0: Samples the level of the POE10# pin input by PCLK/4, and accepts a request when consecutive low-level results are detected for the specified times. Settings other than above are prohibited.
	POE10M2[3:0]	—	POE10 Sampling Count Select
	POE10F	POE10 Flag [Setting condition] When the input set by the POE10M[1:0] bits occurs at the POE10# pin [Clearing condition] By writing 0 to the POE10F flag after reading POE10F = 1 When low-level sampling is set by the POE10M[1:0] bits, the high level needs to be input to the POE10# pin to write 0 to this flag.	POE10 Flag [Setting condition] When the input set by the POE10M[3:0] and POE10M2[3:0] bits occurs at the POE10# pin [Clearing condition] By writing 0 to the POE10F flag after reading POE10F = 1 When low-level sampling is set by the POE10M[3:0] bits, the high level needs to be input to the POE10# pin to write 0 to this flag.

Register	Bit	RX24T(POE3b, POE3A)	RX66T(POE3B)
ICSR5	POE11M[1:0](RX24T) POE11M[3:0](RX66T)	POE11 Mode Select b1 b0 0 0: Accepts a request on the falling edge of POE11# pin input. 0 1: Accepts a request when POE11# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when POE11# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when POE11# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	POE11 Mode Select b3 b0 0 0 0 0: Accepts a request on the falling edge of POE11# pin input. 0 0 0 1: Samples the level of the POE11# pin input by PCLK/8, and accepts a request when consecutive low-level results are detected for the specified times. 0 0 1 0: Samples the level of the POE11# pin input by PCLK/16, and accepts a request when consecutive low-level results are detected for the specified times. 0 0 1 1: Samples the level of the POE11# pin input by PCLK/128, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 0 0: Samples the level of the POE11# pin input by PCLK, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 0 1: Samples the level of the POE11# pin input by PCLK/2, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 1 0: Samples the level of the POE11# pin input by PCLK/4, and accepts a request when consecutive low-level results are detected for the specified times. Settings other than above are prohibited.
	POE11M2[3:0]	—	POE11 Sampling Count Select
	POE11F	POE11 Flag [Setting condition] When the input set by the POE11M[1:0] bits occurs at the POE11# pin [Clearing condition] By writing 0 to the POE11F flag after reading POE11F = 1 When low-level sampling is set by the POE11M[1:0] bits, the high level needs to be input to the POE11# pin to write 0 to this flag.	POE11 Flag [Setting condition] When the input set by the POE11M[3:0] and POE11M2[3:0] bits occurs at the POE11# pin [Clearing condition] By writing 0 to the POE11F flag after reading POE11F = 1 When low-level sampling is set by the POE11M[3:0] bits, the high level needs to be input to the POE11# pin to write 0 to this flag.

Register	Bit	RX24T(POE3b, POE3A)	RX66T(POE3B)
ICSR7	POE12M[1:0](RX24T) POE12M[3:0](RX66T)	POE12 Mode Select b1 b0 0 0: Accepts a request on the falling edge of POE12# pin input. 0 1: Accepts a request when POE12# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when POE12# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when POE12# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	POE12 Mode Select b3 b0 0 0 0 0: Accepts a request on the falling edge of POE12# pin input. 0 0 0 1: Samples the level of the POE12# pin input by PCLK/8, and accepts a request when consecutive low-level results are detected for the specified times. 0 0 1 0: Samples the level of the POE12# pin input by PCLK/16, and accepts a request when consecutive low-level results are detected for the specified times. 0 0 1 1: Samples the level of the POE12# pin input by PCLK/128, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 0 0: Samples the level of the POE12# pin input by PCLK, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 0 1: Samples the level of the POE12# pin input by PCLK/2, and accepts a request when consecutive low-level results are detected for the specified times. 0 1 1 0: Samples the level of the POE12# pin input by PCLK/4, and accepts a request when consecutive low-level results are detected for the specified times. Settings other than above are prohibited.
	POE12M2[3:0]	—	POE12 Sampling Count Select
	POE12F	POE12 Flag [Setting condition] When the input set by the POE12M[1:0] bits occurs at the POE12# pin [Clearing condition] By writing 0 to the POE12F flag after reading POE12F = 1 When low-level sampling is set by the POE12M[1:0] bits, the high level needs to be input to the POE12# pin to write 0 to this flag.	POE12 Flag [Setting condition] When the input set by the POE12M[3:0] and POE12M2[3:0] bits occurs at the POE12# pin [Clearing condition] By writing 0 to the POE12F flag after reading POE12F = 1 When low-level sampling is set by the POE12M[3:0] bits, the high level needs to be input to the POE12# pin to write 0 to this flag.
ICSR8	—	—	Input Level Control/Status Register 8
ICSR9	—	—	Input Level Control/Status Register 9

Register	Bit	RX24T(POE3b, POE3A)	RX66T(POE3B)
ICSR10	—	—	Input Level Control/Status Register 10
M0SELR1	—	—	MTU0 Pin Select Register 1
M0SELR2	—	—	MTU0 Pin Select Register 2
M3SELR	—	—	MTU3 Pin Select Register
M4SELR1	—	—	MTU4 Pin Select Register 1
M4SELR2	—	—	MTU4 Pin Select Register 2
M6SELR	—	—	MTU6 Pin Select Register
M7SELR1	—	—	MTU7 Pin Select Register 1
M7SELR2	—	—	MTU7 Pin Select Register 2
M9SELR1	—	—	MTU9 Pin Select Register 1
M9SELR2	—	—	MTU9 Pin Select Register 2
G0SELR	—	—	GPTW0 Pin Select Register
G1SELR	—	—	GPTW1 Pin Select Register
G2SELR	—	—	GPTW2 Pin Select Register
G3SELR	—	—	GPTW3 Pin Select Register
G4SELR	—	—	GPTW4 Pin Select Register
G5SELR	—	—	GPTW5 Pin Select Register
G6SELR	—	—	GPTW6 Pin Select Register
G7SELR	—	—	GPTW7 Pin Select Register
G8SELR	—	—	GPTW8 Pin Select Register
G9SELR	—	—	GPTW9 Pin Select Register
OCSR1	OSF1	Simultaneous Conduction Flag 1 This flag indicates that at least one of the three pairs of two-phase output pins assigned to ports P71 to P76 for MTU complementary PWM output (MTU3 and MTU4) or GPT output (GPT0 to GPT2) has simultaneously become at the active level. If the output disabling control for the corresponding pins is not enabled, this flag does not become 1. [Setting condition] • When the MTIOC3B/GTIOC0A and MTIOC3D/GTIOC0B pins simultaneously go to the active level while the value of the POECR2.MTU3BDZE bit, or of either or both of the PMMCR1.MTU3BME and PMMCR1.MTU3DME bits, is 1. • When the MTIOC4A/GTIOC1A and MTIOC4C/GTIOC1B pins simultaneously go to the active level while the value of the POECR2.MTU4ACZE bit, or either or both of the PMMCR1.MTU4AME and PMMCR1.MTU4CME bits, is 1. • When the MTIOC4B/GTIOC2A and MTIOC4D/GTIOC2B pins simultaneously go to the active level while the value of the POECR2.MTU4BDZE bit, or either or both of the PMMCR1.MTU4BME and PMMCR1.MTU4DME bits, is 1.	Simultaneous Conduction Flag 1 This flag indicates that at least one of the three pairs of two-phase output pins for MTU complementary PWM output (MTU3 and MTU4) has simultaneously become at the active level. If the output disabling control for the corresponding pins is not enabled, this flag does not become 1. [Setting condition] • When the MTIOC3B and MTIOC3D pins simultaneously go to the active level for at least one cycle of PCLK while the value of the POECR2.MTU3BDZE bit, or either or both of the PMMCR1.MTU3BME and PMMCR1.MTU3DME bits, is 1. • When the MTIOC4A and MTIOC4C pins simultaneously go to the active level for at least one cycle of PCLK while the value of the POECR2.MTU4ACZE bit, or either or both of the PMMCR1.MTU4AME and PMMCR1.MTU4CME bits, is 1. • When the MTIOC4B and MTIOC4D pins simultaneously go to the active level for at least one cycle of PCLK while the value of the POECR2.MTU4BDZE bit, or either or both of the PMMCR1.MTU4BME and PMMCR1.MTU4DME bits, is 1.

Register	Bit	RX24T(POE3b, POE3A)	RX66T(POE3B)
OCSR1	OSF1	[Clearing condition] By writing 0 to the OSF1 flag after reading OSF1 = 1 To write 0 to this flag, the inactive level needs to be output from MTU complementary PWM output pins or GPT output pins.	[Clearing condition] By writing 0 to the OSF1 flag after reading OSF1 = 1 To write 0 to this flag, the inactive level needs to be output of MTU complementary PWM output pins.
OCSR3	—	—	Output Level Control/Status Register 3
OCSR4	—	—	Output Level Control/Status Register 4
OCSR5	—	—	Output Level Control/Status Register 5
ALR1	OLSG0A	MTIOC3B/GTIOC0A (P71) Pin Active Level Setting	MTIOC3B Pin Active Level Setting
	OLSG0B	MTIOC3D/GTIOC0B (P74) Pin Active Level Setting	MTIOC3D Pin Active Level Setting
	OLSG1A	MTIOC4A/GTIOC1A (P72) Pin Active Level Setting	MTIOC4A Pin Active Level Setting
	OLSG1B	MTIOC4C/GTIOC1B (P75) Pin Active Level Setting	MTIOC4C Pin Active Level Setting
	OLSG2A	MTIOC4B/GTIOC2A (P73) Pin Active Level Setting	MTIOC4B Pin Active Level Setting
	OLSG2B	MTIOC4D/GTIOC2B (P76) Pin Active Level Setting	MTIOC4D Pin Active Level Setting
ALR3	—	—	Active Level Setting Register 3
ALR4	—	—	Active Level Setting Register 4
ALR5	—	—	Active Level Setting Register 5
SPOER	MTUCH34HIZ (Note 1)	MTU3 and MTU4 or GPT0 to GPT2 Pin Output Disable	MTU3 and MTU4 Pin Output Disable
	GPT01HIZ	—	GPTW0 and GPTW1 Pin Output Disable
	GPT03HIZ	GPT0 to GPT3 Pin Output Disable	—
	GPT23HIZ	—	GPTW2 and GPTW3 Pin Output Disable
	GPT02HIZ	—	GPTW0 to GPTW2 Pin Output Disable
	GPT46HIZ	—	GPTW4 to GPTW6 Pin Output Disable
	GPT79HIZ	—	GPTW7 to GPTW9 Pin Output Disable
POECR1	MTU0A1ZE	MTIOC0A (P31) Pin High-Impedance Enable	—
	MTU0B1ZE	MTIOC0B (P30) Pin High-Impedance Enable	—
POECR3	GPT0A1ZE	GTIOC0A (PD2) Pin High-Impedance Enable	—
	GPT0B1ZE	GTIOC0B (PD1) Pin High-Impedance Enable	—
	GPT1A1ZE	GTIOC1A (PD0) Pin High-Impedance Enable	—
	GPT1B1ZE	GTIOC1B (PB7) Pin High-Impedance Enable	—

Register	Bit	RX24T(POE3b, POE3A)	RX66T(POE3B)
POECR3	GPT2A1ZE	GTIOC2A (PB6) Pin High-Impedance Enable	—
	GPT2B1ZE	GTIOC2B (PB5) Pin High-Impedance Enable	—
	GPT3A1ZE	GTIOC3A High-Impedance Enable	—
	GPT3B1ZE	GTIOC3B High-Impedance Enable	—
	GPT0ABZE	—	GTIOC0A/GTIOC0B Pin High-Impedance Enable
	GPT1ABZE	—	GTIOC1A/GTIOC1B Pin High-Impedance Enable
	GPT2ABZE	—	GTIOC2A/GTIOC2B Pin High-Impedance Enable
	GPT3ABZE	—	GTIOC3A/GTIOC3B Pin High-Impedance Enable
	GPT4ABZE	—	GTIOC4A/GTIOC4B Pin High-Impedance Enable
	GPT5ABZE	—	GTIOC5A/GTIOC5B Pin High-Impedance Enable
	GPT6ABZE	—	GTIOC6A/GTIOC6B Pin High-Impedance Enable
	GPT7ABZE	—	GTIOC7A/GTIOC7B Pin High-Impedance Enable
	GPT8ABZE	—	GTIOC8A/GTIOC8B Pin High-Impedance Enable
	GPT9ABZE	—	GTIOC9A/GTIOC9B Pin High-Impedance Enable
POECR4	IC1ADDMT34ZE	—	MTU3 and MTU4 Output Disabling Condition POE0F Add
	CMADDMT67ZE	MTU6 and MTU7 Output Disabling Condition CFLAG Add	—
	IC1ADDMT67ZE	MTU6 and MTU7 Output Disabling Condition POE0F Add	—
	IC8ADDMT34ZE	—	MTU3 and MTU4 Output Disabling Condition POE9F Add
	IC9ADDMT34ZE	—	MTU3 and MTU4 Output Disabling Condition POE13F Add
	IC10ADDMT34ZE	—	MTU3 and MTU4 Output Disabling Condition POE14F Add
	IC3ADDMT67ZE	MTU6 and MTU7 Output Disabling Condition POE8F Add	—
	IC4ADDMT67ZE	MTU6 and MTU7 Output Disabling Condition POE10F Add	—
	IC5ADDMT67ZE	MTU6 and MTU7 Output Disabling Condition POE11F Add	—
	IC6ADDMT67ZE	MTU6 and MTU7 Output Disabling Condition POE12F Add	—
POECR4B	—	—	Port Output Enable Control Register 4B
POECR5	IC3ADDMT0ZE	—	MTU0 Output Disabling Condition POE8F Add
	IC8ADDMT0ZE	—	MTU0 Output Disabling Condition POE9F Add

Register	Bit	RX24T(POE3b, POE3A)	RX66T(POE3B)
POECR5	IC9ADDMT0ZE	—	MTU0 Output Disabling Condition POE13F Add
	IC10ADDMT0ZE	—	MTU0 Output Disabling Condition POE14F Add
POECR6	CMADDGPT01ZE	—	GPTW0 and GPTW1 Output Disabling Condition CFLAG Add
	IC1ADDGPT01ZE	—	GPTW0 and GPTW1 Output Disabling Condition POE0F Add
	IC2ADDGPT01ZE	—	GPTW0 and GPTW1 Output Disabling Condition POE4F Add
	IC3ADDGPT01ZE	—	GPTW0 and GPTW1 Output Disabling Condition POE8F Add
	IC4ADDGPT01ZE	—	GPTW0 and GPTW1 Output Disabling Condition POE10F Add
	IC5ADDGPT01ZE	—	GPTW0 and GPTW1 Output Disabling Condition POE11F Add
	IC6ADDGPT01ZE	—	GPTW0 and GPTW1 Output Disabling Condition POE12F Add
	IC8ADDGPT01ZE	—	GPTW0 and GPTW1 Output Disabling Condition POE9F Add
	IC9ADDGPT01ZE	—	GPTW0 and GPTW1 Output Disabling Condition POE13F Add
	IC10ADDGPT01ZE	—	GPTW0 and GPTW1 Output Disabling Condition POE14F Add
	CMADDGPT03ZE	GPT0 to GPT3 Output Disabling Condition CFLAG Add	—
	IC1ADDGPT03ZE	GPT0 to GPT3 Output Disabling Condition POE0F Add	—
	IC2ADDGPT03ZE	GPT0 to GPT3 Output Disabling Condition POE4F Add	—
	IC3ADDGPT03ZE	GPT0 to GPT3 Output Disabling Condition POE8F Add	—
	IC4ADDGPT03ZE	GPT0 to GPT3 Output Disabling Condition POE10F Add	—
	IC6ADDGPT03ZE	GPT0 to GPT3 Output Disabling Condition POE12F Add	—
POECR6B	—	—	Port Output Enable Control Register 6B
POECR7	MTU9A1ZE	MTIOC9A (P21) Pin High-Impedance Enable	—
	MTU9B1ZE	MTIOC9B (P10) Pin High-Impedance Enable	—
	MTU9C1ZE	MTIOC9C (P20) Pin High-Impedance Enable	—
	MTU9D1ZE	MTIOC9D (P02) Pin High-Impedance Enable	—
POECR8	IC6ADDMT9ZE	—	MTU9 Output Disabling Condition POE12F Add
	IC8ADDMT9ZE	—	MTU9 Output Disabling Condition POE9F Add
	IC9ADDMT9ZE	—	MTU9 Output Disabling Condition POE13F Add
	IC10ADDMT9ZE	—	MTU9 Output Disabling Condition POE14F Add

Register	Bit	RX24T(POE3b, POE3A)	RX66T(POE3B)
POECR9	—	—	Port Output Enable Control Register 9
POECR10	—	—	Port Output Enable Control Register 10
POECR11	—	—	Port Output Enable Control Register 11
PMMCR0	MTU0A1ME	MTIOC0A (P31) Pin Port Mode Mask Enable	—
	MTU0B1ME	MTIOC0B (P30) Pin Port Mode Mask Enable	—
	MTU9AME	—	MTIOC9A Pin Port Mode Mask Enable
	MTU9BME	—	MTIOC9B Pin Port Mode Mask Enable
	MTU9CME	—	MTIOC9C Pin Port Mode Mask Enable
	MTU9DME	—	MTIOC9D Pin Port Mode Mask Enable
PMMCR1	MTU4BME	MTIOC4B/GTIOC2A (P73) Pin Port Mode Mask Enable	MTIOC4B Pin Port Mode Mask Enable
	MTU4AME	MTIOC4A/GTIOC1A (P72) Pin Port Mode Mask Enable	MTIOC4A Pin Port Mode Mask Enable
	MTU3BME	MTIOC3B/GTIOC0A (P71) Pin Port Mode Mask Enable	MTIOC3B Pin Port Mode Mask Enable
	MTU4DME	MTIOC4D/GTIOC2B (P76) Pin Port Mode Mask Enable	MTIOC4D Pin Port Mode Mask Enable
	MTU4CME	MTIOC4C/GTIOC1B (P75) Pin Port Mode Mask Enable	MTIOC4C Pin Port Mode Mask Enable
	MTU3DME	MTIOC3D/GTIOC0B (P74) Pin Port Mode Mask Enable	MTIOC3D Pin Port Mode Mask Enable
PMMCR2	GPT0A1ME(RX24T) GPT0AME(RX66T)	GTIOC0A (PD2) Pin Port Mode Mask Enable (b8)	GTIOC0A Pin Port Mode Mask Enable (b0)
	GPT0B1ME(RX24T) GPT0BME(RX66T)	GTIOC0B (PD1) Pin Port Mode Mask Enable (b9)	GTIOC0B Pin Port Mode Mask Enable (b1)
	GPT1A1ME(RX24T) GPT1AME(RX66T)	GTIOC1A (PD0) Pin Port Mode Mask Enable (b10)	GTIOC1A Pin Port Mode Mask Enable (b2)
	GPT1B1ME(RX24T) GPT1BME(RX66T)	GTIOC1B (PB7) Pin Port Mode Mask Enable (b11)	GTIOC1B Pin Port Mode Mask Enable (b3)
	GPT2A1ME(RX24T) GPT2AME(RX66T)	GTIOC2A (PB6) Pin Port Mode Mask Enable (b12)	GTIOC2A Pin Port Mode Mask Enable (b4)
	GPT2B1ME(RX24T) GPT2BME(RX66T)	GTIOC2B (PB5) Pin Port Mode Mask Enable (b13)	GTIOC2B Pin Port Mode Mask Enable (b5)
	GPT3A1ME(RX24T) GPT3AME(RX66T)	GTIOC3A/MTIOC9A (PD7) Pin Port Mode Mask Enable (b14)	GTIOC3A Pin Port Mode Mask Enable (b6)
	GPT3B1ME(RX24T) GPT3BME(RX66T)	GTIOC3B/MTIOC9C (PD6) Pin Port Mode Mask Enable (b15)	GTIOC3B Pin Port Mode Mask Enable (b7)
	GPT4AME	—	GTIOC4A Pin Port Mode Mask Enable
	GPT4BME	—	GTIOC4B Pin Port Mode Mask Enable
	GPT5AME	—	GTIOC5A Pin Port Mode Mask Enable

Register	Bit	RX24T(POE3b, POE3A)	RX66T(POE3B)
PMMCR2	GPT5BME	—	GTIOC5B Pin Port Mode Mask Enable
	GPT6AME	—	GTIOC6A Pin Port Mode Mask Enable
	GPT6BME	—	GTIOC6B Pin Port Mode Mask Enable
	GPT7AME	—	GTIOC7A Pin Port Mode Mask Enable
	GPT7BME	—	GTIOC7B Pin Port Mode Mask Enable
PMMCR3	MTU9AME	MTIOC9A/GTIOC3A (PD7) Pin Port Mode Mask Enable	—
	MTU9BME	MTIOC9B (PE0) Pin Port Mode Mask Enable	—
	MTU9CME	MTIOC9C/GTIOC3B (PD6) Pin Port Mode Mask Enable	—
	MTU9DME	MTIOC9D (PE1) Pin Port Mode Mask Enable	—
	MTU9A1ME	MTIOC9A (P21) Pin Port Mode Mask Enable	—
	MTU9B1ME	MTIOC9B (P10) Pin Port Mode Mask Enable	—
	MTU9C1ME	MTIOC9C (P20) Pin Port Mode Mask Enable	—
	MTU9D1ME	MTIOC9D (P02) Pin Port Mode Mask Enable	—
	GPT8AME	—	GTIOC8A Pin Port Mode Mask Enable
	GPT8BME	—	GTIOC8B Pin Port Mode Mask Enable
	GPT9AME	—	GTIOC9A Pin Port Mode Mask Enable
	GPT9BME	—	GTIOC9B Pin Port Mode Mask Enable
POECMPFR	C4FLAG	—	Comparator Channel 4 Output Detection Flag
	C5FLAG	—	Comparator Channel 5 Output Detection Flag
POECMPSEL	POEREQ4	—	Comparator Channel 4 Output Disabling Request Enable
	POEREQ5	—	Comparator Channel 5 Output Disabling Request Enable
POECMPEXm	—	Port Output Enable Comparator Request Extended Selection Register m (m = 0 to 2, 4, 5)	Port Output Enable Comparator Request Extended Selection Register m (m = 0 to 8)
	POEREQ4	—	Comparator Channel 4 Output Disabling Request Enable
	POEREQ5	—	Comparator Channel 5 Output Disabling Request Enable

Note 1. Pins GPT and MTU are controlled by this register in RX24T, however, these pins are controlled by separate registers in RX66T.

2.16 General PWM Timer

Table 2.35 lists Comparison of Specifications for General PWM Timer and Table 2.36 lists Comparison of Registers for General PWM Timer.

Table 2.35 Comparison of Specifications for General PWM Timer

Item	RX24T(GPTB)	RX66T(GPTW)
Function	• Selectable from 16 bits × 4 channels, 16 bits × 2 channels + 32 bits × 1 channel, and 32 bits × 2 channels • Up-counting or down-counting (saw waves) or up/down-counting (triangle waves) for each counter. • Operating mode Saw-wave PWM mode Saw-wave one-shot pulse mode Triangle-wave PWM mode 1 Triangle-wave PWM mode 2 Triangle-wave PWM mode 3 • Clock sources (nine internal clocks and four external clocks) independently selectable for each channel • Two I/O pins per channel • Noise filter can be set on each input path. (Note 1) • Two output compare/input capture registers per channel • For the two output compare/input capture registers of each channel, four registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at crests or troughs, enabling the generation of laterally asymmetric PWM waveforms. • Registers for setting up frame cycles in each channel (with capability for generating interrupts at overflow or underflow) • Synchronous operation of the several counters • Synchronous operation modes: simultaneous start or phase shifting start by desired times • Generation of dead times in PWM operation	• 32 bits × 10 channels • Up-counting or down-counting (sawtooth waves) or up/down-counting (triangle waves) for each counter. • Operating mode Sawtooth-wave PWM mode Sawtooth-wave one-shot pulse mode Triangle-wave PWM mode 1 Triangle-wave PWM mode 2 Triangle-wave PWM mode 3 • Clock sources independently selectable for each channel • Two I/O pins per channel • Noise filter can be set on each input path. (Note 1) • Two output compare/input capture registers per channel • For the two output compare/input capture registers of each channel, four registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at crests or troughs, enabling the generation of laterally asymmetric PWM waveforms. • Registers for setting up frame cycles in each channel (with capability for generating interrupts at overflow or underflow) • Simultaneous start/stop/clearing of desired channel counters • Modes of synchronous operation (synchronized or displaced by a desired time to obtain relative phase shifts) • Generation of dead times in PWM operation

Item	RX24T(GPTB)	RX66T(GPTW)
Function	• Starting, clearing, and stopping counters in response to external or internal triggers (hardware sources) • Internal trigger sources: comparator output, MTU count start, software, and compare match	• Operation of count start/count stop/counter clearing/up-counting/down-counting/input capture by maximum of eight ELC events based on the ELC setting • Operation of count start/count stop/counter clearing/up-counting/down-counting/input capture by detecting two input signal conditions • Operation of count start/count stop/counter clearing/up-counting/down-counting/input capture by maximum of four external triggers • Function to control output negation by requests for disabling of output from the POEG
	• A/D converter start trigger generation function	• A/D converter start trigger generation function • Event signals for compare match A to F and for overflow/underflow can be output to the ELC • Input capture input can select noise filter function • Bus clock: PCLKA, GPTW count reference clock: PCLKC, Frequency ratio between PCLKA: PCLKC = 1: N (N = 1/2)
	• Through combination of three counters, generation of three-phase PWM waveforms incorporating dead times	• Through combination of three counters, generation of three-phase PWM waveforms incorporating dead times
	• Monitors the clock output from the main clock oscillator, low- and high-speed on-chip oscillators, the PLL frequency synthesizer, IWDT-dedicated on-chip oscillator, and PCLKB (refer to the Clock Frequency Accuracy Measurement Circuit (CAC) chapter.)	• Monitors the clock output from the main clock oscillator, low- and high-speed on-chip oscillators, the PLL frequency synthesizer, IWDT-dedicated on-chip oscillator, and PCLKB (refer to the Clock Frequency Accuracy Measurement Circuit (CAC) chapter.) • Capable of adjusting rising/falling timing at PWM waveforms with resolution of PCLKC cycles x 1/32 for maximum of 4 channels of complementary PWM output pins (refer to the High Resolution PWM Waveform Generation Circuit (HRPWM) chapter.)

Item		RX24T(GPTB)	RX66T(GPTW)
Synchronous operation	Target channels for synchronization	Synchronous operation is supported on channels 0 to 3.	Synchronous operation is supported on channels 0 to 9.
	Method of synchronous clear	Software source: Simultaneously setting multiple bits among GTHCCR.CCSW0 to GTHCCR.CCSW3 to 1. Hardware source: Bits GTSYNC.SYNCn[1:0] specify which channel's clear source is used as the synchronous clear source.	Software source: Simultaneously setting multiple bits in the GTCLR register to 1. Hardware source: The GTCSR register is used to set the synchronous clear source to the same clear source as the synchronous channels (either external trigger or ELC event input).
	Method of synchronous start	Software source: Simultaneously setting multiple bits in the GTSTR register to 1. Hardware source: The GTHSSR and GTHSCR registers are used to set the same start source as that of the channels on which synchronous operation will start (COMPC0/COMPC1/ COMPC2/COMPC3 comparator output, MTU0/MTU1/MTU2/MTU4/MTU7/MTU9 count start, GTIOC3A/GTIOC3B/ GTETRG pin input, or GTIOC3A/ GTIOC3B internal output (output compare)).	Software source: Simultaneously setting multiple bits in the GTSTR register to 1. Hardware source: The GTSSR register is used to set the same start source as that of the channels on which synchronous operation will start (either external trigger or ELC event input).
	Method of synchronous stop	Software source: Simultaneously setting multiple bits in the GTSTR register to 0. Hardware source: The GTHPSR and GTHSCR registers are used to set the same stop source as that of the channels on which synchronous operation will stop (COMPC0/COMPC1/COMPC2/COMPC3 comparator output, GTIOC3A/GTIOC3B/GTETRG pin input, or GTIOC3A/GTIOC3B internal output (output compare)).	Software source: Simultaneously setting multiple bits in the GTSTP register to 1. Hardware source: The GTPSR register is used to set the same stop source as that of the channels on which synchronous operation will stop (either external trigger or ELC event input).

Note 1. On the RX24T Group the input capture input pins, external trigger input pins, and external clock input pins, and on the RX66T Group the input capture input pins and external trigger input pins, have a noise filter function.

Table 2.36 Comparison of Registers for General PWM Timer

Register	Bit	RX24T(GPTB)	RX66T(GPTW)
GTSTR	CST0(RX24T) CSTRT0(RX66T)	GPT0.GTCNT Count Start	Channel 0 Count Start
	CST1(RX24T) CSTRT1(RX66T)	GPT1.GTCNT/GPT01.GTCNTLW Count Start	Channel 1 Count Start
	CST2(RX24T) CSTRT2(RX66T)	GPT2.GTCNT Count Start	Channel 2 Count Start
	CST3(RX24T) CSTRT3(RX66T)	GPT3.GTCNT/GPT23.GTCNTLW Count Start	Channel 3 Count Start
	CSTRT4 to CSTRT9	—	Channel 4 to 9 Count Start
NFCR	—	Noise Filter Control Register	—
GTHSCR	—	General PWM Timer Hardware Source Start/Stop Control Register	—
GTHCCR	—	General PWM Timer Hardware Source Clear Control Register	—
GTHSSR	—	General PWM Timer Hardware Start Source Select Register	—
GTHPSR	—	General PWM Timer Hardware Stop/Clear Source Select Register	—
GTWP	WP0 to WP3(RX24T) WP(RX66T)	GPT0, GPT1/GPT01, GPT2, GPT3/GPT23 Register Write Disable	Register Write Disabled
	STRWP	—	GTSTR.CSTRT Bit Write Disabled
	STPWP	—	GTSTP.CSTOP Bit Write Disabled
	CLRWP	—	GTCLR.CCLR Bit Write Disabled
	CMNWP	—	Common Register Write Disabled
	PRKEY[7:0]	—	GTWP Key Code
GTSYNC	—	General PWM Timer Sync Register	—
GTETINT	—	General PWM Timer External Trigger Input Interrupt Register	—
GTBDR	—	General PWM Timer Buffer Operation Disable Register	—
GTSWP	—	General PWM Timer Start Write-Protection Register	—
GTCWP	—	General PWM Timer Clearing Write-Protection Register	—
GTCMNWP	—	General PWM Timer Common Register Write-Protection Register	—
GTMDR	—	General PWM Timer Mode Register	—
GTECNFCR	—	General PWM Timer External Clock Noise Filter Control Register	—

Register	Bit	RX24T(GPTB)	RX66T(GPTW)
GTADSMR	ADSMS0[3:0](RX24T) ADSMS0[1:0](RX66T)	A/D Conversion Start Request Signal Monitor 0 Selection b3 b0 0 0 0 0: A/D conversion start request signal generated by the GPT0.GTADTRA register during up-counting 0 0 0 1: A/D conversion start request signal generated by the GPT0.GTADTRA register during down-counting 0 0 1 0: A/D conversion start request signal generated by the GPT0.GTADTRB register during up-counting 0 0 1 1: A/D conversion start request signal generated by the GPT0.GTADTRB register during down-counting 0 1 0 0: A/D conversion start request signal generated by the GPT1.GTADTRA/GPT01.GTADTRALW register during up-counting 0 1 0 1: A/D conversion start request signal generated by the GPT1.GTADTRA/GPT01.GTADTRALW register during down-counting 0 1 1 0: A/D conversion start request signal generated by the GPT1.GTADTRB/GPT01.GTADTRBLW register during up-counting 0 1 1 1: A/D conversion start request signal generated by the GPT1.GTADTRB/GPT01.GTADTRBLW register during down-counting 1 0 0 0: A/D conversion start request signal generated by the GPT2.GTADTRA register during up-counting 1 0 0 1: A/D conversion start request signal generated by the GPT2.GTADTRA register during down-counting 1 0 1 0: A/D conversion start request signal generated by the GPT2.GTADTRB register during up-counting	A/D Conversion Start Request Signal Monitor 0 Selection b1 b0 0 0: A/D conversion start request signal generated by the GTADTRA register during up-counting 0 1: A/D conversion start request signal generated by the GTADTRA register during down-counting 1 0: A/D conversion start request signal generated by the GTADTRB register during up-counting 1 1: A/D conversion start request signal generated by the GTADTRB register during down-counting

Register	Bit	RX24T(GPTB)	RX66T(GPTW)
GTADSMR	ADSMS0[3:0](RX24T) ADSMS0[1:0](RX66T)	1 0 1 1: A/D conversion start request signal generated by the GPT2.GTADTRB register during down-counting 1 1 0 0: A/D conversion start request signal generated by the GPT3.GTADTRA/GPT23.GTADTRALW register during up-counting 1 1 0 1: A/D conversion start request signal generated by the GPT3.GTADTRA/GPT23.GTADTRALW register during down-counting 1 1 1 0: A/D conversion start request signal generated by the GPT3.GTADTRB/GPT23.GTADTRBLW register during up-counting 1 1 1 1: A/D conversion start request signal generated by the GPT3.GTADTRB/GPT23.GTADTRBLW register during down-counting	

Register	Bit	RX24T(GPTB)	RX66T(GPTW)
GTADSMR	ADSMS1[3:0](RX24T) ADSMS1[1:0](RX66T)	A/D Conversion Start Request Signal Monitor 1 Selection b19 b16 0 0 0 0: A/D conversion start request signal generated by the GPT0.GTADTRA register during up-counting 0 0 0 1: A/D conversion start request signal generated by the GPT0.GTADTRA register during down-counting 0 0 1 0: A/D conversion start request signal generated by the GPT0.GTADTRB register during up-counting 0 0 1 1: A/D conversion start request signal generated by the GPT0.GTADTRB register during down-counting 0 1 0 0: A/D conversion start request signal generated by the GPT1.GTADTRA/GPT01.GTADTRALW register during up-counting 0 1 0 1: A/D conversion start request signal generated by the GPT1.GTADTRA/GPT01.GTADTRALW register during down-counting 0 1 1 0: A/D conversion start request signal generated by the GPT1.GTADTRB/GPT01.GTADTRBLW register during up-counting 0 1 1 1: A/D conversion start request signal generated by the GPT1.GTADTRB/GPT01.GTADTRBLW register during down-counting 1 0 0 0: A/D conversion start request signal generated by the GPT2.GTADTRA register during up-counting 1 0 0 1: A/D conversion start request signal generated by the GPT2.GTADTRA register during down-counting 1 0 1 0: A/D conversion start request signal generated by the GPT2.GTADTRB register during up-counting	A/D Conversion Start Request Signal Monitor 1 Selection b17 b16 0 0: A/D conversion start request signal generated by the GTADTRA register during up-counting 0 1: A/D conversion start request signal generated by the GTADTRA register during down-counting 1 0: A/D conversion start request signal generated by the GTADTRB register during up-counting 1 1: A/D conversion start request signal generated by the GTADTRB register during down-counting

Register	Bit	RX24T(GPTB)	RX66T(GPTW)
GTADSMR	ADSMS1[3:0](RX24T) ADSMS1[1:0](RX66T)	1 0 1 1: A/D conversion start request signal generated by the GPT2.GTADTRB register during down-counting 1 1 0 0: A/D conversion start request signal generated by the GPT3.GTADTRA/GPT23.GTADTRALW register during up-counting 1 1 0 1: A/D conversion start request signal generated by the GPT3.GTADTRA/GPT23.GTADTRALW register during down-counting 1 1 1 0: A/D conversion start request signal generated by the GPT3.GTADTRB/GPT23.GTADTRBLW register during up-counting 1 1 1 1: A/D conversion start request signal generated by the GPT3.GTADTRB/GPT23.GTADTRBLW register during down-counting	
GTIOR	GTIOA[5:0](RX24T) GTIOA[4:0](RX66T)	GTIOCnA Pin Function Select (b5 to b0) Refer to the User's Manual: Hardware for details.	GTIOCnA Pin Function Select (b4 to b0) Refer to the User's Manual: Hardware for details.
	OAE	—	GTIOCnA Pin Output Enable
	OADF[1:0]	—	GTIOCnA Pin Negate Value Setting
	NFAEN	—	GTIOCnA Pin Input Noise Filter Enable
	NFCSA[1:0]	—	GTIOCnA Pin Input Noise Filter Sampling Clock Select
	GTIOB[5:0](RX24T) GTIOB[4:0](RX66T)	GTIOCnB Pin Function Select (b13 to b8) Refer to the User's Manual: Hardware for details.	GTIOCnB Pin Function Select (b20 to b16) Refer to the User's Manual: Hardware for details.
	OBDFLT	GTIOCnB Pin Output Value Setting at the Count Stop (b14)	GTIOCnB Pin Output Value Setting at the Count Stop (b22)
	OBHLD	GTIOCnB Pin Output Setting at the Start/Stop Count (b15)	GTIOCnB Pin Output Retention at the Start/Stop Count (b23)
	OBE	—	GTIOCnB Pin Output Enable
	OBDF[1:0]	—	GTIOCnB Pin Negate Value Setting

Register	Bit	RX24T(GPTB)	RX66T(GPTW)
GTIOR	NFBEN	—	GTIOCnB Pin Input Noise Filter Enable
	NFCSB[1:0]	—	GTIOCnB Pin Input Noise Filter Sampling Clock Select
GTCR	CST	—	Count Start
	ICDS	—	Input Capture Operation Select at Count Stop
	MD[2:0]	Mode Select (b2 to b0) b2 b0 0 0 0: Saw-wave PWM mode (single buffer or double buffer possible) 0 0 1: Saw-wave one-shot pulse mode (fixed buffer operation) 0 1 0: Setting prohibited 0 1 1: Setting prohibited 1 0 0: Triangle-wave PWM mode 1 (16-bit transfer at crest) (single buffer or double buffer possible) 1 0 1: Triangle-wave PWM mode 2 (16-bit transfer at crest and trough) (single buffer or double buffer possible) 1 1 0: Triangle-wave PWM mode 3 (32-bit transfer at trough) fixed buffer operation) 1 1 1: Setting prohibited	Mode Select (b18 to b16) b18 b16 0 0 0: Sawtooth-wave PWM mode (single buffer or double buffer possible) 0 0 1: Sawtooth-wave one-shot pulse mode (fixed buffer operation) 0 1 0: Setting prohibited 0 1 1: Setting prohibited 1 0 0: Triangle-wave PWM mode 1 (32-bit transfer at trough) (single buffer or double buffer possible) 1 0 1: Triangle-wave PWM mode 2 (32-bit transfer at crest and trough) (single buffer or double buffer possible) 1 1 0: Triangle-wave PWM mode 3 (64-bit transfer at trough) (fixed buffer operation) 1 1 1: Setting prohibited

Register	Bit	RX24T(GPTB)	RX66T(GPTW)
GTCR	TPCS[3:0]	Timer Prescaler Select (b11 to b8) b11 b8 0 0 0 0: PCLKA 0 0 0 1: PCLKA/2 0 0 1 0: PCLKA/4 0 0 1 1: PCLKA/8 0 1 0 0: PCLKA/16 0 1 0 1: PCLKA/32 0 1 1 0: PCLKA/64 0 1 1 1: PCLKA/256 1 0 0 0: PCLKA/1024 1 0 0 1: Setting prohibited 1 0 1 0: Setting prohibited 1 0 1 1: Setting prohibited 1 1 0 0: GTECLKA 1 1 0 1: GTECLKB 1 1 1 0: GTECLKC 1 1 1 1: GTECLKD	Timer Prescaler Select (b26 to b23) b26 b23 0 0 0 0: PCLKC 0 0 0 1: PCLKC/2 0 0 1 0: PCLKC/4 0 0 1 1: PCLKC/8 0 1 0 0: PCLKC/16 0 1 0 1: PCLKC/32 0 1 1 0: PCLKC/64 0 1 1 1: Setting prohibited 1 0 0 0: PCLKC/256 1 0 0 1: Setting prohibited 1 0 1 0: PCLKC/1024 1 0 1 1: Setting prohibited 1 1 0 0: GTETRGA (via the POEG) 1 1 0 1: GTETRGB (via the POEG) 1 1 1 0: GTETRGC (via the POEG) 1 1 1 1: GTETRGD (via the POEG)
	CCLR[1:0]	Counter Clear Source Select	—
GTINTAD	EINT	Dead Time Error Interrupt Enable	—
	ADTRAUEN	GTADTRA(LW) Compare Match (Up-Counting) A/D Converter Start Request Enable (b12)	GTADTRA Register Compare Match (Up-Counting) A/D Converter Start Request Enable (b16)
	ADTRADEN	GTADTRA(LW) Compare Match (Down-Counting) A/D Converter Start Request Enable (b13)	GTADTRA Register Compare Match (Down-Counting) A/D Converter Start Request Enable (b17)
	ADTRBUEN	GTADTRB(LW) Compare Match (Up-Counting) A/D Converter Start Request Enable (b14)	GTADTRB Register Compare Match (Up-Counting) A/D Converter Start Request Enable (b18)
	ADTRBDEN	GTADTRB(LW) Compare Match (Down-Counting) A/D Converter Start Request Enable (b15)	GTADTRB Register Compare Match (Down-Counting) A/D Converter Start Request Enable (b19)
	GRP[1:0]	—	Output Stop Group Select
	GRPDTE	—	Dead Time Error Output Stop Detection Enable
	GRPABH	—	Simultaneous High Output Stop Detection Enable
	GRPABL	—	Simultaneous Low Output Stop Detection Enable
GTBER	BD[0]	—	GTCCRA/GTCCRB Registers Buffer Operation Disable
	BD[1]	—	GTPR Register Buffer Operation Disable
	BD[2]	—	GTADTRA/GTADTRB Registers Buffer Operation Disable

Register	Bit	RX24T(GPTB)	RX66T(GPTW)
GTBER	BD[3]	—	GTDVU/GTDVD Registers Buffer Operation Disable
	DBRTECA	—	GTCCRA Register Double Buffer Repeat Operation Enable
	DBRTECB	—	GTCCRB Register Double Buffer Repeat Operation Enable
	CCRA[1:0]	GTCCRA(LW) Buffer Operation (b1 to b0)	GTCCRA Register Buffer Operation (b17 to b16)
	CCRB[1:0]	GTCCRB(LW) Buffer Operation (b3 to b2)	GTCCRB Register Buffer Operation (b19 to b18)
	PR[1:0]	GTPR(LW) Buffer Operation (b5 to b4)	GTPR Register Buffer Operation (b21 to b20)
	CCRSWT	GTCCRA(LW) and GTCCRB(LW) Forcible Buffer Operation (b6)	GTCCRA and GTCCRB Registers Forcible Buffer Operation (b22)
	ADTTA[1:0]	GTADTRA(LW) Buffer Transfer Timing Select (b9 to b8)	GTADTRA Register Buffer Transfer Timing Select (b25 to b24)
	ADTDA	GTADTRA(LW) Double Buffer Operation (b10)	GTADTRA Register Double Buffer Operation (b26)
	ADTTB[1:0]	GTADTRB(LW) Buffer Transfer Timing Select (b13 to b12)	GTADTRB Register Buffer Transfer Timing Select (b29 to b28)
	ADTDB	GTADTRB(LW) Double Buffer Operation (b14)	GTADTRB Register Double Buffer Operation (b30)
GTUDC	—	General PWM Timer Count Direction Register	—
GTST	DTEF	Dead Time Error Flag (b11)	Dead Time Error Flag (b28)
	ADTRAUF	—	GTADTRA Register Compare Match (Up-Counting) A/D Converter Start Request Flag
	ADTRADF	—	GTADTRA Register Compare Match (Down-Counting) A/D Converter Start Request Flag
	ADTRBUF	—	GTADTRB Register Compare Match (Up-Counting) A/D Converter Start Request Flag
	ADTRBDF	—	GTADTRB Register Compare Match (Down-Counting) A/D Converter Start Request Flag
	ODF	—	Output Stop Request Flag
	OABHF	—	Simultaneous High Output Flag
	OABLF	—	Simultaneous Low Output Flag
GTCNT	—	General PWM Timer Counter The GTCNT counter is a 16-bit readable/writable counter. Access in 8-bit units to the GTCNT counter is prohibited, and it should be accessed in 16-bit units.	General PWM Timer Counter The GTCNT counter is a 32-bit readable/writable counter. Access in 8-bit or 16-bit units to the GTCNT counter is prohibited, and it should be accessed in 32-bit units. Set the range of the GTCNT counter within the range of 0 ≤ GTCNT counter ≤ GTPR register.

Register	Bit	RX24T(GPTB)	RX66T(GPTW)
GTCNTLW	—	General PWM Timer Longword Counter	—
GTCCRm	—	General PWM Timer Compare Capture Register m (m = A to F) The GTCCRm registers are 16-bit readable/writable registers.	General PWM Timer Compare Capture Register m (m = A to F) The GTCCRm register is a 32-bit readable/writable register. Access in 8-bit or 16-bit units to the GTCCRm register is prohibited, and it should be accessed in 32-bit units.
GTCCRmLW	—	General PWM Timer Longword Compare Capture Register m (m = A to F)	—
GTPR	—	General PWM Timer Period Setting Register The GTPR register is a 16-bit readable/writable register.	General PWM Timer Period Setting Register The GTPR register is a 32-bit readable/writable register. Access in 8-bit or 16-bit units to the GTPR register is prohibited, and it should be accessed in 32-bit units.
GTPRLW	—	General PWM Timer Longword Period Setting Register	—
GTPBR	—	General PWM Timer Period Setting Buffer Register The GTPBR register is a 16-bit readable/writable register.	General PWM Timer Period Setting Buffer Register The GTPBR register is a 32-bit readable/writable register. Access in 8-bit or 16-bit units to the GTPBR register is prohibited, and it should be accessed in 32-bit units.
GTPBRLW	—	General PWM Timer Longword Period Setting Buffer Register	—
GTPDBR	—	General PWM Timer Period Setting Double Buffer Register The GTPDBR register is a 16-bit readable/writable register.	General PWM Timer Period Setting Double-Buffer Register The GTPDBR register is a 32-bit readable/writable register. Access in 8-bit or 16-bit units to the GTPDBR register is prohibited, and it should be accessed in 32-bit units.
GTPDBRLW	—	General PWM Timer Longword Period Setting Double Buffer Register	—

Register	Bit	RX24T(GPTB)	RX66T(GPTW)
GTADTRm	—	A/D Converter Start Request Timing Register m (m = A, B) The GTADTRm registers are 16-bit readable/writable registers. Access in 8-bit units to the GTADTRm registers is prohibited, and they should be accessed in 16-bit units.	A/D Converter Start Request Timing Register m (m = A, B) The GTADTRm register is 32-bit readable/writable register. Access in 8-bit or 16-bit units to the GTADTRm register is prohibited, and it should be accessed in 32-bit units.
GTADTRmLW	—	Longword A/D Converter Start Request Timing Register m (m = A, B)	—
GTADTBRm	—	A/D Converter Start Request Timing Buffer Register m (m = A, B) The GTADTBRm registers are 16-bit readable/writable registers. Access in 8-bit units to the GTADTBRm registers is prohibited, and they should be accessed in 16-bit units.	A/D Converter Start Request Timing Buffer Register m (m = A, B) The GTADTBRm register is 32-bit readable/writable register. Access in 8-bit or 16-bit units to the GTADTBRm register is prohibited, and it should be accessed in 32-bit units.
GTADTBRmLW	—	Longword A/D Converter Start Request Timing Buffer Register m (m = A, B)	—
GTADTDBRm	—	A/D Converter Start Request Timing Double Buffer Register m (m = A, B) The GTADTDBRm registers are 16-bit readable/writable registers. Access in 8-bit units to the GTADTDBRm registers is prohibited, and they should be accessed in 16-bit units.	A/D Converter Start Request Timing Double-Buffer Register m (m = A, B) The GTADTDBRm register is 32-bit readable/writable register. Access in 8-bit or 16-bit units to the GTADTDBRm register is prohibited, and it should be accessed in 32-bit units.
GTADTDBRmLW	—	Longword A/D Converter Start Request Timing Double Buffer Register m (m = A, B)	—
GTONCR	—	General PWM Timer Output Negate Control Register	—
GTDVm	—	General PWM Timer Dead Time Value Register m (m = U, D) The GTDVm registers are 16-bit readable/writable registers. Access in 8-bit units to the GTDVm registers is prohibited, and they should be accessed in 16-bit units.	General PWM Timer Dead Time Value Register m (m = U, D) The GTDVm register is 32-bit readable/writable register Access in 8-bit or 16-bit units to the GTDVm register is prohibited, and it should be accessed in 32-bit units.
GTDVmLW	—	General PWM Timer Longword Dead Time Value Register m	—

Register	Bit	RX24T(GPTB)	RX66T(GPTW)
GTDBm	—	General PWM Timer Dead Time Buffer Register m (m = U, D) The GTDBm registers are 16-bit readable/writable registers.	General PWM Timer Dead Time Value Buffer Register m (m = U, D) The GTDBm register is 32-bit readable/writable register. Access in 8-bit or 16-bit units to the GTDBm register is prohibited, and it should be accessed in 32-bit units.
GTDBmLW	—	General PWM Timer Longword Dead Time Buffer Register m (m = U, D)	—
GTSTP	—	—	General PWM Timer Software Stop Register
GTCLR	—	—	General PWM Timer Software Clear Register
GTSSR	—	—	General PWM Timer Start Source Select Register
GTPSR	—	—	General PWM Timer Stop Source Select Register
GTCSR	—	—	General PWM Timer Clear Source Select Register
GTUPSR	—	—	General PWM Timer Count-Up Source Select Register
GTDNSR	—	—	General PWM Timer Count-Down Source Select Register
GTICASR	—	—	General PWM Timer Input Capture Source Select Register A
GTICBSR	—	—	General PWM Timer Input Capture Source Select Register B
GTUDDTYC	—	—	General PWM Timer Count Direction and Duty Setting Register
GTEITC	—	—	General PWM Timer Extended Interrupt Skipping Counter Control Register
GTEITLI1	—	—	General PWM Timer Extended Interrupt Skipping Setting Register 1
GTEITLI2	—	—	General PWM Timer Extended Interrupt Skipping Setting Register 2
GTEITLB	—	—	General PWM Timer Extended Buffer Transfer Skipping Setting Register
GTSECSR	—	—	General PWM Timer Operation Enable Bit Simultaneous Control Channel Select Register
GTSECR	—	—	General PWM Timer Operation Enable Bit Simultaneous Control Register

2.17 8-Bit Timer

Table 2.37 lists Comparison of Specifications for 8-Bit Timer and Table 2.38 lists Comparison of Registers for 8-Bit Timer.

Table 2.37 Comparison of Specifications for 8-Bit Timer

Item	RX24T(TMR)	RX66T(TMR)
Count clock	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192 • External clock: external count clock	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192 • External clock: external count clock
Number of channels	(8 bits × 2 channels) × 4 units	(8 bits × 2 channels) × 4 units
Compare match	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)
Counter clear	Selected by compare match A or B, or an external counter reset signal.	Selected by compare match A or B, or an external counter reset signal.
Timer output	Output pulses with a desired duty cycle or PWM output	Output pulses with a desired duty cycle or PWM output
Cascading of two channels	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits, TMR4 for the upper 8 bits and TMR5 for the lower 8 bits, TMR6 for the upper 8 bits and TMR7 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches, TMR5 can be used to count TMR4 compare matches, TMR7 can be used to count TMR6 compare matches).	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits, TMR4 for the upper 8 bits and TMR5 for the lower 8 bits, TMR6 for the upper 8 bits and TMR7 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches, TMR5 can be used to count TMR4 compare matches, TMR7 can be used to count TMR6 compare matches).
Interrupt sources	Compare match A, compare match B, and overflow	Compare match A, compare match B, and overflow
Event link function (Output)	—	Compare match A, compare match B, and overflow (TMR0 to TMR3)
Event link function (Input)	—	One of the following three operations proceeds in response to an event reception: (1) Counting start operation (TMR0 to TMR3) (2) Event counting operation (TMR0 to TMR3) (3) Counting restart operation (TMR0 to TMR3)
DTC activation	DTC can be activated by compare match A interrupts or compare match B interrupts.	DTC can be activated by compare match A interrupts or compare match B interrupts.
A/D conversion start trigger of the A/D converter	Compare match A of TMR0, TMR2, TMR4, and TMR6	Compare match A of TMR0, TMR2, TMR4, and TMR6
Capable of generating baud rate clock for SCI	Generates baud rate clock for SCI.	Generates baud rate clock for SCI.
Low power consumption function	Each unit can be placed in a module stop state	Each unit can be placed in a module stop state

Table 2.38 Comparison of Registers for 8-Bit Timer

Register	Bit	RX24T(TMR)	RX66T(TMR)
TCSTR	—	—	Timer Counter Start Register

2.18 Compare Match Timer

Table 2.39 lists Comparison of Specifications for Compare Match Timer.

Table 2.39 Comparison of Specifications for Compare Match Timer

Item	RX24T(CMT)	RX66T(CMT)
Count clocks	• Four frequency dividing clocks One clock from PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected for each channel.	• Four frequency dividing clocks One clock from PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected for each channel.
Interrupt	A compare match interrupt can be requested for each channel.	A compare match interrupt can be requested for each channel.
Event link function (output)	—	An event signal is output upon a CMT1 compare match.
Event link function (input)	—	• Linking to the specified module is possible. • CMT1 count start, event counter, or count restart operation is possible.
Low power consumption function	Each unit can be placed in a module stop state.	Each unit can be placed in a module stop state.

2.19 Independent Watchdog Timer

Table 2.40 lists Comparison of Specifications for Independent Watchdog Timer and Table 2.41 lists Comparison of Registers for Independent Watchdog Timer.

Table 2.40 Comparison of Specifications for Independent Watchdog Timer

Item	RX24T(IWDTa)	RX66T(IWDTa)
Count source	IWDT-dedicated clock (IWDTCLK)	IWDT-dedicated clock (IWDTCLK)
Clock divide ratio	Divide by 1, 16, 32, 64, 128, or 256	Divide by 1, 16, 32, 64, 128, or 256
Counter operation	Counting down using a 14-bit down-counter	Counting down using a 14-bit down-counter
Conditions for starting the counter	• Counting automatically starts after a reset (auto-start mode) • Counting is started (register start mode) by refreshing the counter (writing 00h and then FFh to the IWDTRR register).	• Auto-start mode: Counting automatically starts after a reset is released • Register start mode: Counting is started by refresh operation (writing 00h and then FFh to the IWDTRR register).
Conditions for stopping the counter	• Reset (the down-counter and other registers return to their initial values) • In low power consumption states (depends on the register setting) • A counter underflows or a refresh error occurs Counting restarts (In auto-start mode, counting automatically restarts after a reset or after a non-maskable interrupt request is output. In register start mode, counting restarts after refreshing.)	• Reset (the down-counter and other registers return to their initial values) • In low power consumption states (depends on the register setting) • A counter underflows or a refresh error occurs (only in register start mode)
Window function	• Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)	• Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Reset output sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Non-maskable interrupt/ interrupt sources	• A non-maskable interrupt is generated by an underflow of the down-counter. • Refreshing outside the refresh-permitted period (refresh error)	• A non-maskable interrupt or interrupt (WUNI) is generated by an underflow of the down-counter. • Refreshing outside the refresh-permitted period (refresh error)
Reading the counter value	The down-counter value can be read by the IWDTSR register.	The down-counter value can be read by the IWDTSR register.
Output signal (internal signal)	• Reset output • Interrupt request output • Sleep mode count stop control output	• Reset output • Interrupt request output • Sleep mode count stop control output
Event link function (output)	—	• Down-counter underflow event output • Refresh error event output

Item	RX24T(IWDTa)	RX66T(IWDTa)
Auto-start mode (controlled by option function select register 0 (OFS0))	• Selecting the clock frequency divide ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting the reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, or deep sleep mode (OFS0.IWDTSLCSTP bit)	• Selecting the clock frequency divide ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting the reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (OFS0.IWDTSLCSTP bit)
Register start mode (controlled by the IWDT registers)	• Selecting the clock frequency divide ratio after refreshing (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting the reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, or deep sleep mode (IWDTCSTPR.SLCSTP bit)	• Selecting the clock frequency divide ratio after refreshing (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting the reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (IWDTCSTPR.SLCSTP bit)

Table 2.41 Comparison of Registers for Independent Watchdog Timer

Register	Bit	RX24T(IWDTa)	RX66T(IWDTa)
IWDTCR	TOPS[1:0]	Timeout Period Select b1 b0 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1024 cycles (03FFh) 1 1: 2048 cycles (07FFh)	Timeout Period Select b1 b0 0 0: 1024 cycles (03FFh) 0 1: 4096 cycles (0FFFh) 1 0: 8192 cycles (1FFFh) 1 1: 16384 cycles (3FFFh)
IWDTRCR	RSTIRQS	Reset Interrupt Request Select 0: Non-maskable interrupt request output is enabled. 1: Reset output is enabled.	Reset Interrupt Request Select 0: Non-maskable interrupt request or interrupt request output is enabled. (Note 1) 1: Reset output is enabled.
IWDTCSTPR	SLCSTP	Sleep Mode Count Stop Control 0: Count stop is disabled. 1: Count is stopped at a transition to sleep mode, software standby mode, or deep sleep mode.	Sleep Mode Count Stop Control 0: Count stop is disabled. 1: Count is stopped at a transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode.

Note 1. When the value of the NMIER.IWDTEN bit is 1 non-maskable interrupts, and when it is 0 maskable interrupts, are generated.

2.20 Serial Communications Interface

Table 2.42 lists Comparison of Specifications for Serial Communications Interface, Table 2.43 lists Comparison of Channels in Serial Communications Interface and Table 2.44 lists Comparison of Registers for Serial Communications Interface.

Table 2.42 Comparison of Specifications for Serial Communications Interface

Item		RX24T(SCIg)	RX66T(SCIj, SCIi, SCIh)
Serial communications mode		• Asynchronous • Clock synchronous • Smart card interface • Simple I²C-bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C-bus • Simple SPI bus
Transfer speed		Bit rate specifiable with the on-chip baud rate generator.	Bit rate specifiable with the on-chip baud rate generator.
Full-duplex communications		• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.
Data transfer		Selectable as LSB first or MSB first transfer	Selectable as LSB first or MSB first transfer
Interrupt sources		• Transmit end, transmit data empty, receive data full, and receive error • Completion of generation of a start condition, restart condition, or stop condition (for simple I2C mode)	• Transmit end, transmit data empty, receive data full, receive error, receive data ready (SCI11), and data match (SCI1, SCI5, SCI6, SCI8, SCI9, SCI11) • Completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)
Low power consumption function		Module stop state can be set for each channel.	Module stop state can be set for each channel.
Asynchronous mode	Data length	7, 8, or 9 bits	7, 8, or 9 bits
	Transmission stop bit	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/ reception
	Transmit/receive FIFO	—	16-stage FIFOs for transmit and receive buffers (SCI11)
	Data match detection	—	Compares receive data and comparison data, and generates interrupt when they are matched (SCI1, SCI5, SCI6, SCI8, SCI9, SCI11)
	Start-bit detection	Low level or falling edge is selectable.	Low level or falling edge is selectable.
	Break detection	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly or reading the SPTR.RXDMON flag.

Item		RX24T(SCIg)	RX66T(SCIj, SCIi, SCIh)
Asynchronous mode	Clock source	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used. (SCI5, SCI6)	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used. (SCI5, SCI6, SCI12)
	Double-speed mode	Baud rate generator double-speed mode is selectable.	Baud rate generator double-speed mode is selectable.
	Multi-processor communications function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate digital noise filters.	The signal paths from input on the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Transmit/receive FIFO	—	16-stage FIFOs for transmit and receive buffers (SCI11)
Smart card interface mode	Error processing	• An error signal can be automatically transmitted when detecting a parity error during reception • Data can be automatically retransmitted when receiving an error signal during transmission	• An error signal can be automatically transmitted when detecting a parity error during reception • Data can be automatically retransmitted when receiving an error signal during transmission
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.
Simple I^2C mode	Transfer format	I^2C-bus format	I^2C-bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer rate	Fast mode is supported (refer to Bit Rate Register (BRR) to set the transfer rate)	Fast mode is supported (refer to Bit Rate Register (BRR) to set the transfer rate)
	Noise cancellation	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.
Simple SPI bus	Data length	8 bits	8 bits
	Detection of errors	Overrun error	Overrun error
	SS input pin function	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.
	Clock settings	Four kinds of settings for clock phase and clock polarity are selectable.	Four kinds of settings for clock phase and clock polarity are selectable.
Event link function (supported by SCI5 only)		—	Error (receive error or error signal detection) event output
		—	Receive data full event output
		—	Transmit data empty event output
		—	Transmit end event output

Item		RX24T(SCIg)	RX66T(SCIj, SCIi, SCIh)
Extended serial mode (supported by SCI 12 only)	Start Frame transmission	—	• Output of a low level as the Break Field over a specified width and generation of interrupts on completion • Detection of bus collisions and the generation of interrupts on detection • Detection of the Break Field low width and generation of an interrupt on detection • Comparison of Control Fields 0 and 1 and generation of an interrupt when the two match • Two kinds of data for comparison (primary and secondary) can be set in Control Field 1. • A priority interrupt bit can be set in Control Field 1. • Handling of Start Frames that do not include a Break Field • Handling of Start Frames that do not include a Control Field 0 • Function for measuring bit rates
	I/O control function	—	• Selectable polarity for TXDX12 and RXDX12 signals • Selection of a digital filter for the RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Selectable timing for the sampling of data received through RXDX12
	Timer function	—	Usable as a reloading timer
Bit rate modulation function		Correction of outputs from the on-chip baud rate generator can reduce errors.	Correction of outputs from the on-chip baud rate generator can reduce errors.

Table 2.43 Comparison of Channels in Serial Communications Interface

Item	RX24T(SCIg)	RX66T(SCIj, SCIi, SCIh)
Asynchronous mode	SCI1, SCI5, SCI6	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11, SCI12
Clock synchronous mode	SCI1, SCI5, SCI6	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11, SCI12
Smart card interface mode	SCI1, SCI5, SCI6	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11, SCI12
Simple I^2C mode	SCI1, SCI5, SCI6	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11, SCI12
Simple SPI mode	SCI1, SCI5, SCI6	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11, SCI12
FIFO mode	—	SCI11
Data match detection	—	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11
Extended serial mode	—	SCI12
TMR clock input	SCI5, SCI6	SCI5, SCI6, SCI12
Event link function	—	SCI5
Peripheral module clock	PCLKB	PCLKB : SCI1, SCI5, SCI6, SCI8, SCI9, SCI12 PCLKA : SCI11

Table 2.44 Comparison of Registers for Serial Communications Interface

Register	Bit	RX24T(SCIg)	RX66T(SCIj,SCIi,SCIh)
FRDR	—	—	Receive FIFO Data Register
FTDR	—	—	Transmit FIFO Data Register
SCR	CKE[1:0]	Clock Enable When SCMR.SMIF = 0 ● For SCI1 Asynchronous mode: b1 b0 0 0: On-chip baud rate generator The SCKn pin functions as I/O port. 0 1: On-chip baud rate generator The clock with the same frequency as the bit rate is output from the SCKn pin. 1 x: External clock The clock with a frequency 16 times the bit rate should be input from the SCKn pin. Input a clock signal with a frequency eight times the bit rate when the SEMR.ABCS bit is 1. Clock synchronous mode: b1 b0 0 x: Internal clock The SCKn pin functions as the clock output pin. 1 x: External clock The SCKn pin functions as the clock input pin. ● For SCI5 and SCI6 Asynchronous mode: b1 b0 0 0: On-chip baud rate generator The SCKn pin is available for use as an I/O port according to the I/O port settings. 0 1: On-chip baud rate generator The clock with the same frequency as the bit rate is output from the SCKn pin. 1 x: External clock or TMR clock - The clock with a frequency 16 times the bit rate should be input from the SCKn pin. Input a clock signal with a frequency eight times the bit rate when the SEMR.ABCS bit is 1. - The TMR clock can be used. The SCKn pin is available for use as an I/O port according to the I/O port settings when the TMR clock is used. Clock synchronous mode: b1 b0 0 x: Internal clock The SCKn pin functions as the clock output pin. 1 x: External clock The SCKn pin functions as the clock input pin.	Clock Enable When SCMR.SMIF = 0 ● For SCI1, SCI8, SCI9, and SCI11 Asynchronous mode: b1 b0 0 0: On-chip baud rate generator The SCKn pin becomes high-impedance. 0 1: On-chip baud rate generator The clock with the same frequency as the bit rate is output from the SCKn pin. 1 x: External clock The clock with a frequency 16 times the bit rate should be input from the SCKn pin. Input a clock signal with a frequency eight times the bit rate when the SEMR.ABCS bit is 1. Clock synchronous mode: b1 b0 0 x: Internal clock The SCKn pin functions as the clock output pin. 1 x: External clock The SCKn pin functions as the clock input pin. ● For SCI5, SCI6, and SCI12 Asynchronous mode: b1 b0 0 0: On-chip baud rate generator The SCKn pin becomes high-impedance. 0 1: On-chip baud rate generator The clock with the same frequency as the bit rate is output from the SCKn pin. 1 x: External clock or TMR clock - The clock with a frequency 16 times the bit rate should be input from the SCKn pin. Input a clock signal with a frequency eight times the bit rate when the SEMR.ABCS bit is 1. - The SCKn pin becomes high-impedance when the TMR clock is used. Clock synchronous mode: b1 b0 0 x: Internal clock The SCKn pin functions as the clock output pin. 1 x: External clock The SCKn pin functions as the clock input pin.

Register	Bit	RX24T(SCIg)	RX66T(SCIj,SCIi,SCIh)
SCR	CKE[1:0]	When SCMR.SMIF = 1 ● When SMR.GM = 0 b1 b0 0 0: Output disabled The SCKn pin is available for use as an I/O port according to the I/O port settings. 0 1: Clock output 1 x: Setting prohibited ● When SMR.GM = 1 b1 b0 0 0: Output fixed low x 1: Clock output 1 0: Output fixed high	When SCMR.SMIF = 1 ● When SMR.GM = 0 b1 b0 0 0: Output disabled The SCKn pin becomes high-impedance. 0 1: Clock output 1 x: Setting prohibited ● When SMR.GM = 1 b1 b0 0 0: Output fixed low x 1: Clock output 1 0: Output fixed high
SSR (When SCMR.SMIF = 0, FCR.FM = 1)	DR	—	Receive Data Ready Flag
	TEND	—	Transmit End Flag
	PER	—	Parity Error Flag
	FER	—	Framing Error Flag
	ORER	—	Overrun Error Flag
	RDF	—	Receive FIFO Full Flag
	TDFE	—	Transmit FIFO Empty Flag
SSRFIFO	—	—	Serial Status Register
SEMR	ACS0	Asynchronous Mode Clock Source Select (Valid only in asynchronous mode) 0: External clock input 1: Logical AND of two compare matches output from TMR (valid for SCI5 and SCI6 only) Available compare match output varies per SCI channel.	Asynchronous Mode Clock Source Select (Valid only in asynchronous mode) 0: External clock input 1: Logical AND of two compare matches output from TMR (valid for SCI5, SCI6, and SCI12 only) Available compare match output varies per SCI channel.
	ABCSE	—	Asynchronous Mode Base Clock Select Extended
FCR	—	—	FIFO Control Register
FDR	—	—	FIFO Data Count Register
LSR	—	—	Line Status Register
CDR	—	—	Comparison Data Register
DCCR	—	—	Data Comparison Control Register
SPTR	—	—	Serial Port Register
ESMER	—	—	Extended Serial Module Enable Register
CR0	—	—	Control Register 0
CR1	—	—	Control Register 1
CR2	—	—	Control Register 2
CR3	—	—	Control Register 3
PCR	—	—	Port Control Register
ICR	—	—	Interrupt Control Register
STR	—	—	Status Register
STCR	—	—	Status Clear Register
CF0DR	—	—	Control Field 0 Data Register
CF0CR	—	—	Control Field 0 Compare Enable Register

Register	Bit	RX24T(SCIg)	RX66T(SCIj,SCIi,SCIh)
CF0RR	—	—	Control Field 0 Receive Data Register
PCF1DR	—	—	Primary Control Field 1 Data Register
SCF1DR	—	—	Secondary Control Field 1 Data Register
CF1CR	—	—	Control Field 1 Compare Enable Register
CF1RR	—	—	Control Field 1 Receive Data Register
TCR	—	—	Timer Control Register
TMR	—	—	Timer Mode Register
TPRE	—	—	Timer Prescaler Register
TCNT	—	—	Timer Count Register

2.21 I²C-bus Interface

Table 2.45 lists Comparison of Specifications for I²C-bus Interface.

Table 2.45 Comparison of Specifications for I²C-bus Interface

Item	RX24T(RIICa)	RX66T(RIICa)
Number of channels	One channel	One channel
Communications format	• I²C-bus format or SMBus format • Master mode or slave mode selectable • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate	• I²C-bus format or SMBus format • Master mode or slave mode selectable • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate
Transfer rate	Fast-mode is supported (up to 400 kbps)	Fast-mode is supported (up to 400 kbps)
SCL clock	For master operation, the duty cycle of the SCL clock is selectable in the range from 4 to 96%.	For master operation, the duty cycle of the SCL clock is selectable in the range from 4 to 96%.
Issuing and detecting conditions	Start, restart, and stop conditions are automatically generated. Start conditions (including restart conditions) and stop conditions are detectable.	Start, restart, and stop conditions are automatically generated. Start conditions (including restart conditions) and stop conditions are detectable.
Slave address	• Up to three different slave addresses can be set. • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.	• Up to three different slave addresses can be set. • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.
Acknowledgment	• For transmission, the acknowledge bit is automatically loaded. - Transfer of the next data for transmission can be automatically suspended on detection of a not-acknowledge bit. • For reception, the acknowledge bit is automatically transmitted. - If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.	• For transmission, the acknowledge bit is automatically loaded. - Transfer of the next data for transmission can be automatically aborted on detection of a not-acknowledge bit. • For reception, the acknowledge bit is automatically transmitted. - If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.
Wait function	In reception, the following periods of waiting can be obtained by holding the SCL clock at the low level: • Waiting between the eighth and ninth clock cycles • Waiting between the ninth clock cycle and the first clock cycle of the next transfer	In reception, the following periods of waiting can be obtained by holding the SCL clock at the low level: • Waiting between the eighth and ninth clock cycles • Waiting between the ninth clock cycle and the first clock cycle of the next transfer
SDA output delay function	Timing of the output of transmitted data, including the acknowledge bit, can be delayed.	Timing of the output of transmitted data, including the acknowledge bit, can be delayed.

Item	RX24T(RIICa)	RX66T(RIICa)
Arbitration	• For multi-master operation - Operation to synchronize the SCL clock in cases of conflict with the SCL signal from another master is possible. - When issuing the start condition would create conflict on the bus, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. - In master operation, loss of arbitration is detected by testing for non-matching between the signal on the SDA line and the internal signal for the SDA line. • Loss of arbitration due to detection of the start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • Loss of arbitration in transfer of a not-acknowledge bit due to the internal signal for the SDA line and the level on the SDA line not matching is detectable. • Loss of arbitration due to non-matching of internal and line levels for data is detectable in slave transmission.	• For multi-master operation - Operation to synchronize the SCL clock in cases of conflict with the SCL signal from another master is possible. - When issuing the start condition would create conflict on the bus, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. - In master operation, loss of arbitration is detected by testing for non-matching between the signal on the SDA line and the internal signal for the SDA line. • Loss of arbitration due to detection of the start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • Loss of arbitration in transfer of a not-acknowledge bit due to the internal signal for the SDA line and the level on the SDA line not matching is detectable. • Loss of arbitration due to non-matching of internal and line levels for data is detectable in slave transmission.
Timeout function	The internal timeout function is capable of detecting long-interval stop of the SCL clock.	The internal timeout function is capable of detecting long-interval stop of the SCL clock.
Noise cancellation	The interface incorporates digital noise filters for both the SCL and SDA signals, and the width for noise cancellation by the filters is adjustable by software.	The interface incorporates digital noise filters for both the SCL and SDA signals, and the width for noise cancellation by the filters is adjustable by software.
Interrupt sources	Four sources: • Error in transfer or occurrence of events Detection of arbitration, NACK, timeout, a start condition including a restart condition, or a stop condition • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmit end	Four sources: • Error in transfer or occurrence of events Detection of arbitration, NACK, timeout, a start condition including a restart condition, or a stop condition • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmit end
Low power consumption function	Module stop state can be set.	Module stop state can be set.
RIIC operating modes	Four modes: • Master transmit mode • Master receive mode • Slave transmit mode • Slave receive mode	Four modes: • Master transmit mode • Master receive mode • Slave transmit mode • Slave receive mode

Item	RX24T(RIICa)	RX66T(RIICa)
Event link function (output)	—	Four sources: • Error in transfer or occurrence of events Detection of arbitration, NACK, timeout, a start condition including a restart condition, or a stop condition • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmit end

2.22 CAN Module

Table 2.46 lists Comparison of Specifications for CAN Module and Table 2.47 lists Comparison of Registers for CAN Module.

Table 2.46 Comparison of Specifications for CAN Module

Item	RX24T(RSCAN)	RX66T(CAN)
Number of channels	One channel	One channel
Protocol	ISO 11898-1 compliant	ISO 11898-1 compliant (standard and extended frames)
Bit rate	• Maximum 1 Mbps	• Programmable bit rate up to 1 Mbps (fCAN ≥ 8 MHz) • fCAN: CAN clock source
Message box	20 buffers in total • Individual buffers: 4 buffers (4 buffers for one channel) Transmit buffer: 4 buffers per a channel • Shared buffers: 16 buffers Receive buffer: 0 to 16 buffers Receive FIFO buffer: 2 FIFO buffers (up to 16 buffers allocatable to each) Transmit/receive FIFO buffer: A FIFO buffer per a channel (up to 16 buffers allocatable to each)	• 32 mailboxes: Two selectable mailbox modes • Normal mailbox mode: 32 mailboxes can be configured for either transmission or reception. • FIFO mailbox mode: 24 mailboxes can be configured for either transmission or reception. Of the other mailboxes, four FIFO stages can be configured for transmission and four FIFO stages for reception.
Reception	• Receives data frames and remote frames. • Selects ID format (standard ID, extended ID, or both IDs) to be received. • Sets interrupt enable/disable for each FIFO. • Mirror function (to receive messages transmitted from the own CAN node) • Timestamp function (to record message reception time as a 16-bit timer value)	• Data frame and remote frame can be received. • Selectable receiving ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot reception function • Selectable from overwrite mode (message overwritten) and overrun mode (message discarded) • The reception complete interrupt can be individually enabled or disabled for each mailbox.

Item	RX24T(RSCAN)	RX66T(CAN)
Acceptance filter	See description of reception filter function.	• Eight acceptance masks (one mask for every four mailboxes) • The mask can be individually enabled or disabled for each mailbox
Reception filter function	• Selects receive messages according to 16 receive rules. • Sets the number of receive rules (0 to 16) for each channel. • Acceptance filter processing: Sets ID and mask for each receive rule. • DLC filter processing: Sets DLC check value for each receive rule.	—
Receive message transfer function	• Routing function to transfer receive messages to arbitrary destinations (can be transferred to up to 2 buffers). Transfer destination: Receive buffer, receive FIFO buffer, and transmit/receive FIFO buffer • Label addition function Stores label information together when storing a message in a receive buffer and FIFO buffer.	—
Transmission	• Transmits data frames and remote frames. • Selects ID format (standard ID, extended ID, or both IDs) to be transmitted. • Sets interrupt enable/disable for each transmit buffer and transmit/receive FIFO buffer. • One-shot transmission function • Selects ID priority transmission or transmit buffer number priority transmission. • Transmit abort function (completion of the abort can be confirmed with the flag)	• Data frame and remote frame can be transmitted. • Selectable transmitting ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot transmission function • Selectable from ID priority mode and mailbox number priority mode • Transmission request can be aborted (the completion of abort can be confirmed with a flag) • The transmission complete interrupt can be individually enabled or disabled for each mailbox.
Interval transmission function	Sets message transmission interval time (transmit mode of transmit/receive FIFO buffers)	—
Transmit history function	Stores the history information of transmitted messages.	—

Item	RX24T(RSCAN)	RX66T(CAN)
Mode transition for bus-off recovery	Selects a method of returning from bus off state. • ISO 11898-1 compliant • Automatic transition to channel halt mode at bus-off entry • Automatic transition to channel halt mode at bus-off end • Transition to channel halt mode by a program • Transition to the error-active state by a program (forcible return from the bus off state)	Mode transition for the recovery from the bus-off state can be selected: • ISO 11898-1 Standards compliant • Automatic entry to CAN halt mode at bus-off entry • Automatic entry to CAN halt mode at bus-off end • Entry to CAN halt mode by a program • Transition into error-active state by a program
Error status monitoring	• Monitors CAN protocol errors (stuff error, form error, ACK error, CRC error, bit error, ACK delimiter error, and bus dominant lock). • Detects error status transitions (error warning, error passive, bus off entry, and bus off recovery) • Reads the error counter. • Monitors DLC errors.	• CAN bus errors (stuff error, form error, ACK error, CRC error, bit error, and ACK delimiter error) can be monitored. • Transition to error states can be detected (error-warning, error-passive, bus-off entry, and bus-off recovery). • The error counters can be read.
Time stamp function	See description of reception.	• Time stamp function using a 16-bit counter • The reference clock can be selected from 1-, 2-, 4- and 8-bit time periods.
Interrupt function	5 sources • Global (2 sources) Global receive FIFO interrupt Global error interrupt • Channel (3 sources/channel) Channel transmit interrupt - Transmit complete interrupt - Transmit abort interrupt - Transmit/receive FIFO transmit complete interrupt - Transmit history interrupt Transmit/receive FIFO receive interrupt Channel error interrupt	Five types of interrupt sources (reception complete, transmission complete, receive FIFO, transmit FIFO, and error interrupts)
CAN sleep mode	—	Current consumption can be reduced by stopping the CAN clock.
Software support unit	—	Three software support units: • Acceptance filter support • Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search) • Channel search support
CAN clock source	Peripheral module clock (PCLK), CANMCLK	Peripheral module clock (PCLKB) or CANMCLK

Item	RX24T(RSCAN)	RX66T(CAN)
Test mode	Test function for user evaluation • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback) • RAM test (read/write test)	Three test modes available for user evaluation • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback)
Power consumption reducing function	Module stop state can be set.	Module-stop state can be set.

Table 2.47 Comparison of Registers for CAN Module

Register	Bit	RX24T(RSCAN)	RX66T(CAN)
CFGL	—	Bit Configuration Register L	—
CFGH	—	Bit Configuration Register H	—
CTRL	—	Control Register L	—
CTRH	—	Control Register H	—
STSL	—	Status Register L	—
STSH	—	Status Register H	—
ERFLL	—	Error Flag Register L	—
ERFLH	—	Error Flag Register H	—
GCFGL	—	Global Configuration Register L	—
GCFGH	—	Global Configuration Register H	—
GCTRL	—	Global Control Register L	—
GCTRH	—	Global Control Register H	—
GSTS	—	Global Status Register	—
GERFLL	—	Global Error Flag Register	—
GTINTSTS	—	Global Transmit Interrupt Status Register	—
GTSC	—	Timestamp Register	—
GAFLCFG	—	Receive Rule Number Configuration Register	—
GAFLIDLj	—	Receive Rule Entry Register jAL (j = 0 to 15)	—
GAFLIDHj	—	Receive Rule Entry Register jAH (j = 0 to 15)	—
GAFLMLj	—	Receive Rule Entry Register jBL (j = 0 to 15)	—
GAFLMHj	—	Receive Rule Entry Register jBH (j = 0 to 15)	—
GAFLPLj	—	Receive Rule Entry Register jCL (j = 0 to 15)	—
GAFLPHj	—	Receive Rule Entry Register jCH (j = 0 to 15)	—
RMNB	—	Receive Buffer Number Configuration Register	—
RMND0	—	Receive Buffer Receive Complete Flag Register	—
RMIDLn	—	Receive Buffer Register nAL (n = 0 to 15)	—
RMIDHn	—	Receive Buffer Register nAH (n = 0 to 15)	—
RMTSn	—	Receive Buffer Register nBL (n = 0 to 15)	—
RMPTRn	—	Receive Buffer Register nBH (n = 0 to 15)	—
RMDF0n	—	Receive Buffer Register nCL (n = 0 to 15)	—
RMDF1n	—	Receive Buffer Register nCH (n = 0 to 15)	—
RMDF2n	—	Receive Buffer Register nDL (n = 0 to 15)	—

Register	Bit	RX24T(RSCAN)	RX66T(CAN)
RMDF3n	—	Receive Buffer Register nDH (n = 0 to 15)	—
RFCCm	—	Receive FIFO Control Register m (m = 0, 1)	—
RFSTSm	—	Receive FIFO Status Register m (m = 0, 1)	—
RFPCTRm	—	Receive FIFO Pointer Control Register m (m = 0, 1)	—
RFIDLm	—	Receive FIFO Access Register mAL (m = 0, 1)	—
RFIDHm	—	Receive FIFO Access Register mAH (m = 0, 1)	—
RFTSm	—	Receive FIFO Access Register mBL (m = 0, 1)	—
RFPTRm	—	Receive FIFO Access Register mBH (m = 0, 1)	—
RFDF0m	—	Receive FIFO Access Register mCL (m = 0, 1)	—
RFDF1m	—	Receive FIFO Access Register mCH (m = 0, 1)	—
RFDF2m	—	Receive FIFO Access Register mDL (m = 0, 1)	—
RFDF3m	—	Receive FIFO Access Register mDH (m = 0, 1)	—
CFCCL0	—	Transmit/Receive FIFO Control Register 0L	—
CFCCH0	—	Transmit/Receive FIFO Control Register 0H	—
CFSTS0	—	Transmit/Receive FIFO Status Register 0	—
CFPCTR0	—	Transmit/Receive FIFO Pointer Control Register 0	—
CFIDL0	—	Transmit/Receive FIFO Access Register 0AL	—
CFIDH0	—	Transmit/Receive FIFO Access Register 0AH	—
CFTS0	—	Transmit/Receive FIFO Access Register 0BL	—
CFPTR0	—	Transmit/Receive FIFO Access Register 0BH	—
CFDF00	—	Transmit/Receive FIFO Access Register 0CL	—
CFDF10	—	Transmit/Receive FIFO Access Register 0CH	—

Register	Bit	RX24T(RSCAN)	RX66T(CAN)
CFDF20	—	Transmit/Receive FIFO Access Register 0DL	—
CFDF30	—	Transmit/Receive FIFO Access Register 0DH	—
RFMSTS	—	Receive FIFO Message Lost Status Register	—
CFMSTS	—	Transmit/Receive FIFO Message Lost Status Register	—
RFISTS	—	Receive FIFO Interrupt Status Register	—
CFISTS	—	Transmit/Receive FIFO Receive Interrupt Status Register	—
TMCp	—	Transmit Buffer Control Register p (p = 0 to 3)	—
TMSTSp	—	Transmit Buffer Status Register p (p = 0 to 3)	—
TMTRSTS	—	Transmit Buffer Transmit Request Status Register	—
TMTCSTS	—	Transmit Buffer Transmit Complete Status Register	—
TMTASTS	—	Transmit Buffer Transmit Abort Status Register	—
TMIEC	—	Transmit Buffer Interrupt Enable Register	—
TMIDLp	—	Transmit Buffer Register pAL (p = 0 to 3)	—
TMIDHp	—	Transmit Buffer Register pAH (p = 0 to 3)	—
TMPTRp	—	Transmit Buffer Register pBH (p = 0 to 3)	—
TMDF0p	—	Transmit Buffer Register pCL (p = 0 to 3)	—
TMDF1p	—	Transmit Buffer Register pCH (p = 0 to 3)	—
TMDF2p	—	Transmit Buffer Register pDL (p = 0 to 3)	—
TMDF3p	—	Transmit Buffer Register pDH (p = 0 to 3)	—
THLCC0	—	Transmit History Buffer Control Register	—
THLSTS0	—	Transmit History Buffer Status Register	—
THLACC0	—	Transmit History Buffer Access Register	—
THLPCTR0	—	Transmit History Buffer Pointer Control Register	—
GRWCR	—	Global RAM Window Control Register	—
GTSTCFG	—	Global Test Configuration Register	—
GTSTCTRL	—	Global Test Control Register	—
GLOCKK	—	Global Test Protection Unlock Register	—

Register	Bit	RX24T(RSCAN)	RX66T(CAN)
RPGACCr	—	RAM Test Register r (r = 0 to 127)	—
CTLR	—	—	Control Register
BCR	—	—	Bit Configuration Register
MKRk	—	—	Mask Register k (k = 0 to 7)
FIDCR0	—	—	FIFO Received ID Compare Registers 0
FIDCR1	—	—	FIFO Received ID Compare Registers 1
MKIVLR	—	—	Mask Invalid Register
MBj	—	—	Mailbox Register j (j = 0 to 31)
MIER	—	—	Mailbox Interrupt Enable Register
MCTLj	—	—	Message Control Register j (j = 0 to 31)
RFCR	—	—	Receive FIFO Control Register
RFPCR	—	—	Receive FIFO Pointer Control Register
TFCR	—	—	Transmit FIFO Control Register
TFPCR	—	—	Transmit FIFO Pointer Control Register
STR	—	—	Status Register
MSMR	—	—	Mailbox Search Mode Register
MSSR	—	—	Mailbox Search Status Register
CSSR	—	—	Channel Search Support Register
AFSR	—	—	Acceptance Filter Support Register
EIER	—	—	Error Interrupt Enable Register
EIFR	—	—	Error Interrupt Factor Judge Register
RECR	—	—	Receive Error Count Register
TECR	—	—	Transmit Error Count Register
ECSR	—	—	Error Code Store Register
TSR	—	—	Time Stamp Register
TCR	—	—	Test Control Register

2.23 Serial Peripheral Interface

Table 2.48 lists Comparison of Specifications for Serial Peripheral Interface and Table 2.49 lists Comparison of Registers for Serial Peripheral Interface.

Table 2.48 Comparison of Specifications for Serial Peripheral Interface

Item	RX24T(RSPIb)	RX66T(RSPIc)
Number of channels	One channel	One channel
RSPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Capable of serial communications in master/slave mode • Communication mode: Full-duplex or transmit-only can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Capable of serial communications in master/slave mode • Communication mode: Full-duplex or transmit-only can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK
Data format	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits).	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits). • Byte swapping of transmit and receive data is selectable
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from divided by 2 to divided by 4096). • In slave mode, the minimum PCLK clock divided by 6 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 6). Width at high level: 3 cycles of PCLK; width at low level: 3 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from divided by 2 to divided by 4096). • In slave mode, the minimum PCLK clock divided by 4 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 4). Width at high level: 2 cycles of PCLK; width at low level: 2 cycles of PCLK
Buffer configuration	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection
Interrupt sources	Interrupt sources • Receive buffer full interrupt • Transmit buffer empty interrupt • RSPI error interrupt (mode fault, overrun, underrun, or parity error) • RSPI idle interrupt (RSPI idle)	Interrupt sources • Receive buffer full interrupt • Transmit buffer empty interrupt • RSPI error interrupt (mode fault, overrun, underrun, or parity error) • RSPI idle interrupt (RSPI idle)

Item	RX24T(RSPIb)	RX66T(RSPIc)
SSL control function	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for either output or unused. • In slave mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) - Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) - Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) - Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for either output or unused. • In slave mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) - Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) - Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) - Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity
Control in master transfer	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function
Event link function (output)	—	The following events can be output to the event link controller. (RSPI0) • Receive buffer full signal • Transmit buffer empty signal • Mode fault, overrun, underrun, or parity error signal • RSPI idle signal • Transmission-completed signal
Others	• Function for switching between CMOS output and open-drain output (switched by ODRn.Bi bit) • Function for initializing the RSPI • Loopback mode	• Function for switching between CMOS output and open-drain output (switched by ODRn.Bi bit) • Function for initializing the RSPI • Loopback mode
Low power consumption function	Module stop state can be set.	Module stop state can be set.

Table 2.49 Comparison of Registers for Serial Peripheral Interface

Register	Bit	RX24T(RSPIb)	RX66T(RSPIc)
SPDR	—	RSPI Data Register Available access size: • Longwords (SPDCR.SPLW=1) • Words (SPDCR.SPLW=0)	RSPI Data Register Available access size: • Longwords (SPDCR.SPLW=1, SPDCR.SPBYT=0) • Words (SPDCR.SPLW=0, SPDCR.SPBYT=0) • Bytes (SPDCR.SPBYT=1)
SPDCR	SPBYT	—	RSPI Byte Access Specification
SPDCR2	—	—	RSPI Data Control Register 2

2.24 CRC Calculator

Table 2.50 lists Comparison of Specifications for CRC Calculator and Table 2.51 lists Comparison of Registers for CRC Calculator.

Table 2.50 Comparison of Specifications for CRC Calculator

Item	RX24T(CRC)	RX66T(CRCA)	
Data size	8 bits	8 bits	32 bits
Data for CRC calculation	CRC codes are generated for any desired data in 8n-bit units (where n is a whole number)	CRC codes are generated for any desired data in 8n-bit units (where n is a whole number)	CRC codes are generated for any desired data in 32n-bit units (where n is a whole number)
CRC processor unit	8-bit parallel processing	8-bit parallel processing	32-bit parallel processing
CRC generating polynomial	One of three generating polynomials is selectable 8-bit CRC: • $X^8 + X^2 + X + 1$ 16-bit CRC: • $X^{16} + X^{15} + X^2 + 1$ • $X^{16} + X^{12} + X^5 + 1$	One of three generating polynomials is selectable 8-bit CRC: • $X^8 + X^2 + X + 1$ 16-bit CRC: • $X^{16} + X^{15} + X^2 + 1$ • $X^{16} + X^{12} + X^5 + 1$	One of two generating polynomials is selectable 32-bit CRC: • $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ • $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$
CRC calculation switching	The bit order of CRC calculation results can be switched for LSB first or MSB first communication	The order of the bits produced by CRC calculation can be switched for LSB first or MSB first communication	
Low power consumption	Module stop state can be set.	Module stop state can be set.	

Table 2.51 Comparison of Registers for CRC Calculator

Register	Bit	RX24T(CRC)	RX66T(CRCA)
CRCCR	GPS[1:0]:RX24T GPS[2:0]:RX66T	CRC Generating Polynomial Switching b1 b0 0 0: No calculation is executed. 0 1: 8-bit CRC ($X^8 + X^2 + X + 1$) 1 0: 16-bit CRC ($X^{16} + X^{15} + X^2 + 1$) 1 1: 16-bit CRC ($X^{16} + X^{12} + X^5 + 1$)	CRC Generating Polynomial Switching b2 b0 0 0 0: No calculation is executed. 0 0 1: 8-bit CRC ($X^8 + X^2 + X + 1$) 0 1 0: 16-bit CRC ($X^{16} + X^{15} + X^2 + 1$) 0 1 1: 16-bit CRC ($X^{16} + X^{12} + X^5 + 1$) 1 0 0: 32-bit CRC ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$) 1 0 1 : 32-bit CRC ($X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$) 1 1 0: No calculation is executed. 1 1 1: No calculation is executed.
	LMS	CRC Calculation Switching (b2)	CRC Calculation Switching (b6)
CRCDIR	—	CRC Data Input Register Available access size: • Bytes	CRC Data Input Register Available access size: • Longwords (When generating a 32-bit CRC) • Bytes (When generating a 16-bit/8-bit CRC)
CRCDOR	—	CRC Data Output Register Available access size: • Words When generating 8-bit CRC, the valid CRC code is obtained from the lower-order byte (b7 to b0).	CRC Data Output Register Available access size: • Longwords (When generating a 32-bit CRC) • Words (When generating a 16-bit CRC) • Bytes (When generating a 8-bit CRC)

2.25 12-Bit A/D Converter

Table 2.52 lists Comparison of Specifications for 12-Bit A/D Converter and Table 2.53 lists Comparison of Registers for 12-Bit A/D Converter.

Table 2.52 Comparison of Specifications for 12-Bit A/D Converter

Item	RX24T(S12ADF)	RX66T(S12ADH)
Number of units	Three units (S12AD, S12AD1, and S12AD2)	Three units (S12AD, S12AD1, and S12AD2)
Input channels	Five channels for S12AD, five channels for S12AD1, and 12 channels for S12AD2	Eight channels for S12AD, eight channels for S12AD1, and 14 channels for S12AD2
Extended analog function	Internal reference voltage (S12AD2 only)	Temperature sensor output, internal reference voltage (S12AD2 only)
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	• 1 µs per channel (when A/D conversion clock ADCLK = 40 MHz)	• 0.9 µs per channel (when A/D conversion clock ADCLK = 60 MHz)
A/D conversion clock	• Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the frequency ratio should be one of the following. PCLK to ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1, 8:1 • ADCLK is set using the clock generation circuit.	• Peripheral module clock PCLK and A/D conversion clock ADCLK can be set with one of the following frequency ratio: PCLK to ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1 • ADCLK is set using the clock generation circuit. • A/D conversion clock (ADCLK) can operate between 8 MHz at a minimum and 60 MHz at a maximum.
Data registers	• 22 registers for analog input (five for S12AD, five for S12AD1, and 12 for S12AD2), 1 for A/D-converted data duplication in double trigger mode, and 2 for A/D-converted data duplication during extended operation in double trigger mode unit. • One register for internal reference (S12AD2) • One register for self-diagnosis per unit • The results of A/D conversion are stored in 12-bit A/D data registers. • 12-bit accuracy output for the results of A/D conversion • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers): A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.	• 30 registers for analog input (eight for S12AD, eight for S12AD1, and 14 for S12AD2), 1 for A/D-converted data duplication in double trigger mode per unit, and 2 for A/D-converted data duplication during extended operation in double trigger mode per unit. • One register for temperature sensor (S12AD2) • One register for internal reference (S12AD2) • One register for self-diagnosis per unit • The results of A/D conversion are stored in 12-bit A/D data registers. • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers): A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.

Item	RX24T(S12ADF)	RX66T(S12ADH)
Operating modes	Operating modes can be set independently for three units. • Single scan mode: - A/D conversion is performed only once on the analog inputs arbitrarily selected. - A/D conversion is performed only once on the internal reference voltage (S12AD2). • Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs arbitrarily selected. • Group scan mode: - Two (groups A and B) or three (groups A, B, and C) can be selected as the number of the groups to be used. Only the combination of groups A and B can be selected when the number of the groups is two. - Analog inputs arbitrarily selected are divided into two groups (group A and B) or three groups (group A, B, and C), and A/D conversion of the analog input selected on a group basis is performed only once. - The conditions for scanning start of groups A, B, and C (synchronous trigger) can be independently selected, thus allowing A/D conversion of each group to be started independently. • Group scan mode (when group priority control selected) : - If a priority-group trigger is input during scanning of the low-priority group, scan of the low-priority group is stopped and scan of the priority group is started. The priority order is group A (highest) > group B > group C (lowest). Whether or not to restart scanning of the low-priority group after processing for the high-priority group completes, is selectable. Rescan can also be set to start either from the beginning of the selected channel or the channel on which A/D conversion is not completed.	Operating modes can be set independently for three units. • Single scan mode: - A/D conversion is performed only once on the analog inputs arbitrarily selected. - A/D conversion is performed only once on the temperature sensor output (S12AD2). - A/D conversion is performed only once on the internal reference voltage (S12AD2). • Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs arbitrarily selected. • Group scan mode: - Two (groups A and B) or three (groups A, B, and C) can be selected as the number of the groups to be used. (Only the combination of groups A and B can be selected when the number of the groups is two.) - Analog inputs, temperature sensor output (S12AD2), and internal reference voltage (S12AD2) that are arbitrarily selected are divided into two groups (group A and B) or three groups (group A, B, and C), and A/D conversion of the analog input selected on a group basis is performed only once. - The conditions for scanning start of groups A, B, and C (synchronous trigger) can be independently selected, thus allowing A/D conversion of each group to be started independently. • Group scan mode (when group priority control selected) : - If a priority-group trigger is input during scanning of the low-priority group, scan of the low-priority group is stopped and scan of the priority group is started. The priority order is group A (highest) > group B > group C (lowest). Whether or not to restart scanning of the low-priority group after processing for the high-priority group completes, is selectable. Rescan can also be set to start either from the beginning of the selected channel or the channel on which A/D conversion is not completed.
Conditions for A/D conversion start	• Software trigger • Synchronous trigger - Trigger by the multi-function timer pulse unit (MTU), general PWM timer (GPT), or 8-bit timer (TMR). • Asynchronous trigger - A/D conversion can be triggered by the external trigger ADTRG0# (S12AD), ADTRG1# (S12AD1), or ADTRG2# (S12AD2) pin (independently for three units).	• Software trigger • Synchronous trigger - Trigger by the multi-function timer pulse unit (MTU), 8-bit timer (TMR), or event link controller (ELC). • Asynchronous trigger - A/D conversion can be triggered by the external trigger ADTRG0# (S12AD), ADTRG1# (S12AD1), or ADTRG2# (S12AD2) pin (independently for three units).

Item	RX24T(S12ADF)	RX66T(S12ADH)
Function	• Channel-dedicated sample-and-hold function (three channels for S12AD1 only)	• Channel-dedicated sample-and-hold function (three channels for S12AD and three channels for S12AD1) (Constant sampling can be set)
	• Variable sampling state count (settable for each channel)	• Variable sampling time (can be set per channel)
	• Self-diagnosis of 12-bit A/D converter	• Self-diagnosis of 12-bit A/D converter
	• Selectable A/D-converted value addition mode or average mode	• Selectable A/D-converted value addition mode or average mode
	• Analog input disconnection detection assist function (discharge function/precharge function)	• Analog input disconnection detection assist function (discharge function/precharge function)
	• Double trigger mode (duplication of A/D conversion data)	• Double trigger mode (duplication of A/D conversion data)
	• Automatic clear function of A/D data registers	• Automatic clear function of A/D data registers
		• Comparison function (windows A and B)
		• Order of channel conversion in each unit can be set.
	• Input signal amplification function of the programmable gain amplifier (1 channel for S12AD and 3 channels for S12AD1)	• Input signal amplification function of the programmable gain amplifier (each unit has 3 channels; either single-ended input or pseudo-differential input can be selected)
Interrupt sources	• In the modes except double trigger mode and group scan mode, a scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of single scan. (Independently for three units).	• In the modes except double trigger mode and group scan mode, a scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of single scan. (Independently for three units).
	• In double trigger mode, a scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of double scan. (Independently for three units).	• In double trigger mode, a scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of double scan. (Independently for three units).
	• In group scan mode, a scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of group A scan, whereas a scan end interrupt request (GBADI, GBADI1, or GBADI2) for group B can be generated on completion of group B scan, and a group C scan end interrupt request (GCADI, GCADI1, or GCADI2) can be generated on completion of group C scan.	• In group scan mode, a scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of group A scan, whereas a group B scan end interrupt request (S12GBADI, S12GBADI1, or S12GBADI2) can be generated on completion of group B scan, and a group C scan end interrupt request (S12GCADI, S12GCADI1, or S12GCADI2) can be generated on completion of group C scan.
	• When double trigger mode is selected in group scan mode, an A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of double scan of group A, and the corresponding scan end interrupt request (GBADI/GCADI, GBADI1/GCADI1, or GBADI2/GCADI2) can be generated on completion of group B and group C scan.	• When double trigger mode is selected in group scan mode, an A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of double scan of group A, and the corresponding scan end interrupt request (S12GBADI/S12GCADI, S12GBADI1/S12GCADI1, or S12GBADI2/S12GCADI2) can be generated on completion of group B and group C scan.
		• A compare interrupt request (S12CMPAI, S12CMPAI1, S12CMPAI2, S12CMPBI, S12CMPBI1, or S12CMPBI2) can be generated upon a match with the comparison condition for the digital compare function.
	• The S12ADI/S12ADI1/S12ADI2, GBADI/GBADI1/GBADI2, and GCADI/GCADI1/GCADI2 interrupts can activate the data transfer controller (DTC).	• The S12ADI/S12ADI1/S12ADI2, S12GBADI/S12GBADI1/S12GBADI2, and S12GCADI/S12GCADI1/S12GCADI2 interrupts can trigger the DMA controller (DMAC) and data transfer controller (DTC).

Item	RX24T(S12ADF)	RX66T(S12ADH)
Event link	—	• The event signal is generated when all scans are finished. • The event signal is generated depending on conditions for comparison function window in single scan mode. • Able to start scanning by a trigger from the ELC.
Low power consumption function	Module stop state can be set.	Module stop state can be set.

Table 2.53 Comparison of Registers for 12-Bit A/D Converter

Register	Bit	RX24T(S12ADF)	RX66T(S12ADH)
ADDRy	—	A/D Data Registers y (S12AD: y = 0 to 3, 16, S12AD1: y = 0 to 3, 16, S12AD2: y = 0 to 11)	A/D Data Registers y (S12AD: y = 0 to 7, S12AD1: y = 0 to 7, S12AD2: y = 0 to 11, 16, 17)
ADTSDR	—	—	A/D Temperature Sensor Data Register
ADANSA0	[S12AD.ADANSA0] ANSA000 to 003 (RX24T) ANSA000 to 007 (RX66T) [S12AD1.ADANSA0] ANSA000 to 003 (RX24T) ANSA000 to 007 (RX66T)	A/D Conversion Channel Select	A/D Conversion Channel Select
ADANSA1	[S12AD.ADANSA1] ANSA100 (RX24T) — (RX66T) [S12AD1.ADANSA1] ANSA100 (RX24T) — (RX66T) [S12AD2.ADANSA1] — (RX24T) ANSA100, 101 (RX66T)	A/D Conversion Channel Select	A/D Conversion Channel Select
ADANSB0	[S12AD.ADANSB0] ANSB000 to 003 (RX24T) ANSB000 to 007 (RX66T) [S12AD1.ADANSB0] ANSB000 to 003 (RX24T) ANSB000 to 007 (RX66T)	A/D Conversion Channel Select	A/D Conversion Channel Select
ADANSB1	[S12AD.ADANSB1] ANSB100 (RX24T) — (RX66T) [S12AD1.ADANSB1] ANSB100 (RX24T) — (RX66T) [S12AD2.ADANSB1] — (RX24T) ANSB100, 101 (RX66T)	A/D Conversion Channel Select	A/D Conversion Channel Select

Register	Bit	RX24T(S12ADF)	RX66T(S12ADH)
ADANSC0	[S12AD.ADANSC0] ANSC000 to 003 (RX24T) ANSC000 to 007 (RX66T) [S12AD1.ADANSC0] ANSC000 to 003 (RX24T) ANSC000 to 007 (RX66T)	A/D Conversion Channel Select	A/D Conversion Channel Select
ADANSC1	[S12AD.ADANSC1] ANSC100 (RX24T) — (RX66T) [S12AD1.ADANSC1] ANSC100 (RX24T) — (RX66T) [S12AD2.ADANSC1] — (RX24T) ANSC100, 101 (RX66T)	A/D Conversion Channel Select	A/D Conversion Channel Select
ADSCSn	—	—	A/D Channel Conversion Order Setting Register n (n = 0 to 13)
ADADS0	[S12AD.ADADS0] ADS000 to 003 (RX24T) ADS000 to 007 (RX66T) [S12AD1.ADADS0] ADS000 to 003 (RX24T) ADS000 to 007 (RX66T)	A/D-Converted Value Addition/Average Channel Select	A/D-Converted Value Addition/Average Channel Select
ADADS1	[S12AD.ADADS1] ADS100 (RX24T) — (RX66T) [S12AD1.ADADS1] ADS100 (RX24T) — (RX66T) [S12AD2.ADADS1] — (RX24T) ADS100, 101 (RX66T)	A/D-Converted Value Addition/Average Channel Select	A/D-Converted Value Addition/Average Channel Select
ADSTRGR	TRSA[5:0]	A/D Conversion Start Trigger Select When scanning is executed in group scan mode or double trigger mode, set the ADCSR.TRGE bit to 1.	A/D Conversion Start Trigger Select When performing scanning in group scan mode or double trigger mode, set the ADCSR.TRGE bit to 1 and set the ADCSR.EXTRG bit to 0.
ADEXICR	TSSAD	—	Temperature Sensor Output A/D-Converted Value Addition/Average Mode Select

Register	Bit	RX24T(S12ADF)	RX66T(S12ADH)
ADEXICR	TSSA	—	Temperature Sensor Output A/D Conversion Select
	TSSB	—	Group B Temperature Sensor Output A/D Conversion Select
	OCSB	—	Group B Internal Reference Voltage A/D Conversion Select
ADGCEXCR	—	—	A/D Group C Extended Input Control Register
ADSSTRn	—	A/D Sampling State Register n (n = 0 to 11, L, O)	A/D Sampling State Register n (n = 0 to 11, L, T, O)
		Set a value that is 5 states or more when PCLK to ADCLK frequency ratio = 1:1, 2:1, 4:1, or 8:1. Set a value that is 6 states or more when PCLK to ADCLK frequency ratio = 1:2.	Specify the value for the register as a multiples of 3 in the range from 12 to 252 (clock cycles).
		Initial values after a reset are different.	
ADSHCR	SSTSH[7:0]	Set the sampling time (4 to 255 states).	Set a sampling time between 12 and 252 clock cycles.
		Initial values after a reset are different.	
ADSHMSR	—	—	A/D Sample-and-Hold Operating Mode Select Register
ADDISCR	ADNDIS[4:0]	A/D Disconnection Detection Assist Setting ADNDIS[3:0]: Discharge/precharge period The setting value is a value other than 0000b or 0001b.	A/D Disconnection Detection Assist Setting ADNDIS[3:0]: Specify the period for discharging or precharging as a number of ADCLK cycles. The setting value is one of the following: b3 b0 0 0 0 0: No charging (disconnection detection assist function is disabled.) 0 0 1 1: Charging period of 3 clock cycles 0 1 1 0: Charging period of 6 clock cycles 1 0 0 1: Charging period of 9 clock cycles 1 1 0 0: Charging period of 12 clock cycles 1 1 1 1: Charging period of 15 clock cycles
ADELCCR	—	—	A/D Event Link Control Register

Register	Bit	RX24T(S12ADF)	RX66T(S12ADH)
ADPGACR [S12AD. ADPGACR]	b0	The write value should be 1.	(P000CR[3:0]) P000 Amplifier Control
	b1	(P000SEL1) PGA P000 Amplifier Pass-Through Enable	
	b2	(P000ENAMP) PGA P000 Amplifier Enable	
	b3	The write value should be 1.	
	b4		(P001CR[3:0]) P001 Amplifier Control
	b5	The write value should be 0.	
	b6		
	b7	The write value should be 1.	
	b8		(P002CR[3:0]) P002 Amplifier Control
	b9	The write value should be 0.	
	b10		
	b11	The write value should be 1.	
	b12		The write value should be 0.
	b13	The write value should be 0.	
	b14		
	b15	The write value should be 1.	
ADPGACR [S12AD1. ADPGACR]	b0	The write value should be 1.	(P100CR[3:0]) P100 Amplifier Control
	b1	(P100SEL1) PGA P100 Amplifier Pass-Through Enable	
	b2	(P100ENAMP) PGA P100 Amplifier Enable	
	b3	The write value should be 1.	
	b4		(P101CR[3:0]) P101 Amplifier Control
	b5	(P101SEL1) PGA P101 Amplifier Pass-Through Enable	
	b6	(P101ENAMP) PGA P101 Amplifier Enable	
	b7	The write value should be 1.	
	b8		(P102CR[3:0]) P102 Amplifier Control
	b9	(P102SEL1) PGA P102 Amplifier Pass-Through Enable	
	b10	(P102ENAMP) PGA P102 Amplifier Enable	
	b11	The write value should be 1.	
	b12		The write value should be 0.
	b13	The write value should be 0.	
	b14		
	b15	The write value should be 1.	

Register	Bit	RX24T(S12ADF)	RX66T(S12ADH)
ADPGAGS0 [S12AD. ADPGAGS0]	P000GAIN[3:0]	PGA P000 Gain Setting b3 b0 0 0 0 0: × 2.000 0 0 0 1: × 2.500 0 1 0 0: × 3.077 0 1 1 0: × 3.636 0 1 1 1: × 4.000 1 0 0 0: × 4.444 Settings other than above are prohibited.	P000 Amplifier Gain Setting When pseudo-differential input is disabled (ADPGADCR0.PxDEN bit = 0) b3 b0 0 0 0 0: × 2.000 0 0 0 1: × 2.500 0 0 1 1: × 3.077 0 1 0 1: × 3.636 0 1 1 0: × 4.000 0 1 1 1: × 4.444 1 0 0 0: × 5.000 1 0 1 0: × 6.667 1 0 1 1: × 8.000 1 1 0 0: × 10.000 1 1 0 1: × 13.333 1 1 1 0: × 20.000 Settings other than above are prohibited. When pseudo-differential input is enabled (ADPGADCR0.PxDEN bit = 1 and ADPGACR.PxCR[2] bit = 1) b3 b0 0 0 0 1: × 1.500 1 0 0 0: × 4.000 1 0 1 1: × 7.000 1 1 0 1: × 12.333 Settings other than above are prohibited.
	P001GAIN[3:0]	—	P001 Amplifier Gain Setting
	P002GAIN[3:0]	—	P002 Amplifier Gain Setting

Register	Bit	RX24T(S12ADF)	RX66T(S12ADH)
ADPGAGS0 [S12AD1. ADPGAGS0]	P100GAIN[3:0]	PGA P100 Gain Setting b3 b0 0 0 0 0: × 2.000 0 0 0 1: × 2.500 0 1 0 0: × 3.077 0 1 1 0: × 3.636 0 1 1 1: × 4.000 1 0 0 0: × 4.444 Settings other than above are prohibited.	P100 Amplifier Gain Setting When pseudo-differential input is disabled (ADPGADCR0.PxDEN bit = 0) b3 b0 0 0 0 0: × 2.000 0 0 0 1: × 2.500 0 0 1 1: × 3.077 0 1 0 1: × 3.636 0 1 1 0: × 4.000 0 1 1 1: × 4.444 1 0 0 0: × 5.000 1 0 1 0: × 6.667 1 0 1 1: × 8.000 1 1 0 0: × 10.000 1 1 0 1: × 13.333 1 1 1 0: × 20.000 Settings other than above are prohibited. When pseudo-differential input is enabled (ADPGADCR0.PxDEN bit = 1 and ADPGACR.PxCR[2] bit = 1) b3 b0 0 0 0 1: × 1.500 1 0 0 0: × 4.000 1 0 1 1: × 7.000 1 1 0 1: × 12.333 Settings other than above are prohibited.

Register	Bit	RX24T(S12ADF)	RX66T(S12ADH)
ADPGAGS0 [S12AD1. ADPGAGS0]	P101GAIN[3:0]	PGA P101 Gain Setting b3 b0 0 0 0 0: × 2.000 0 0 0 1: × 2.500 0 1 0 0: × 3.077 0 1 1 0: × 3.636 0 1 1 1: × 4.000 1 0 0 0: × 4.444 Settings other than above are prohibited.	P101 Amplifier Gain Setting When pseudo-differential input is disabled (ADPGADCR0.PxDEN bit = 0) b3 b0 0 0 0 0: × 2.000 0 0 0 1: × 2.500 0 0 1 1: × 3.077 0 1 0 1: × 3.636 0 1 1 0: × 4.000 0 1 1 1: × 4.444 1 0 0 0: × 5.000 1 0 1 0: × 6.667 1 0 1 1: × 8.000 1 1 0 0: × 10.000 1 1 0 1: × 13.333 1 1 1 0: × 20.000 Settings other than above are prohibited. When pseudo-differential input is enabled (ADPGADCR0.PxDEN bit = 1 and ADPGACR.PxCR[2] bit = 1) b3 b0 0 0 0 1: × 1.500 1 0 0 0: × 4.000 1 0 1 1: × 7.000 1 1 0 1: × 12.333 Settings other than above are prohibited.

Register	Bit	RX24T(S12ADF)	RX66T(S12ADH)
ADPGAGS0 [S12AD1. ADPGAGS0]	P102GAIN[3:0]	PGA P102 Gain Setting b3 b0 0 0 0 0: × 2.000 0 0 0 1: × 2.500 0 1 0 0: × 3.077 0 1 1 0: × 3.636 0 1 1 1: × 4.000 1 0 0 0: × 4.444 Settings other than above are prohibited.	P102 Amplifier Gain Setting When pseudo-differential input is disabled (ADPGADCR0.PxDEN bit = 0) b3 b0 0 0 0 0: × 2.000 0 0 0 1: × 2.500 0 0 1 1: × 3.077 0 1 0 1: × 3.636 0 1 1 0: × 4.000 0 1 1 1: × 4.444 1 0 0 0: × 5.000 1 0 1 0: × 6.667 1 0 1 1: × 8.000 1 1 0 0: × 10.000 1 1 0 1: × 13.333 1 1 1 0: × 20.000 Settings other than above are prohibited. When pseudo-differential input is enabled (ADPGADCR0.PxDEN bit = 1 and ADPGACR.PxCR[2] bit = 1) b3 b0 0 0 0 1: × 1.500 1 0 0 0: × 4.000 1 0 1 1: × 7.000 1 1 0 1: × 12.333 Settings other than above are prohibited.
ADCMPCR	—	—	A/D Comparison Function Control Register
ADCMPANSR0	—	—	A/D Comparison Function Window A Channel Select Register 0
ADCMPANSR1	—	—	A/D Comparison Function Window A Channel Select Register 1
ADCMPANSER	—	—	A/D Comparison Function Window A Extended Input Select Register
ADCMPLR0	—	—	A/D Comparison Function Window A Comparison Condition Setting Register 0
ADCMPLR1	—	—	A/D Comparison Function Window A Comparison Condition Setting Register 1

Register	Bit	RX24T(S12ADF)	RX66T(S12ADH)
ADCMPLER	—	—	A/D Comparison Function Window A Extended Input Comparison Condition Setting Register
ADCMPDR0	—	—	A/D Comparison Function Window A Lower Level Setting Register
ADCMPDR1	—	—	A/D Comparison Function Window A Upper Level Setting Register
ADCMPSR0	—	—	A/D Comparison Function Window A Channel Status Register 0
ADCMPSR1	—	—	A/D Comparison Function Window A Channel Status Register 1
ADCMPSER	—	—	A/D Comparison Function Window A Extended Input Channel Status Register
ADWINMON	—	—	A/D Comparison Function Window A/B Status Monitoring Register
ADCMPBNSR	—	—	A/D Comparison Function Window B Channel Select Register
ADWINLLB	—	—	A/D Comparison Function Window B Lower Level Setting Register
ADWINULB	—	—	A/D Comparison Function Window B Upper Level Setting Register
ADCMPBSR	—	—	A/D Comparison Function Window B Channel Status Register
ADPGADCR0	—	—	A/D Programmable Gain Amplifier Differential Input Control Register
ADVMONCR	—	—	A/D Internal Reference Voltage Monitoring Circuit Enable Register
ADVMONO	—	—	A/D Internal Reference Voltage Monitoring Circuit Output Enable Register

2.26 D/A Converter

Table 2.54 lists Comparison of Specifications for D/A Converter and Table 2.55 lists Comparison of Registers for D/A Converter.

Table 2.54 Comparison of Specifications for D/A Converter

Item	RX24T(DA, DAa)	RX66T(R12DAb)
Resolution	8 bits	12 bits
Output channels	One channel (chip version A) or Two channels (chip version B)	Two channels
Measure against mutual interference between analog modules	• Measure against interference between D/A and A/D conversion D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable input signal from the 12-bit A/D converter (unit 2). Therefore, the degradation of A/D conversion accuracy due to interference is reduced by controlling the timing in which the 8-bit D/A converter inrush current occurs, with the enable signal.	• Measure against interference between D/A and A/D conversion D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable signal from the 12-bit A/D converter (unit 2). Therefore, the degradation of A/D conversion accuracy due to interference is reduced by controlling the timing in which the 12-bit D/A converter inrush current occurs, with the enable signal.
Low power consumption function	Module stop state can be set.	Module stop state can be set.
Event link function (input)	—	DA0 conversion can be started when an event signal is input.
Destination Selection	—	Outputs to the external pin and to the comparator C are separately controllable.

Table 2.55 Comparison of Registers for D/A Converter

Register	Bit	RX24T(DA, DAa)	RX66T(R12DAb)
DACR	DAE	—	D/A Enable
DADSELR	—	—	D/A Destination Select Register

2.27 Comparator C

Table 2.56 lists Comparison of Specifications for Comparator C and Table 2.57 lists Comparison of Registers for Comparator C.

Table 2.56 Comparison of Specifications for Comparator C

Item	RX24T(CMPC)	RX66T(CMPC)
Number of channels	Four (comparator C0 to comparator C3)	Six (comparator C0 to comparator C5)
Analog input voltages	Input voltage to the CMPCnm pin (n = channel number; m = 0 to 3)	Input voltage from the CMPCnm pin (n = channel number; m = 0 to 3)
Reference input voltage	[Chip version A] Input voltage to the CVREFC0/CVREFC1 pin or on-chip D/A converter 0 output voltage [Chip version B] Output voltage from on-chip D/A converter 0 or on-chip D/A converter 1	Either of the output voltage from the on-chip D/A converter 0 or D/A converter 1, or the input voltage from the CVREFC0 or CVREFC1 pin Either of the output voltage from the on-chip D/A converter 0 or D/A converter 1, or the input voltage from the CVREFC0 or CVREFC1 pin
Comparison result	The comparison result can be output externally.	The comparison result can be output externally.
Digital filter function	• One of three sampling periods can be selected. • The filter function can also be disabled. • A noise-filtered signal can be used to generate the interrupt request output, POE source output, and GPT internal trigger source output, and the signal can be used to read the comparison result via registers.	• One of three sampling periods can be selected. • The filter function can also be disabled. • A noise-filtered signal can be used to generate the interrupt request output, event output to the ELC, and POE source output, and the signal can be used to read the comparison result via registers.
Interrupt request	• An interrupt request is generated upon detecting a valid edge of the comparison result. • Rising edge, falling edge, or both edges of the comparison result can be selected.	• An interrupt request is generated upon detecting a valid edge of the comparison result. • A valid edge can be selected from a rising or a falling edge or both edges.
Low power consumption function	Module stop state can be set.	Module stop state can be set.

Item	RX24T(CMPC)	RX66T(CMPC)
Precautions when the 12-bit A/D converter is in the module-stop state	The programmable gain amplifier (PGA) and 12-bit A/D converter are controlled by the same module-stop signal, so PGA output for the following pins cannot be compared when the 12-bit A/D converter is in the module-stop state. • PGA output for AN000 pin • PGA output for AN100 pin • PGA output for AN101 pin • PGA output for AN102 pin The comparison for the following analog input pins is possible since they are directly connected to the comparator. • AN000 pin • AN100 pin • AN101 pin • AN102 pin	The programmable gain amplifier (PGA) and 12-bit A/D converter are controlled by the same module-stop signal, so PGA output for the following pins cannot be compared when the 12-bit A/D converter is in the module-stop state. • PGA output for AN000 pin • PGA output for AN001 pin • PGA output for AN002 pin • PGA output for AN100 pin • PGA output for AN101 pin • PGA output for AN102 pin The comparison for the following analog input pins is not possible. • AN000 pin • AN001 pin • AN002 pin • AN100 pin • AN101 pin • AN102 pin

Table 2.57 Comparison of Registers for Comparator C

Register	Bit	RX24T(CMPC)	RX66T(CMPC)
CMPSEL0	CMPSEL[3:0]	Comparator Input Select ● Comparator C0 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC00 selected 0 0 1 0: CMPC01 selected 0 1 0 0: CMPC02 selected 1 0 0 0: CMPC03 selected Settings other than above are prohibited. ● Comparator C1 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC10 selected 0 0 1 0: CMPC11 selected 0 1 0 0: CMPC12 selected 1 0 0 0: CMPC13 selected Settings other than above are prohibited. ● Comparator C2 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC20 selected 0 0 1 0: CMPC21 selected 0 1 0 0: CMPC22 selected 1 0 0 0: CMPC23 selected Settings other than above are prohibited. ● Comparator C3 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC30 selected 0 0 1 0: CMPC31 selected 0 1 0 0: CMPC32 selected 1 0 0 0: CMPC33 selected Settings other than above are prohibited.	Comparator Input Select ● Comparator C0 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC00 selected 0 0 1 0: CMPC01 selected 0 1 0 0: CMPC02 selected 1 0 0 0: CMPC03 selected Settings other than above are prohibited. ● Comparator C1 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC10 selected 0 0 1 0: CMPC11 selected 0 1 0 0: CMPC12 selected 1 0 0 0: CMPC13 selected Settings other than above are prohibited. ● Comparator C2 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC20 selected 0 0 1 0: CMPC21 selected 0 1 0 0: CMPC22 selected 1 0 0 0: CMPC23 selected Settings other than above are prohibited. ● Comparator C3 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC30 selected 0 0 1 0: CMPC31 selected 0 1 0 0: CMPC32 selected 1 0 0 0: CMPC33 selected Settings other than above are prohibited. ● Comparator C4 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC40 selected 0 0 1 0: CMPC41 selected 0 1 0 0: CMPC42 selected 1 0 0 0: CMPC43 selected Settings other than above are prohibited.

Register	Bit	RX24T(CMPC)	RX66T(CMPC)
CMPSEL0	CMPSEL[3:0]		• Comparator C5 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC50 selected 0 0 1 0: CMPC51 selected 0 1 0 0: CMPC52 selected 1 0 0 0: CMPC53 selected Settings other than above are prohibited.
CMPSEL1	CVRS[1:0](RX24T) CVRS[3:0](RX66T)	Reference Input Voltage Select [Chip version A] • Comparator C0 b1 b0 0 0: No input 0 1: Input voltage to the CVREFC0 pin selected as reference input voltage 1 0: On-chip D/A converter 0 output voltage selected as reference input voltage Settings other than above are prohibited. • Comparator C1 to comparator C3 b1 b0 0 0: No input 0 1: Input voltage to the CVREFC1 pin selected as reference input voltage 1 0: On-chip D/A converter 0 output voltage selected as reference input voltage Settings other than above are prohibited.	Reference Input Voltage Select b3 b0 0 0 0 0: No input 0 0 0 1: On-chip D/A converter 1 output voltage selected as reference input voltage 0 0 1 0: On-chip D/A converter 0 output voltage selected as reference input voltage 0 1 0 0: Input voltage to the CVREFC1 pin selected as reference input voltage 1 0 0 0: Input voltage to the CVREFC0 pin selected as reference input voltage Settings other than above are prohibited. b3 b0 0 0 0 0: No input 0 0 0 1: On-chip D/A converter 1 output voltage selected as reference input voltage 0 0 1 0: On-chip D/A converter 0 output voltage selected as reference input voltage 0 1 0 0: Input voltage to the CVREFC1 pin selected as reference input voltage 1 0 0 0: Input voltage to the CVREFC0 pin selected as reference input voltage Settings other than above are prohibited.

Register	Bit	RX24T(CMPC)	RX66T(CMPC)
CMPSEL1	CVRS[1:0](RX24T) CVRS[3:0](RX66T)	[Chip version B] b1 b0 0 0: No input 0 1: On-chip D/A converter 1 output voltage selected as reference input voltage 1 0: On-chip D/A converter 0 output voltage selected as reference input voltage Settings other than above are prohibited.	 b3 b0 0 0 0 0: No input 0 0 0 1: On-chip D/A converter 1 output voltage selected as reference input voltage 0 0 1 0: On-chip D/A converter 0 output voltage selected as reference input voltage 0 1 0 0: Input voltage to the CVREFC1 pin selected as reference input voltage 1 0 0 0: Input voltage to the CVREFC0 pin selected as reference input voltage Settings other than above are prohibited.

2.28 Data Operation Circuit

Table 2.58 lists Comparison of Specifications for Data Operation Circuit.

Table 2.58 Comparison of Specifications for Data Operation Circuit

Item	RX24T(DOC)	RX66T(DOC)
Data operation function	16-bit data comparison, addition, and subtraction	16-bit data comparison, addition, and subtraction
Lower power consumption function	Module stop state can be set.	Module stop state can be set.
Interrupts	• The compared values either match or mismatch • The result of data addition is greater than FFFFh • The result of data subtraction is less than 0000h	• The compared values either match or mismatch • The result of data addition is greater than FFFFh • The result of data subtraction is less than 0000h
Event link function (output)	—	• The compared values either match or mismatch • The result of data addition is greater than FFFFh • The result of data subtraction is less than 0000h

2.29 RAM

Table 2.59 lists Comparison of RAM Specifications and Table 2.60 lists Comparison of RAM Registers.

Table 2.59 Comparison of RAM Specifications

Item	RX24T(RAM)	RX66T	
		Without ECC Error Correction (RAM)	With ECC Error Correction (ECCRAM)
Capacity	32 Kbytes, 16 Kbytes	64 Kbytes, 128 Kbytes	16 Kbytes
Memory bus	Memory bus 1	Memory bus 1	Memory bus 3
Access	• Single-cycle access is possible for both reading and writing. • On-chip RAM can be enabled or disabled.	• Single-cycle access is possible for both reading and writing. • Enabling or disabling of the RAM is selectable.	Enabling or disabling of the ECC function is selectable. [When MEMWAIT is set to 0] • The ECC function is disabled: Access takes two cycles whether for reading or writing. • The ECC function is enabled (when no error has occurred): Access takes two cycles whether for reading or writing. • The ECC function is enabled (when an error has occurred): Access takes three cycles whether for reading or writing. [When MEMWAIT is set to 1] • The ECC function is disabled: Access takes three cycles whether for reading or writing. • The ECC function is enabled (when no error has occurred): Reading takes three cycles and writing takes four cycles. • The ECC function is enabled (when an error has occurred): Access takes five cycles whether for reading or writing.
Address	• RAM capacity: 32 Kbytes 0000 0000h to 0000 7FFFh • RAM capacity: 16 Kbytes 0000 0000h to 0000 3FFFh	• RAM capacity: 64 Kbytes 0000 0000h to 0000 FFFFh • RAM capacity: 128 Kbytes 0000 0000h to 0001 FFFFh	00FF C000h to 00FF FFFFh
Data retention function	—	Not available in deep software standby mode	

Item	RX24T(RAM)	RX66T	
		Without ECC Error Correction (RAM)	With ECC Error Correction (ECCRAM)
Low power consumption function	The module stop state is selectable for RAM0.	Transition to the module stop state is separately possible for the RAM and ECCRAM.	
Error checking	—	• Detection of 1-bit errors • A non-maskable interrupt or interrupt is generated in response to an error.	• ECC Error Correction: Correction of 1-bit errors and detection of 2-bit errors • A non-maskable interrupt or interrupt is generated in response to an error.

Table 2.60 Comparison of RAM Registers

Register	Bit	RX24T(RAM)	RX66T(RAM,ECCRAM)
ECCRAMMODE	—	—	ECCRAM Operating Mode Control Register
ECCRAM2STS	—	—	ECCRAM 2-Bit Error Status Register
ECCRAM1STSEN	—	—	ECCRAM 1-Bit Error Information Update Enable Register
ECCRAM1STS	—	—	ECCRAM 1-Bit Error Status Register
ECCRAMPRCR	—	—	ECCRAM Protection Register
ECCRAM2ECAD	—	—	ECCRAM 2-Bit Error Address Capture Register
ECCRAM1ECAD	—	—	ECCRAM 1-Bit Error Address Capture Register
ECCRAMPRCR2	—	—	ECCRAM Protection Register 2
ECCRAMETST	—	—	ECCRAM Test Control Register
RAMMODE	—	—	RAM Operating Mode Control Register
RAMSTS	—	—	RAM Error Status Register
RAMECAD	—	—	RAM Error Address Capture Register
RAMPRCR	—	—	RAM Protection Register

2.30 Flash Memory

Table 2.61 lists Comparison of Specifications for Flash Memory and Table 2.62 lists Comparison of Registers for the Flash Memory.

Table 2.61 Comparison of Specifications for Flash Memory

Item	RX24T		RX66T	
	ROM	E2 DataFlash	Code Flash Memory	Data Flash Memory
Memory capacity	• User area: 512 Kbytes, 384 Kbytes, 256 Kbytes, 128 Kbytes	Data area: 8 Kbytes	• User area: 1 Mbyte, 512 Kbytes, 256 Kbytes • User boot area: 32 Kbytes	Data area: 32 Kbytes
ROM cache	• Cache size: 2 Kbytes		• Capacity: 8 Kbytes • Mapping method: direct mapping • Line size: 16 bytes	—
Read cycle	No ROM wait cycles when ICLK ≤ 32 MHz, ROM wait cycle when ICLK > 32 MHz	—	• While ROM cache operation is enabled: When the cache is hit, one cycle; When the cache is missed, - One to two cycles if ICLK ≤ 120 MHz - Two to three cycles if ICLK > 120 MHz • When ROM cache operation is disabled: - One cycle if ICLK ≤ 120 MHz - Two cycles if ICLK > 120 MHz	A read operation takes eight cycles of FCLK in word or byte access
Value after erasure	FFh	FFh	FFh	Undfined
Interrupt	An interrupt (FRDYI) is generated upon completion of software command processing or forced stop processing.		• A flash ready interrupt request (FRDYI) is generated upon completion of FACI command execution. • An interrupt or a code flash memory access error interrupt (FIFERR) is generated when the flash sequencer transitions to the command-lock state.	• A flash ready interrupt request (FRDYI) is generated upon completion of FACI command execution. • An interrupt or a data flash memory access error interrupt (FIFERR) is generated when the flash sequencer transitions to the command-lock state.

Item	RX24T		RX66T	
	ROM	E2 DataFlash	Code Flash Memory	Data Flash Memory
Programming /erasing method	• The following commands are implemented: Program, blank check, block erase, all-block erase • The following commands are implemented for programming the extra area: Start-up area information program, access window information program		• The dedicated sequencer (FCU) is incorporated for programming of the flash memory. • Programming and erasing the code flash memory/data flash memory is handled by the FACI commands specified in the FACI command issuing area (007E 0000h). • Programming/erasure through transfer by a flash-memory programmer via a serial interface (serial programming) • Programming/erasure of flash memory by a user program (self-programming)	
Security function	Protects against illicit tampering with or reading out of data in flash memory		Protects against illicit tampering with or reading out of data in flash memory	
Protection function	Protects against erroneous rewriting of the flash memory		Protects against erroneous rewriting of the flash memory	
Trusted memory (TM) function	—		Protects against illicit reading of blocks 8 and 9 in the code flash memory	
Background operation (BGO)	• Programs on the ROM can be executed while rewriting the E2 DataFlash.		• The user area can be read while the data area is being programmed or erased.	
Units of programming and erasure	• Units of programming for the user area: 8 bytes • Units of erasure for the user area: Block units	• Unit of programming for the data area: 1 bytes • Unit of erasure for the data area: Block units	• Units of programming for the user area or user boot area: 256 bytes • Units of erasure for the user area: Block units	• Unit of programming for the data area: 4 bytes • Unit of erasure for the data area: Block units
Other functions	—		Interrupts can be accepted during self-programming.	

Item	RX24T		RX66T	
	ROM	E2 DataFlash	Code Flash Memory	ROM
On-board programming (Serial programming/ Self-programming)	Boot mode (SCI) • Channel 1 of the serial communications interface (SCI1) is used for asynchronous serial communication. • The transfer rate is adjusted automatically. • The user area and data area are rewritable. Boot mode (FINE interface) • The FINE is used. • The user area and data area are rewritable. Self-programming in single-chip mode • The user area and data area are rewritable using the flash rewrite routine in the user program.		Programming/erasure in boot mode (for the SCI interface) • The asynchronous serial interface (SCI1) is used. • The transfer rate is adjusted automatically. • The user boot area can also be programmed or erased. Programming/erasure in boot mode (for the FINE interface) • FINE is used. Programming/erasure in boot mode (for the USB interface) • USBb is used. • Dedicated hardware is not required, so direct connection to a PC is possible. Programming/erasure in user boot mode • Able to create original boot programs of the user's making. Programming/erasure by self-programming • This allows user area/data area programming and erasure without resetting the system.	
Off-board programming (Programming and Erasure by Parallel Programmer)	The user area and data area are rewritable using a flash programmer (serial programmer or parallel programmer) compatible with this MCU.		Programming and erasure of the user area and user boot area by using a parallel programmer is possible.	Programming or erasure of the data area by a parallel programmer is not possible.
Unique ID	A 16-byte ID code provided for each MCU		A 12-byte ID code provided for each MCU	

Table 2.62 Comparison of Registers for the Flash Memory

Register	Bit	RX24T	RX66T
DFLCTL	—	E2 DataFlash Control Register	—
FENTRYR	FENTRY0(RX24T) FENTRYC(RX66T)	ROM P/E Mode Entry 0	Code Flash Memory P/E Mode Entry
	FEKEY[7:0](RX24T) KEY[7:0](RX66T)	Key Code	Key Code
FPR	—	Protection Unlock Register	—
FPSR	—	Protection Unlock Status Register	—
FPMCR	—	Flash P/E Mode Control Register	—
FISR	—	Flash Initial Setting Register	—
FRESETR	—	Flash Reset Register	—
FASR	—	Flash Area Select Register	—
FCR	—	Flash Control Register	—
FEXCR	—	Flash Extra Area Control Register	—
FSARH	—	Flash Processing Start Address Register H	—
FSARL	—	Flash Processing Start Address Register L	—
FEARH	—	Flash Processing End Address Register H	—
FEARL	—	Flash Processing End Address Register L	—
FWBn	—	Flash Write Buffer n Register (n = 0 to 3)	—
FSTATR0 (RX24T) FSTATR (RX66T)	ERERR (RX24T) ERSERR (RX66T)	Erase Error Flag (b0)	Erasure Error Flag (b13)
	PRGERR	Program Error Flag (b1)	Programming Error Flag (b12)
	BCERR	Blank Check Error Flag	—
	ILGLERR	Illegal Command Error Flag (b4)	Illegal Error Command Flag (b14)
	EILGLERR	Extra Area Illegal Command Error Flag	—
	FLWEERR	—	Flash Write/Erase Protect Error Flag
	PRGSPD	—	Programming Suspend Status Flag
	ERSSPD	—	Erasure Suspend Status Flag
	DBFULL	—	Data Buffer Full Flag
	SUSRDY	—	Suspend Ready Flag
	FRDY	—	Flash Ready Flag
FSTATR1	—	Flash Status Register 1	—
FEAMH	—	Flash Error Address Monitor Register H	—
FEAML	—	Flash Error Address Monitor Register L	—
FSCMR	—	Flash Start-Up Setting Monitor Register	—
FAWSMR	—	Flash Access Window Start Address Monitor Register	—
FAWEMR	—	Flash Access Window End Address Monitor Register	—
UIDRn	—	Unique ID Register n (n = 0 to 3)	Unique ID Register n (n = 0 to 2)

Register	Bit	RX24T	RX66T
NCRGn	—	—	Non-Cacheable Area n Address Register (n = 0, 1)
NCRCn	—	—	Non-Cacheable Area n Setting Register (n = 0, 1)
FWEPROR	—	—	Flash P/E Protect Register
FASTAT	—	—	Flash Access Status Register
FAEINT	—	—	Flash Access Error Interrupt Enable Register
FRDYIE	—	—	Flash Ready Interrupt Enable Register
FSADDR	—	—	FACI Command Processing Start Address Register
FEADDR	—	—	FACI Command Processing End Address Register
FPROTR	—	—	Flash Protection Register
FSUINITR	—	—	Flash Sequencer Set-Up Initialization Register
FLKSTAT	—	—	Lock Bit Status Register
FCMDR	—	—	FACI Command Register
FPESTAT	—	—	Flash P/E Status Register
FBCCNT	—	—	Data Flash Blank Check Control Register
FBCSTAT	—	—	Data Flash Blank Check Status Register
FPSADDR	—	—	Data Flash Programming Start Address Register
FCPSR	—	—	Flash Sequencer Processing Switching Register
FPCKAR	—	—	Flash Sequencer Processing Clock Frequency Notification Register

3. Comparison of Pin Functions

This section describes comparison of pin functions as well as comparison of pins for power supply, clocks, and system control. The item which exists only in either of the Group is indicated by blue text. The item which exists in both Groups with different specifications is indicated by red text. **Black text** indicates there is no differences in specifications of the item between Groups.

3.1 100-Pin Package (RX24T: Chip Version B, RX66T: With PGA Pseudo-Differential Input and USB Pins)

Table 3.1 lists Comparison of Pin Functions for 100-Pin Packages (RX24T: Chip Version B, RX66T: With PGA Pseudo-Differential Input and USB Pins).

Table 3.1 Comparison of Pin Functions for 100-Pin Packages (RX24T: Chip Version B, RX66T: With PGA Pseudo-Differential Input and USB Pins)

100 Pins	RX24T (Chip Version B)	RX66T (with PGA pseudo-differential input and USB pins)
1	PE5/IRQ0	PE5/BCLK/MTIOC9D/MTIOC9D#/GTIOC3A/GTETRGB/GTIOC3A#/GTETRGD/SCK9/CTS9#/RTS9#/SS9#/IRQ0/ADST0
2	P02/MTIOC9D/MTIOC9D#/CTS1#/RTS1#/SS1#/IRQ5/ADST0	EMLE
3	VSS	VSS
4	P00/IRQ2/ADST1	UB/P00/A11/MTIOC9A/MTIOC9A#/CACREF/RXD9/SMISO9/SSCL9/RXD12/SMISO12/SSCL12/RXDX12/IRQ2/ADST1/COMP0
5	VCL	VCL
6	MD/FINED	MD/FINED
7	P01/POE12#/IRQ4/ADST2	P01/A10/MTIOC9C/MTIOC9C#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE12#/TXD9/SMOSI9/SSDA9/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/IRQ4/ADST2/COMP1
8	PE4/MTCLKC/MTCLKC#/POE10#/IRQ1	PE4/A9/MTCLKC/MTCLKC#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE10#/SCK9/IRQ1
9	PE3/MTCLKD/MTCLKD#/POE11#/IRQ2	PE3/A8/MTCLKD/MTCLKD#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE11#/CTS9#/RTS9#/SS9#/IRQ2_DS
10	RES#	RES#
11	XTAL/P37	XTAL/P37
12	VSS	VSS
13	EXTAL/P36	EXTAL/P36
14	VCC	VCC
15	PE2/POE10#/NMI	UPSEL/PE2/POE10#/NMI
16	PE1/MTIOC9D/MTIOC9D#/TMO5/CTS5#/RTS5#/SS5#/SSLA3	PE1/WR0#/WR#/MTIOC9D/MTIOC9D#/TMO5/CTS5#/RTS5#/SS5#/CTS12#/RTS12#/SS12#/SSLA3/IRQ15
17	PE0/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/SSCL5/SSLA2	PE0/WR1#/BC1#/WAIT#/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/SSCL5/SSLA2/CRX0/USB0_OVRCURB/IRQ7
18	PD7/MTIOC9A/MTIOC9A#/TMRI1/TMRI5/GTIOC3A/GTIOC3A#/TXD5/SMOSI5/SSDA5/SSLA1	TRST#/PD7/MTIOC9A/MTIOC9A#/GTIOC0A/GTIOC3A/GTIOC0A#/GTIOC3A#/TMRI1/TMRI5/TXD5/SMOSI5/SSDA5/SSLA1/CTX0/IRQ8

100 Pins	RX24T (Chip Version B)	RX66T (with PGA pseudo-differential input and USB pins)
19	PD6/MTIOC9C/MTIOC9C#/TMO1/ GTIOC3B/GTIOC3B#/CTS1#/RTS1#/SS1#/ SSLA0/IRQ5/ADST0	TMS/PD6/MTIOC9C/MTIOC9C#/GTIOC0B/ GTIOC3B/GTIOC0B#/GTIOC3B#/TMO1/ CTS1#/RTS1#/SS1#/CTS11#/RTS11#/ SS11#/SSLA0/IRQ5/ADST0
20	PD5/TMRI0/TMRI6/GTECLKA/RXD1/ SMISO1/SSCL1/IRQ3	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/ TMRI0/TMRI6/RXD1/SMISO1/SSCL1/ RXD11/SMISO11/SSCL11/IRQ6
21	PD4/TMCI0/TMCI6/GTECLKB/SCK1/IRQ2	TCK/PD4/GTIOC1B/GTETRGB/ GTIOC1B#/TMCI0/TMCI6/SCK1/SCK11/IRQ2
22	PD3/TMO0/GTECLKC/TXD1/SMOSI1/ SSDA1	TDO/PD3/GTIOC2A/GTETRGC/GTIOC2A#/ TMO0/TXD1/SMOSI1/SSDA1/TXD11/ SMOSI11/SSDA11
23	PD2/TMCI1/TMO4/GTIOC0A/GTIOC0A#/ SCK5/MOSIA	TRCLK/PD2/A7/GTIOC2B/GTIOC0A/ GTIOC2B#/GTIOC0A#/TMCI1/TMO4/ SCK5/SCK8/MOSIA/USB0_VBUS
24	PD1/TMO2/GTIOC0B/GTIOC0B#/MISOA	USB0_DM
25	PD0/TMO6/GTIOC1A/GTIOC1A#/RSPCKA	USB0_DP
26	PB7/GTIOC1B/GTIOC1B#/SCK5	VCC_USB
27	PB6/GTIOC2A/GTIOC2A#/RXD5/SMISO5/ SSCL5/IRQ5	TRDATA0/PB6/A3/GTIOC2A/GTIOC2A#/ RXD5/SMISO5/SSCL5/RXD11/SMISO11/ SSCL11/RXD12/SMISO12/SSCL12/ RXDX12/CRX0/USB0_OVRCURA/IRQ2
28	PB5/GTIOC2B/GTIOC2B#/TXD5/SMOSI5/ SSDA5	TRSYNC/PB5/A2/GTIOC2B/GTIOC2B#/ TXD5/SMOSI5/SSDA5/TXD11/SMOSI11/ SSDA11/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/CTX0/USB0_VBUSEN
29	VCC	VCC
30	PB4/POE8#/GTETRG/GTECLKD/CTS5#/ RTS5#/SS5#/IRQ3	PB4/A1/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE8#/CTS5#/RTS5#/SS5#/ SCK11/CTS11#/RTS11#/SS11#/ USB0_OVRCURB/IRQ3_DS
31	VSS	VSS/VSS_USB
32	PB3/MTIOC0A/MTIOC0A#/CACREF/SCK6/ RSPCKA	PB3/A7/MTIOC0A/MTIOC0A#/CACREF/ SCK6/RSPCKA/IRQ9
33	PB2/MTIOC0B/MTIOC0B#/TMRI0/ADSM0/ TXD6/SMOSI6/SSDA6/SDA0	PB2/A6/MTIOC0B/MTIOC0B#/GTADSM0/ TMRI0/TXD6/SMOSI6/SSDA6/SDA/ADSM0
34	PB1/MTIOC0C/MTIOC0C#/TMCI0/ADSM1/ RXD6/SMISO6/SSCL6/SCL0	PB1/A5/MTIOC0C/MTIOC0C#/GTADSM1/ TMCI0/RXD6/SMISO6/SSCL6/SCL/IRQ4/ ADSM1
35	PB0/MTIOC0D/MTIOC0D#/TMO0/TXD6/ SMOSI6/SSDA6/MOSIA/ADTRG2#	PB0/A0/A4/BC0#/MTIOC0D/MTIOC0D#/ TMO0/TXD6/SMOSI6/SSDA6/CTS11#/ RTS11#/SS11#/MOSIA/IRQ8/ADTRG2#
36	PA5/MTIOC1A/MTIOC1A#/TMCI3/RXD6/ SMISO6/SSCL6/MISOA/IRQ1/ADTRG1#	PA5/A3/MTIOC1A/MTIOC1A#/TMCI3/ RXD6/SMISO6/SSCL6/RXD8/SMISO8/ SSCL8/MISOA/IRQ1/ADTRG1#
37	PA4/MTIOC1B/MTIOC1B#/TMCI7/SCK6/ RSPCKA/ADTRG0#	PA4/A2/MTIOC1B/MTIOC1B#/TMCI7/ SCK6/TXD8/SMOSI8/SSDA8/RSPCKA/ ADTRG0#
38	PA3/MTIOC2A/MTIOC2A#/TMRI7/ GTADSM0/SSLA0	PA3/A1/MTIOC2A/MTIOC2A#/GTADSM0/ TMRI7/TXD9/SMOSI9/SSDA9/SCK8/SSLA0
39	PA2/MTIOC2B/MTIOC2B#/TMO7/ GTADSM1/CTS6#/RTS6#/SS6#/SSLA1	PA2/A0/BC0#/MTIOC2B/MTIOC2B#/ GTADSM1/TMO7/CTS6#/RTS6#/SS6#/ RXD9/SMISO9/SSCL9/SCK11/SSLA1

100 Pins	RX24T (Chip Version B)	RX66T (with PGA pseudo-differential input and USB pins)
40	PA1/MTIOC6A/MTIOC6A#/TMO4/SSLA2/ CRXD0/ADTRG0#	PA1/MTIOC6A/MTIOC6A#/TMO4/TXD9/ SMOSI9/SSDA9/RXD11/SMISO11/SSCL11/ SSLA2/CRX0/USB0_ID/USB0_OVRCURA/ IRQ14_DS/ADTRG0#
41	PA0/MTIOC6C/MTIOC6C#/TMO2/SSLA3/ CTXD0	PA0/MTIOC6C/MTIOC6C#/TMO2/SCK9/ TXD11/SMOSI11/SSDA11/SSLA3/CTX0/ USB0_EXICEN/USB0_VBUSEN
42	VCC	VCC
43	P96/POE4#/IRQ4	P96/CS0#/WAIT#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE4#/CTS8#/ RTS8#/SS8#/IRQ4_DS
44	VSS	VSS
45	P95/MTIOC6B/MTIOC6B#	P95/MTIOC6B/MTIOC6B#/GTIOC4A/ GTIOC7A/GTIOC4A#/GTIOC7A#
46	P94/MTIOC7A/MTIOC7A#	P94/MTIOC7A/MTIOC7A#/GTIOC5A/ GTIOC8A/GTIOC5A#/GTIOC8A#
47	P93/MTIOC7B/MTIOC7B#	P93/MTIOC7B/MTIOC7B#/GTIOC6A/ GTIOC9A/GTIOC6A#/GTIOC9A#
48	P92/MTIOC6D/MTIOC6D#	P92/MTIOC6D/MTIOC6D#/GTIOC4B/ GTIOC7B/GTIOC4B#/GTIOC7B#
49	P91/MTIOC7C/MTIOC7C#	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC8B/GTIOC5B#/GTIOC8B#
50	P90/MTIOC7D/MTIOC7D#	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC9B/GTIOC6B#/GTIOC9B#
51	P76/MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC2B#	P76/D0[A0/D0]/MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC6B/GTIOC2B#/GTIOC6B#
52	P75/MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC1B#	P75/D1[A1/D1]/MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#
53	P74/MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC0B#	P74/D2[A2/D2]/MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#
54	P73/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC2A#	P73/D3[A3/D3]/MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC6A/GTIOC2A#/GTIOC6A#
55	P72/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC1A#	P72/D4[A4/D4]/MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC5A/GTIOC1A#/GTIOC5A#
56	P71/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC0A#	P71/D5[A5/D5]/MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC4A/GTIOC0A#/GTIOC4A#
57	P70/POE0#/IRQ5	P70/D6[A6/D6]/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE0#/CTS9#/ RTS9#/SS9#/IRQ5_DS
58	P33/MTIOC3A/MTIOC3A#/MTCLKA/ MTCLKA#/TMO0/SSLA3	P33/D7[A7/D7]/MTIOC3A/MTCLKA/ MTIOC3A#/MTCLKA#/GTIOC3B/ GTIOC3B#/TMO0/SSLA3/IRQ13_DS
59	P32/MTIOC3C/MTIOC3C#/MTCLKB/ MTCLKB#/TMO6/SSLA2	P32/D8[A8/D8]/MTIOC3C/MTCLKB/ MTIOC3C#/MTCLKB#/GTIOC3A/ GTIOC3A#/TMO6/SSLA2/IRQ12_DS
60	VCC	VCC
61	P31/MTIOC0A/MTIOC0A#/MTCLKC/ MTCLKC#/TMRI6/SSLA1/IRQ6	P31/D9[A9/D9]/MTIOC0A/MTCLKC/ MTIOC0A#/MTCLKC#/TMRI6/SSLA1/IRQ6
62	VSS	VSS
63	P30/MTIOC0B/MTIOC0B#/MTCLKD/ MTCLKD#/TMCI6/SSLA0/IRQ7/COMP3	P30/D10[A10/D10]/MTIOC0B/MTCLKD/ MTIOC0B#/MTCLKD#/TMCI6/SCK8/ CTS8#/RTS8#/SS8#/SSLA0/IRQ7/COMP3
64	P24/MTIC5U/MTIC5U#/TMCI2/TMO6/ RSPCKA/COMP0/DA0	P27/CS3#/MTIOC1A/MTIOC0C/ MTIOC1A#/MTIOC0C#/POE9#/IRQ15

100 Pins	RX24T (Chip Version B)	RX66T (with PGA pseudo-differential input and USB pins)
65	P23/MTIC5V/MTIC5V#/TMO2/CACREF/ MOSIA/COMP1/DA1	P24/D11[A11/D11]/MTIC5U/MTIC5U#/ TMCI2/TMO6/CTS8#/RTS8#/SS8#/SCK8/ RSPCKA/IRQ4/COMP0
66	P22/MTIC5W/MTIC5W#/TMRI2/TMO4/ MISOA/ADTRG2#/COMP2	P23/D12[A12/D12]/MTIC5V/MTIC5V#/ TMO2/CACREF/TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/SSDA12/TXDX12/ SIOX12/MOSIA/CTX0/IRQ11/COMP1
67	P21/MTCLKA/MTCLKA#/MTIOC9A/ MTIOC9A#/TMCI4/IRQ6/ADTRG1#/AN116	P22/D13[A13/D13]/MTIC5W/MTCLKD/ MTIC5W#/MTCLKD#/MTIOC9B/TMRI2/ TMO4/RXD8/SMISO8/SSCL8/RXD12/ SMISO12/SSCL12/RXDX12/MISOA/CRX0/ IRQ10/ADTRG2#/COMP2
68	P20/MTCLKB/MTCLKB#/MTIOC9C/ MTIOC9C#/TMRI4/IRQ7/ADTRG0#/AN016	P21/D14[A14/D14]/MTIOC9A/MTCLKA/ MTIOC9A#/MTCLKA#/TMCI4/TXD8/ SMOSI8/SSDA8/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/MOSIA/ IRQ6_DS/AN217/ADTRG1#/COMP5
69	P65/AN205	P20/D15[A15/D15]/MTIOC9C/MTCLKB/ MTIOC9C#/MTCLKB#/TMRI4/CTS8#/ RTS8#/SS8#/SCK8/RSPCKA/IRQ7_DS/ AN216/ADTRG0#/COMP4
70	P64/AN204	P65/A12/IRQ9/AN211/CMPC53/DA1
71	AVCC2	P64/A13/IRQ8/AN210/CMPC33/DA0
72	VREF	AVCC2
73	AVSS2	AVSS2
74	P63/AN203/IRQ7	P63/A12/A14/IRQ7/AN209/CMPC23
75	P62/AN202/IRQ6	P62/A13/A15/IRQ6/AN208/CMPC43
76	P61/AN201/IRQ5	P61/A14/A16/IRQ5/AN207/CMPC13
77	P60/AN200/IRQ4	P60/A15/A17/IRQ4/AN206/CMPC03
78	P55/AN211/IRQ3	P55/A16/A18/IRQ3/AN203/CMPC32
79	P54/AN210/IRQ2	P54/A17/A19/IRQ2/AN202/CMPC22
80	P53/AN209/IRQ1	P53/A18/A20/IRQ1/AN201/CMPC12
81	P52/AN208/IRQ0	P52/IRQ0/AN200/CMPC02
82	P51/AN207	P47/AN103
83	P50/AN206	P46/AN102/CMPC50/CMPC51
84	P47/AN103	P45/AN101/CMPC40/CMPC41
85	P46/AN102/CMPC12/CMPC13/CMPC30/ CMPC31	P44/AN100/CMPC30/CMPC31
86	P45/AN101/CMPC02/CMPC03/CMPC20/ CMPC21	PH4/AN107/PGAVSS1
87	P44/AN100/CMPC10/CMPC11/CMPC32/ CMPC33	P43/AN003
88	P43/AN003	P42/AN002/CMPC20/CMPC21
89	P42/AN002	P41/AN001/CMPC10/CMPC11
90	P41/AN001	P40/AN000/CMPC00/CMPC01
91	P40/AN000/CMPC00/CMPC01/CMPC22/ CMPC23	PH0/AN007/PGAVSS0
92	AVCC1	AVCC1
93	AVCC0	AVCC0
94	AVSS0	AVSS0
95	AVSS1	AVSS1
96	P82/MTIC5U/MTIC5U#/TMO4/SCK6	P82/ALE/WAIT#/MTIC5U/MTIC5U#/ TMO4/SCK6/SCK12/IRQ3/COMP5

100 Pins	RX24T (Chip Version B)	RX66T (with PGA pseudo-differential input and USB pins)
97	P81/MTIC5V/MTIC5V#/TMCI4/TXD6/ SMOSI6/SSDA6	P81/CS2#/MTIC5V/MTIC5V#/TMCI4/ TXD6/SMOSI6/SSDA6/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/COMP4
98	P80/MTIC5W/MTIC5W#/TMRI4/RXD6/ SMISO6/SSCL6	P80/CS1#/MTIC5W/MTIC5W#/TMRI4/ RXD6/SMISO6/SSCL6/RXD12/SMISO12/ SSCL12/RXDX12/IRQ5/COMP3
99	P11/MTIOC3A/MTIOC3A#/MTCLKC/ MTCLKC#/TMO3/IRQ1	P11/RD#/MTIOC3A/MTCLKC/ MTIOC3A#/MTCLKC#/MTIOC9D/ GTIOC3B/GTETRGA/GTIOC3B#/ GTETRGC/TMO3/POE9#/IRQ1_DS
100	P10/MTIOC9B/MTIOC9B#/MTCLKD/ MTCLKD#/TMRI3/POE12#/CTS6#/RTS6#/ SS6#/IRQ0	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/GTETRGB/GTETRGD/TMRI3/ POE12#/CTS6#/RTS6#/SS6#/IRQ0_DS

3.2 100-Pin Package (RX24T: Chip Version B, RX66T: With PGA Pseudo-Differential Input and Without USB Pins)

Table 3.2 lists Comparison of Pin Functions for 100-Pin Packages (RX24T: Chip Version B, RX66T: With PGA Pseudo-Differential Input and Without USB Pins).

Table 3.2 Comparison of Pin Functions for 100-Pin Packages (RX24T: Chip Version B, RX66T: With PGA Pseudo-Differential Input and Without USB Pins)

100 Pins	RX24T (Chip Version B)	RX66T (with PGA pseudo-differential input and without USB pins)
1	PE5/IRQ0	PE5/BCLK/MTIOC9D/MTIOC9D#/GTIOC3A/ GTETRGB/GTIOC3A#/GTETRGD/SCK9/ CTS9#/RTS9#/SS9#/IRQ0/ADST0
2	P02/MTIOC9D/MTIOC9D#/CTS1#/RTS1#/ SS1#/IRQ5/ADST0	EMLE
3	VSS	VSS
4	P00/IRQ2/ADST1	UB/P00/A11/MTIOC9A/MTIOC9A#/CACREF/ RXD9/SMISO9/SSCL9/RXD12/SMISO12/ SSCL12/RXDX12/IRQ2/ADST1/COMP0
5	VCL	VCL
6	MD/FINED	MD/FINED
7	P01/POE12#/IRQ4/ADST2	P01/A10/MTIOC9C/MTIOC9C#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE12#/ TXD9/SMOSI9/SSDA9/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/IRQ4/ADST2/ COMP1
8	PE4/MTCLKC/MTCLKC#/POE10#/IRQ1	PE4/A9/MTCLKC/MTCLKC#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE10#/ SCK9/IRQ1
9	PE3/MTCLKD/MTCLKD#/POE11#/IRQ2	PE3/A8/MTCLKD/MTCLKD#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE11#/ CTS9#/RTS9#/SS9#/IRQ2_DS
10	RES#	RES#
11	XTAL/P37	XTAL/P37
12	VSS	VSS
13	EXTAL/P36	EXTAL/P36
14	VCC	VCC
15	PE2/POE10#/NMI	PE2/POE10#/NMI
16	PE1/MTIOC9D/MTIOC9D#/TMO5/CTS5#/ RTS5#/SS5#/SSLA3	PE1/WR0#/WR#/MTIOC9D/MTIOC9D#/ TMO5/CTS5#/RTS5#/SS5#/CTS12#/ RTS12#/SS12#/SSLA3/IRQ15
17	PE0/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/ RXD5/SMISO5/SSCL5/SSLA2	PE0/WR1#/BC1#/WAIT#/MTIOC9B/ MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/ SSCL5/SSLA2/CRX0/IRQ7
18	PD7/MTIOC9A/MTIOC9A#/TMRI1/TMRI5/ GTIOC3A/GTIOC3A#/TXD5/SMOSI5/ SSDA5/SSLA1	TRST#/PD7/MTIOC9A/MTIOC9A#/ GTIOC0A/GTIOC3A/GTIOC0A#/ GTIOC3A#/TMRI1/TMRI5/TXD5/SMOSI5/ SSDA5/SSLA1/CTX0/IRQ8
19	PD6/MTIOC9C/MTIOC9C#/TMO1/ GTIOC3B/GTIOC3B#/CTS1#/RTS1#/SS1#/ SSLA0/IRQ5/ADST0	TMS/PD6/MTIOC9C/MTIOC9C#/GTIOC0B/ GTIOC3B/GTIOC0B#/GTIOC3B#/TMO1/ CTS1#/RTS1#/SS1#/CTS11#/RTS11#/ SS11#/SSLA0/IRQ5/ADST0
20	PD5/TMRI0/TMRI6/GTECLKA/RXD1/ SMISO1/SSCL1/IRQ3	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/ TMRI0/TMRI6/RXD1/SMISO1/SSCL1/ RXD11/SMISO11/SSCL11/IRQ6
21	PD4/TMCI0/TMCI6/GTECLKB/SCK1/IRQ2	TCK/PD4/GTIOC1B/GTETRGB/ GTIOC1B#/TMCI0/TMCI6/SCK1/SCK11/IRQ2

100 Pins	RX24T (Chip Version B)	RX66T (with PGA pseudo-differential input and without USB pins)
22	PD3/TMO0/GTECLKC/TXD1/SMOSI1/ SSDA1	TDO/PD3/GTIOC2A/GTETRGC/GTIOC2A#/ TMO0/TXD1/SMOSI1/SSDA1/TXD11/ SMOSI11/SSDA11
23	PD2/TMCI1/TMO4/GTIOC0A/GTIOC0A#/ SCK5/MOSIA	TRCLK/PD2/A7/GTIOC2B/GTIOC0A/ GTIOC2B#/GTIOC0A#/TMCI1/TMO4/ SCK5/SCK8/MOSIA
24	PD1/TMO2/GTIOC0B/GTIOC0B#/MISOA	TRDATA3/PD1/A6/GTIOC3A/GTIOC0B/ GTIOC3A#/GTIOC0B#/TMO2/RXD8/ SMISO8/SSCL8/MISOA
25	PD0/TMO6/GTIOC1A/GTIOC1A#/RSPCKA	TRDATA2/PD0/A5/GTIOC3B/GTIOC1A/ GTIOC3B#/GTIOC1A#/TMO6/TXD8/ SMOSI8/SSDA8/RSPCKA
26	PB7/GTIOC1B/GTIOC1B#/SCK5	TRDATA1/PB7/A4/GTIOC1B/GTIOC1B#/ SCK5/SCK11/SCK12
27	PB6/GTIOC2A/GTIOC2A#/RXD5/SMISO5/ SSCL5/IRQ5	TRDATA0/PB6/A3/GTIOC2A/GTIOC2A#/ RXD5/SMISO5/SSCL5/RXD11/SMISO11/ SSCL11/RXD12/SMISO12/SSCL12/ RXDX12/CRX0/IRQ2
28	PB5/GTIOC2B/GTIOC2B#/TXD5/SMOSI5/ SSDA5	TRSYNC/PB5/A2/GTIOC2B/GTIOC2B#/ TXD5/SMOSI5/SSDA5/TXD11/SMOSI11/ SSDA11/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/CTX0
29	VCC	VCC
30	PB4/POE8#/GTETRG/GTECLKD/CTS5#/ RTS5#/SS5#/IRQ3	PB4/A1/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE8#/CTS5#/RTS5#/SS5#/ SCK11/CTS11#/RTS11#/SS11#/IRQ3_DS
31	VSS	VSS
32	PB3/MTIOC0A/MTIOC0A#/CACREF/SCK6/ RSPCKA	PB3/A7(Note 1)/MTIOC0A/MTIOC0A#/CACREF/ SCK6/RSPCKA/IRQ9
33	PB2/MTIOC0B/MTIOC0B#/TMRI0/ADSM0/ TXD6/SMOSI6/SSDA6/SDA0	PB2/A6(Note 1)/MTIOC0B/MTIOC0B#/GTADSM0/ TMRI0/TXD6/SMOSI6/SSDA6/SDA/ADSM0
34	PB1/MTIOC0C/MTIOC0C#/TMCI0/ADSM1/ RXD6/SMISO6/SSCL6/SCL0	PB1/A5(Note 1)/MTIOC0C/MTIOC0C#/GTADSM1/ TMCI0/RXD6/SMISO6/SSCL6/SCL/IRQ4/ ADSM1
35	PB0/MTIOC0D/MTIOC0D#/TMO0/TXD6/ SMOSI6/SSDA6/MOSIA/ADTRG2#	PB0/A0/A4(Note 1)/BC0#/MTIOC0D/MTIOC0D#/ TMO0/TXD6/SMOSI6/SSDA6/CTS11#/ RTS11#/SS11#/MOSIA/IRQ8/ADTRG2#
36	PA5/MTIOC1A/MTIOC1A#/TMCI3/RXD6/ SMISO6/SSCL6/MISOA/IRQ1/ADTRG1#	PA5/A3(Note 1)/MTIOC1A/MTIOC1A#/TMCI3/ RXD6/SMISO6/SSCL6/RXD8/SMISO8/ SSCL8/MISOA/IRQ1/ADTRG1#
37	PA4/MTIOC1B/MTIOC1B#/TMCI7/SCK6/ RSPCKA/ADTRG0#	PA4/A2(Note 1)/MTIOC1B/MTIOC1B#/TMCI7/ SCK6/TXD8/SMOSI8/SSDA8/RSPCKA/ ADTRG0#
38	PA3/MTIOC2A/MTIOC2A#/TMRI7/ GTADSM0/SSLA0	PA3/A1(Note 1)/MTIOC2A/MTIOC2A#/GTADSM0/ TMRI7/TXD9/SMOSI9/SSDA9/SCK8/SSLA0
39	PA2/MTIOC2B/MTIOC2B#/TMO7/ GTADSM1/CTS6#/RTS6#/SS6#/SSLA1	PA2/A0/BC0#/MTIOC2B/MTIOC2B#/ GTADSM1/TMO7/CTS6#/RTS6#/SS6#/ RXD9/SMISO9/SSCL9/SCK11(Note 1)/SSLA1
40	PA1/MTIOC6A/MTIOC6A#/TMO4/SSLA2/ CRXD0/ADTRG0#	PA1/MTIOC6A/MTIOC6A#/TMO4/TXD9/ SMOSI9/SSDA9/RXD11/SMISO11/SSCL11/ SSLA2/CRX0/IRQ14_DS/ADTRG0#
41	PA0/MTIOC6C/MTIOC6C#/TMO2/SSLA3/ CTXD0	PA0/MTIOC6C/MTIOC6C#/TMO2/SCK9/ TXD11/SMOSI11/SSDA11/SSLA3/CTX0
42	VCC	VCC

100 Pins	RX24T (Chip Version B)	RX66T (with PGA pseudo-differential input and without USB pins)
43	P96/POE4#/IRQ4	P96/CS0#/WAIT#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE4#/CTS8#/ RTS8#/SS8#/IRQ4_DS
44	VSS	VSS
45	P95/MTIOC6B/MTIOC6B#	P95/MTIOC6B/MTIOC6B#/GTIOC4A/ GTIOC7A/GTIOC4A#/GTIOC7A#
46	P94/MTIOC7A/MTIOC7A#	P94/MTIOC7A/MTIOC7A#/GTIOC5A/ GTIOC8A/GTIOC5A#/GTIOC8A#
47	P93/MTIOC7B/MTIOC7B#	P93/MTIOC7B/MTIOC7B#/GTIOC6A/ GTIOC9A/GTIOC6A#/GTIOC9A#
48	P92/MTIOC6D/MTIOC6D#	P92/MTIOC6D/MTIOC6D#/GTIOC4B/ GTIOC7B/GTIOC4B#/GTIOC7B#
49	P91/MTIOC7C/MTIOC7C#	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC8B/GTIOC5B#/GTIOC8B#
50	P90/MTIOC7D/MTIOC7D#	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC9B/GTIOC6B#/GTIOC9B#
51	P76/MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC2B#	P76/D0[A0/D0]/MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC6B/GTIOC2B#/GTIOC6B#
52	P75/MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC1B#	P75/D1[A1/D1]/MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#
53	P74/MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC0B#	P74/D2[A2/D2]/MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#
54	P73/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC2A#	P73/D3[A3/D3]/MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC6A/GTIOC2A#/GTIOC6A#
55	P72/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC1A#	P72/D4[A4/D4]/MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC5A/GTIOC1A#/GTIOC5A#
56	P71/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC0A#	P71/D5[A5/D5]/MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC4A/GTIOC0A#/GTIOC4A#
57	P70/POE0#/IRQ5	P70/D6[A6/D6]/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE0#/CTS9#/ RTS9#/SS9#/IRQ5_DS
58	P33/MTIOC3A/MTIOC3A#/MTCLKA/ MTCLKA#/TMO0/SSLA3	P33/D7[A7/D7]/MTIOC3A/MTCLKA/ MTIOC3A#/MTCLKA#/GTIOC3B/ GTIOC3B#/TMO0/SSLA3/IRQ13_DS
59	P32/MTIOC3C/MTIOC3C#/MTCLKB/ MTCLKB#/TMO6/SSLA2	P32/D8[A8/D8]/MTIOC3C/MTCLKB/ MTIOC3C#/MTCLKB#/GTIOC3A/ GTIOC3A#/TMO6/SSLA2/IRQ12_DS
60	VCC	VCC
61	P31/MTIOC0A/MTIOC0A#/MTCLKC/ MTCLKC#/TMRI6/SSLA1/IRQ6	P31/D9[A9/D9]/MTIOC0A/MTCLKC/ MTIOC0A#/MTCLKC#/TMRI6/SSLA1/IRQ6
62	VSS	VSS
63	P30/MTIOC0B/MTIOC0B#/MTCLKD/ MTCLKD#/TMCI6/SSLA0/IRQ7/COMP3	P30/D10[A10/D10]/MTIOC0B/MTCLKD/ MTIOC0B#/MTCLKD#/TMCI6/SCK8/ CTS8#/RTS8#/SS8#/SSLA0/IRQ7/COMP3
64	P24/MTIC5U/MTIC5U#/TMCI2/TMO6/ RSPCKA/COMP0/DA0	P27/CS3#(Note 1)/MTIOC1A/MTIOC0C/ MTIOC1A#/MTIOC0C#/POE9#/IRQ15
65	P23/MTIC5V/MTIC5V#/TMO2/CACREF/ MOSIA/COMP1/DA1	P24/D11[A11/D11]/MTIC5U/MTIC5U#/ TMCI2/TMO6/CTS8#/RTS8#/SS8#/SCK8/ RSPCKA/IRQ4/COMP0
66	P22/MTIC5W/MTIC5W#/TMRI2/TMO4/ MISOA/ADTRG2#/COMP2	P23/D12[A12/D12]/MTIC5V/MTIC5V#/ TMO2/CACREF/TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/SSDA12/TXDX12/ SIOX12/MOSIA/CTX0/IRQ11/COMP1

100 Pins	RX24T (Chip Version B)	RX66T (with PGA pseudo-differential input and without USB pins)
67	P21/MTCLKA/MTCLKA#/MTIOC9A/ MTIOC9A#/TMCI4/IRQ6/ADTRG1#/AN116	P22/D13[A13/D13]/MTIC5W/MTCLKD/ MTIC5W#/MTCLKD#/MTIOC9B/TMRI2/ TMO4/RXD8/SMISO8/SSCL8/RXD12/ SMISO12/SSCL12/RXDX12/MISOA/CRX0/ IRQ10/ADTRG2#/COMP2
68	P20/MTCLKB/MTCLKB#/MTIOC9C/ MTIOC9C#/TMRI4/IRQ7/ADTRG0#/AN016	P21/D14[A14/D14]/MTIOC9A/MTCLKA/ MTIOC9A#/MTCLKA#/TMCI4/TXD8/ SMOSI8/SSDA8/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/MOSIA/ IRQ6_DS/AN217/ADTRG1#/COMP5
69	P65/AN205	P20/D15[A15/D15]/MTIOC9C/MTCLKB/ MTIOC9C#/MTCLKB#/TMRI4/CTS8#/ RTS8#/SS8#/SCK8/RSPCKA/IRQ7_DS/ AN216/ADTRG0#/COMP4
70	P64/AN204	P65/A12/IRQ9/AN211/CMPC53/DA1
71	AVCC2	P64/A13/IRQ8/AN210/CMPC33/DA0
72	VREF	AVCC2
73	AVSS2	AVSS2
74	P63/AN203/IRQ7	P63/A12(Note 1)/A14/IRQ7/AN209/CMPC23
75	P62/AN202/IRQ6	P62/A13(Note 1)/A15/IRQ6/AN208/CMPC43
76	P61/AN201/IRQ5	P61/A14(Note 1)/A16/IRQ5/AN207/CMPC13
77	P60/AN200/IRQ4	P60/A15(Note 1)/A17/IRQ4/AN206/CMPC03
78	P55/AN211/IRQ3	P55/A16(Note 1)/A18/IRQ3/AN203/CMPC32
79	P54/AN210/IRQ2	P54/A17(Note 1)/A19/IRQ2/AN202/CMPC22
80	P53/AN209/IRQ1	P53/A18(Note 1)/A20/IRQ1/AN201/CMPC12
81	P52/AN208/IRQ0	P52/IRQ0/AN200/CMPC02
82	P51/AN207	P47/AN103
83	P50/AN206	P46/AN102/CMPC50/CMPC51
84	P47/AN103	P45/AN101/CMPC40/CMPC41
85	P46/AN102/CMPC12/CMPC13/CMPC30/ CMPC31	P44/AN100/CMPC30/CMPC31
86	P45/AN101/CMPC02/CMPC03/CMPC20/ CMPC21	PH4/AN107/PGAVSS1
87	P44/AN100/CMPC10/CMPC11/CMPC32/ CMPC33	P43/AN003
88	P43/AN003	P42/AN002/CMPC20/CMPC21
89	P42/AN002	P41/AN001/CMPC10/CMPC11
90	P41/AN001	P40/AN000/CMPC00/CMPC01
91	P40/AN000/CMPC00/CMPC01/CMPC22/ CMPC23	PH0/AN007/PGAVSS0
92	AVCC1	AVCC1
93	AVCC0	AVCC0
94	AVSS0	AVSS0
95	AVSS1	AVSS1
96	P82/MTIC5U/MTIC5U#/TMO4/SCK6	P82/ALE/WAIT#/MTIC5U/MTIC5U#/ TMO4/SCK6/SCK12/IRQ3/COMP5
97	P81/MTIC5V/MTIC5V#/TMCI4/TXD6/ SMOSI6/SSDA6	P81/CS2#/MTIC5V/MTIC5V#/TMCI4/ TXD6/SMOSI6/SSDA6/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/COMP4
98	P80/MTIC5W/MTIC5W#/TMRI4/RXD6/ SMISO6/SSCL6	P80/CS1#/MTIC5W/MTIC5W#/TMRI4/ RXD6/SMISO6/SSCL6/RXD12/SMISO12/ SSCL12/RXDX12/IRQ5/COMP3

100 Pins	RX24T (Chip Version B)	RX66T (with PGA pseudo-differential input and without USB pins)
99	P11/MTIOC3A/MTIOC3A#/MTCLKC/ MTCLKC#/TMO3/IRQ1	P11/RD#/MTIOC3A/MTCLKC/ MTIOC3A#/MTCLKC#/MTIOC9D/ GTIOC3B/GTETRGA/GTIOC3B#/ GTETRGC/TMO3/POE9#/IRQ1_DS
100	P10/MTIOC9B/MTIOC9B#/MTCLKD/ MTCLKD#/TMRI3/POE12#/CTS6#/RTS6#/ SS6#/IRQ0	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/GTETRGB/GTETRGD/TMRI3/ POE12#/CTS6#/RTS6#/SS6#/IRQ0_DS

Note 1. These pins are only enabled for products with 128 Kbytes of RAM.

3.3 100-Pin Package (RX24T: Chip Version B, RX66T: Without Both PGA Pseudo-Differential Input and USB Pins)

Table 3.3 lists Comparison of Pin Functions for 100-Pin Package (RX24T: Chip Version B, RX66T: Without Both PGA Pseudo-Differential Input and USB Pins).

Table 3.3 Comparison of Pin Functions for 100-Pin Package (RX24T: Chip Version B, RX66T: Without Both PGA Pseudo-Differential Input and USB Pins)

100 Pins	RX24T (Chip Version B)	RX66T (without both PGA pseudo-differential input and USB)
1	PE5/IRQ0	PE5/BCLK/MTIOC9D/MTIOC9D#/GTIOC3A/GTETRGB/GTIOC3A#/GTETRGD/SCK9/CTS9#/RTS9#/SS9#/IRQ0/ADST0
2	P02/MTIOC9D/MTIOC9D#/CTS1#/RTS1#/SS1#/IRQ5/ADST0	EMLE
3	VSS	VSS
4	P00/IRQ2/ADST1	UB/P00/A11/MTIOC9A/MTIOC9A#/CACREF/RXD9/SMISO9/SSCL9/RXD12/SMISO12/SSCL12/RXDX12/IRQ2/ADST1/COMP0
5	VCL	VCL
6	MD/FINED	MD/FINED
7	P01/POE12#/IRQ4/ADST2	P01/A10/MTIOC9C/MTIOC9C#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE12#/TXD9/SMOSI9/SSDA9/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/IRQ4/ADST2/COMP1
8	PE4/MTCLKC/MTCLKC#/POE10#/IRQ1	PE4/A9/MTCLKC/MTCLKC#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE10#/SCK9/IRQ1
9	PE3/MTCLKD/MTCLKD#/POE11#/IRQ2	PE3/A8/MTCLKD/MTCLKD#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE11#/CTS9#/RTS9#/SS9#/IRQ2_DS
10	RES#	RES#
11	XTAL/P37	XTAL/P37
12	VSS	VSS
13	EXTAL/P36	EXTAL/P36
14	VCC	VCC
15	PE2/POE10#/NMI	PE2/POE10#/NMI
16	PE1/MTIOC9D/MTIOC9D#/TMO5/CTS5#/RTS5#/SS5#/SSLA3	PE1/WR0#/WR#/MTIOC9D/MTIOC9D#/TMO5/CTS5#/RTS5#/SS5#/CTS12#/RTS12#/SS12#/SSLA3/IRQ15
17	PE0/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/SSCL5/SSLA2	PE0/WR1#/BC1#/WAIT#/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/SSCL5/SSLA2/CRX0/IRQ7
18	PD7/MTIOC9A/MTIOC9A#/TMRI1/TMRI5/GTIOC3A/GTIOC3A#/TXD5/SMOSI5/SSDA5/SSLA1	TRST#/PD7/MTIOC9A/MTIOC9A#/GTIOC0A/GTIOC3A/GTIOC0A#/GTIOC3A#/TMRI1/TMRI5/TXD5/SMOSI5/SSDA5/SSLA1/CTX0/IRQ8
19	PD6/MTIOC9C/MTIOC9C#/TMO1/GTIOC3B/GTIOC3B#/CTS1#/RTS1#/SS1#/SSLA0/IRQ5/ADST0	TMS/PD6/MTIOC9C/MTIOC9C#/GTIOC0B/GTIOC3B/GTIOC0B#/GTIOC3B#/TMO1/CTS1#/RTS1#/SS1#/CTS11#/RTS11#/SS11#/SSLA0/IRQ5/ADST0
20	PD5/TMRI0/TMRI6/GTECLKA/RXD1/SMISO1/SSCL1/IRQ3	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/TMRI0/TMRI6/RXD1/SMISO1/SSCL1/RXD11/SMISO11/SSCL11/IRQ6

100 Pins	RX24T (Chip Version B)	RX66T (without both PGA pseudo-differential input and USB)
21	PD4/TMCI0/TMCI6/GTECLKB/SCK1/IRQ2	TCK/PD4/GTIOC1B/GTETRGB/ GTIOC1B#/TMCI0/TMCI6/SCK1/SCK11/IRQ2
22	PD3/TMO0/GTECLKC/TXD1/SMOSI1/ SSDA1	TDO/PD3/GTIOC2A/GTETRGC/GTIOC2A#/ TMO0/TXD1/SMOSI1/SSDA1/TXD11/ SMOSI11/SSDA11
23	PD2/TMCI1/TMO4/GTIOC0A/GTIOC0A#/ SCK5/MOSIA	TRCLK/PD2/A7/GTIOC2B/GTIOC0A/ GTIOC2B#/GTIOC0A#/TMCI1/TMO4/ SCK5/SCK8/MOSIA
24	PD1/TMO2/GTIOC0B/GTIOC0B#/MISOA	TRDATA3/PD1/A6/GTIOC3A/GTIOC0B/ GTIOC3A#/GTIOC0B#/TMO2/RXD8/ SMISO8/SSCL8/MISOA
25	PD0/TMO6/GTIOC1A/GTIOC1A#/RSPCKA	TRDATA2/PD0/A5/GTIOC3B/GTIOC1A/ GTIOC3B#/GTIOC1A#/TMO6/TXD8/ SMOSI8/SSDA8/RSPCKA
26	PB7/GTIOC1B/GTIOC1B#/SCK5	TRDATA1/PB7/A4/GTIOC1B/GTIOC1B#/ SCK5/SCK11/SCK12
27	PB6/GTIOC2A/GTIOC2A#/RXD5/SMISO5/ SSCL5/IRQ5	TRDATA0/PB6/A3/GTIOC2A/GTIOC2A#/ RXD5/SMISO5/SSCL5/RXD11/SMISO11/ SSCL11/RXD12/SMISO12/SSCL12/ RXDX12/CRX0/IRQ2
28	PB5/GTIOC2B/GTIOC2B#/TXD5/SMOSI5/ SSDA5	TRSYNC/PB5/A2/GTIOC2B/GTIOC2B#/ TXD5/SMOSI5/SSDA5/TXD11/SMOSI11/ SSDA11/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/CTX0
29	VCC	VCC
30	PB4/POE8#/GTETRG/GTECLKD/CTS5#/ RTS5#/SS5#/IRQ3	PB4/A1/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE8#/CTS5#/RTS5#/SS5#/ SCK11/CTS11#/RTS11#/SS11#/IRQ3_DS
31	VSS	VSS
32	PB3/MTIOC0A/MTIOC0A#/CACREF/SCK6/ RSPCKA	PB3/A7(Note 1)/MTIOC0A/MTIOC0A#/ CACREF/SCK6/RSPCKA/IRQ9
33	PB2/MTIOC0B/MTIOC0B#/TMRI0/ADSM0/ TXD6/SMOSI6/SSDA6/SDA0	PB2/A6(Note 1)/MTIOC0B/MTIOC0B#/ GTADSM0/TMRI0/TXD6/SMOSI6/SSDA6/ SDA/ADSM0
34	PB1/MTIOC0C/MTIOC0C#/TMCI0/ADSM1/ RXD6/SMISO6/SSCL6/SCL0	PB1/A5(Note 1)/MTIOC0C/MTIOC0C#/ GTADSM1/TMCI0/RXD6/SMISO6/SSCL6/ SCL/IRQ4/ADSM1
35	PB0/MTIOC0D/MTIOC0D#/TMO0/TXD6/ SMOSI6/SSDA6/MOSIA/ADTRG2#	PB0/A0/A4(Note 1)/BC0#/MTIOC0D/MTIOC0D#/ TMO0/TXD6/SMOSI6/SSDA6/CTS11#/ RTS11#/SS11#/MOSIA/IRQ8/ADTRG2#
36	PA5/MTIOC1A/MTIOC1A#/TMCI3/RXD6/ SMISO6/SSCL6/MISOA/IRQ1/ADTRG1#	PA5/A3(Note 1)/MTIOC1A/MTIOC1A#/TMCI3/ RXD6/SMISO6/SSCL6/RXD8/SMISO8/ SSCL8/MISOA/IRQ1/ADTRG1#
37	PA4/MTIOC1B/MTIOC1B#/TMCI7/SCK6/ RSPCKA/ADTRG0#	PA4/A2(Note 1)/MTIOC1B/MTIOC1B#/TMCI7/ SCK6/TXD8/SMOSI8/SSDA8/RSPCKA/ ADTRG0#
38	PA3/MTIOC2A/MTIOC2A#/TMRI7/ GTADSM0/SSLA0	PA3/A1(Note 1)/MTIOC2A/MTIOC2A#/ GTADSM0/TMRI7/TXD9/SMOSI9/SSDA9/ SCK8/SSLA0
39	PA2/MTIOC2B/MTIOC2B#/TMO7/ GTADSM1/CTS6#/RTS6#/SS6#/SSLA1	PA2/A0/BC0#/MTIOC2B/MTIOC2B#/ GTADSM1/TMO7/CTS6#/RTS6#/SS6#/ RXD9/SMISO9/SSCL9/SCK11(Note 1)/SSLA1

100 Pins	RX24T (Chip Version B)	RX66T (without both PGA pseudo-differential input and USB)
40	PA1/MTIOC6A/MTIOC6A#/TMO4/SSLA2/ CRXD0/ADTRG0#	PA1/MTIOC6A/MTIOC6A#/TMO4/TXD9/ SMOSI9/SSDA9/RXD11/SMISO11/SSCL11/ SSLA2/CRX0/IRQ14_DS/ADTRG0#
41	PA0/MTIOC6C/MTIOC6C#/TMO2/SSLA3/ CTXD0	PA0/MTIOC6C/MTIOC6C#/TMO2/SCK9/ TXD11/SMOSI11/SSDA11/SSLA3/CTX0
42	VCC	VCC
43	P96/POE4#/IRQ4	P96/CS0#/WAIT#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/ POE4#/CTS8#/RTS8#/SS8#/IRQ4_DS
44	VSS	VSS
45	P95/MTIOC6B/MTIOC6B#	P95/MTIOC6B/MTIOC6B#/GTIOC4A/ GTIOC7A/GTIOC4A#/GTIOC7A#
46	P94/MTIOC7A/MTIOC7A#	P94/MTIOC7A/MTIOC7A#/GTIOC5A/ GTIOC8A/GTIOC5A#/GTIOC8A#
47	P93/MTIOC7B/MTIOC7B#	P93/MTIOC7B/MTIOC7B#/GTIOC6A/ GTIOC9A/GTIOC6A#/GTIOC9A#
48	P92/MTIOC6D/MTIOC6D#	P92/MTIOC6D/MTIOC6D#/GTIOC4B/ GTIOC7B/GTIOC4B#/GTIOC7B#
49	P91/MTIOC7C/MTIOC7C#	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC8B/GTIOC5B#/GTIOC8B#
50	P90/MTIOC7D/MTIOC7D#	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC9B/GTIOC6B#/GTIOC9B#
51	P76/MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC2B#	P76/D0[A0/D0]/MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC6B/GTIOC2B#/GTIOC6B#
52	P75/MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC1B#	P75/D1[A1/D1]/MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#
53	P74/MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC0B#	P74/D2[A2/D2]/MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#
54	P73/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC2A#	P73/D3[A3/D3]/MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC6A/GTIOC2A#/GTIOC6A#
55	P72/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC1A#	P72/D4[A4/D4]/MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC5A/GTIOC1A#/GTIOC5A#
56	P71/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC0A#	P71/D5[A5/D5]/MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC4A/GTIOC0A#/GTIOC4A#
57	P70/POE0#/IRQ5	P70/D6[A6/D6]/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE0#/CTS9#/ RTS9#/SS9#/IRQ5_DS
58	P33/MTIOC3A/MTIOC3A#/MTCLKA/ MTCLKA#/TMO0/SSLA3	P33/D7[A7/D7]/MTIOC3A/MTCLKA/ MTIOC3A#/MTCLKA#/GTIOC3B/ GTIOC3B#/TMO0/SSLA3/IRQ13_DS
59	P32/MTIOC3C/MTIOC3C#/MTCLKB/ MTCLKB#/TMO6/SSLA2	P32/D8[A8/D8]/MTIOC3C/MTCLKB/ MTIOC3C#/MTCLKB#/GTIOC3A/ GTIOC3A#/TMO6/SSLA2/IRQ12_DS
60	VCC	VCC
61	P31/MTIOC0A/MTIOC0A#/MTCLKC/ MTCLKC#/TMRI6/SSLA1/IRQ6	P31/D9[A9/D9]/MTIOC0A/MTCLKC/ MTIOC0A#/MTCLKC#/TMRI6/SSLA1/IRQ6
62	VSS	VSS
63	P30/MTIOC0B/MTIOC0B#/MTCLKD/ MTCLKD#/TMCI6/SSLA0/IRQ7/COMP3	P30/D10[A10/D10]/MTIOC0B/MTCLKD/ MTIOC0B#/MTCLKD#/TMCI6/SCK8/ CTS8#/RTS8#/SS8#/SSLA0/IRQ7/COMP3
64	P24/MTIC5U/MTIC5U#/TMCI2/TMO6/ RSPCKA/COMP0/DA0	P24/D11[A11/D11]/MTIC5U/MTIC5U#/ TMCI2/TMO6/CTS8#/RTS8#/SS8#/SCK8/ RSPCKA/IRQ4/COMP0

100 Pins	RX24T (Chip Version B)	RX66T (without both PGA pseudo-differential input and USB)
65	P23/MTIC5V/MTIC5V#/TMO2/CACREF/ MOSIA/COMP1/DA1	P23/D12[A12/D12]/MTIC5V/MTIC5V#/ TMO2/CACREF/TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/SSDA12/TXDX12/ SIOX12/MOSIA/CTX0/IRQ11/COMP1
66	P22/MTIC5W/MTIC5W#/TMRI2/TMO4/ MISOA/ADTRG2#/COMP2	P22/D13[A13/D13]/MTIC5W/MTCLKD/ MTIC5W#/MTCLKD#/MTIOC9B/TMRI2/ TMO4/RXD8/SMISO8/SSCL8/RXD12/ SMISO12/SSCL12/RXDX12/MISOA/CRX0/ IRQ10/ADTRG2#/COMP2
67	P21/MTCLKA/MTCLKA#/MTIOC9A/ MTIOC9A#/TMCI4/IRQ6/ADTRG1#/AN116	P21/D14[A14/D14]/MTIOC9A/MTCLKA/ MTIOC9A#/MTCLKA#/TMCI4/TXD8/ SMOSI8/SSDA8/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/MOSIA/ IRQ6_DS/AN217/ADTRG1#/COMP5
68	P20/MTCLKB/MTCLKB#/MTIOC9C/ MTIOC9C#/TMRI4/IRQ7/ADTRG0#/AN016	P20/D15[A15/D15]/MTIOC9C/MTCLKB/ MTIOC9C#/MTCLKB#/TMRI4/CTS8#/ RTS8#/SS8#/SCK8/RSPCKA/IRQ7_DS/ AN216/ADTRG0#/COMP4
69	P65/AN205	P65/A12/IRQ9/AN211/CMPC53/DA1
70	P64/AN204	P64/A13/IRQ8/AN210/CMPC33/DA0
71	AVCC2	AVCC2
72	VREF	AVCC2
73	AVSS2	AVSS2
74	P63/AN203/IRQ7	P63/A12(Note 1)/A14/IRQ7/AN209/CMPC23
75	P62/AN202/IRQ6	P62/A13(Note 1)/A15/IRQ6/AN208/CMPC43
76	P61/AN201/IRQ5	P61/A14(Note 1)/A16/IRQ5/AN207/CMPC13
77	P60/AN200/IRQ4	P60/A15(Note 1)/A17/IRQ4/AN206/CMPC03
78	P55/AN211/IRQ3	P55/A16(Note 1)/A18/IRQ3/AN203/CMPC32
79	P54/AN210/IRQ2	P54/A17(Note 1)/A19/IRQ2/AN202/CMPC22
80	P53/AN209/IRQ1	P53/A18(Note 1)/A20/IRQ1/AN201/CMPC12
81	P52/AN208/IRQ0	P52/IRQ0/AN200/CMPC02
82	P51/AN207	P51/AN205/CMPC52
83	P50/AN206	P50/AN204/CMPC42
84	P47/AN103	P47/AN103
85	P46/AN102/CMPC12/CMPC13/CMPC30/ CMPC31	P46/AN102/CMPC50/CMPC51
86	P45/AN101/CMPC02/CMPC03/CMPC20/ CMPC21	P45/AN101/CMPC40/CMPC41
87	P44/AN100/CMPC10/CMPC11/CMPC32/ CMPC33	P44/AN100/CMPC30/CMPC31
88	P43/AN003	P43/AN003
89	P42/AN002	P42/AN002/CMPC20/CMPC21
90	P41/AN001	P41/AN001/CMPC10/CMPC11
91	P40/AN000/CMPC00/CMPC01/CMPC22/ CMPC23	P40/AN000/CMPC00/CMPC01
92	AVCC1	AVCC1
93	AVCC0	AVCC0
94	AVSS0	AVSS0
95	AVSS1	AVSS1
96	P82/MTIC5U/MTIC5U#/TMO4/SCK6	P82/ALE/WAIT#/MTIC5U/MTIC5U#/ TMO4/SCK6/SCK12/IRQ3/COMP5

100 Pins	RX24T (Chip Version B)	RX66T (without both PGA pseudo-differential input and USB)
97	P81/MTIC5V/MTIC5V#/TMCI4/TXD6/ SMOSI6/SSDA6	P81/CS2#/MTIC5V/MTIC5V#/TMCI4/ TXD6/SMOSI6/SSDA6/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/COMP4
98	P80/MTIC5W/MTIC5W#/TMRI4/RXD6/ SMISO6/SSCL6	P80/CS1#/MTIC5W/MTIC5W#/TMRI4/ RXD6/SMISO6/SSCL6/RXD12/SMISO12/ SSCL12/RXDX12/IRQ5/COMP3
99	P11/MTIOC3A/MTIOC3A#/MTCLKC/ MTCLKC#/TMO3/IRQ1	P11/RD#/MTIOC3A/MTCLKC/ MTIOC3A#/MTCLKC#/MTIOC9D/ GTIOC3B/GTETRGA/GTIOC3B#/ GTETRGC/TMO3/POE9#/IRQ1_DS
100	P10/MTIOC9B/MTIOC9B#/MTCLKD/ MTCLKD#/TMRI3/POE12#/CTS6#/RTS6#/ SS6#/IRQ0	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/GTETRGB/GTETRGD/TMRI3/ POE12#/CTS6#/RTS6#/SS6#/IRQ0_DS

Note 1. These pins are only enabled for products with 128 Kbytes of RAM.

3.4 100-Pin Package (RX24T: Chip Version A, RX66T: With PGA Pseudo-Differential Input and USB Pins)

Table 3.4 lists Comparison of Pin Functions for 100-Pin Packages (RX24T: Chip Version A, RX66T: With PGA Pseudo-Differential Input and USB Pins).

Table 3.4 Comparison of Pin Functions for 100-Pin Packages (RX24T: Chip Version A, RX66T: With PGA Pseudo-Differential Input and USB Pins)

100 Pins	RX24T (Chip Version A)	RX66T (with PGA pseudo-differential input and USB pins)
1	PE5/IRQ0	PE5/BCLK/MTIOC9D/MTIOC9D#/GTIOC3A/GTETRGB/GTIOC3A#/GTETRGD/SCK9/CTS9#/RTS9#/SS9#/IRQ0/ADST0
2	P02/MTIOC9D/CTS1#/RTS1#/SS1#/IRQ5/ADST0	EMLE
3	VSS	VSS
4	P00/IRQ2/ADST1	UB/P00/A11/MTIOC9A/MTIOC9A#/CACREF/RXD9/SMISO9/SSCL9/RXD12/SMISO12/SSCL12/RXDX12/IRQ2/ADST1/COMP0
5	VCL	VCL
6	MD/FINED	MD/FINED
7	P01/POE12#/IRQ4/ADST2	P01/A10/MTIOC9C/MTIOC9C#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE12#/TXD9/SMOSI9/SSDA9/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/IRQ4/ADST2/COMP1
8	PE4/MTCLKC/POE10#/IRQ1	PE4/A9/MTCLKC/MTCLKC#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE10#/SCK9/IRQ1
9	PE3/MTCLKD/POE11#/IRQ2	PE3/A8/MTCLKD/MTCLKD#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE11#/CTS9#/RTS9#/SS9#/IRQ2_DS
10	RES#	RES#
11	XTAL/P37	XTAL/P37
12	VSS	VSS
13	EXTAL/P36	EXTAL/P36
14	VCC	VCC
15	PE2/POE10#/NMI	UPSEL/PE2/POE10#/NMI
16	PE1/MTIOC9D/TMO5/CTS5#/RTS5#/SS5#/SSLA3	PE1/WR0#/WR#/MTIOC9D/MTIOC9D#/TMO5/CTS5#/RTS5#/SS5#/CTS12#/RTS12#/SS12#/SSLA3/IRQ15
17	PE0/MTIOC9B/TMCI1/TMCI5/SSLA2	PE0/WR1#/BC1#/WAIT#/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/SSCL5/SSLA2/CRX0/USB0_OVRCURB/IRQ7
18	PD7/MTIOC9A/TMRI1/TMRI5/SSLA1	TRST#/PD7/MTIOC9A/MTIOC9A#/GTIOC0A/GTIOC3A/GTIOC0A#/GTIOC3A#/TMRI1/TMRI5/TXD5/SMOSI5/SSDA5/SSLA1/CTX0/IRQ8
19	PD6/MTIOC9C/TMO1/CTS1#/RTS1#/SS1#/SSLA0/IRQ5/ADST0	TMS/PD6/MTIOC9C/MTIOC9C#/GTIOC0B/GTIOC3B/GTIOC0B#/GTIOC3B#/TMO1/CTS1#/RTS1#/SS1#/CTS11#/RTS11#/SS11#/SSLA0/IRQ5/ADST0
20	PD5/TMRI0/TMRI6/RXD1/SMISO1/SSCL1/IRQ3	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/TMRI0/TMRI6/RXD1/SMISO1/SSCL1/RXD11/SMISO11/SSCL11/IRQ6
21	PD4/TMCI0/TMCI6/SCK1/IRQ2	TCK/PD4/GTIOC1B/GTETRGB/GTIOC1B#/TMCI0/TMCI6/SCK1/SCK11/IRQ2

100 Pins	RX24T (Chip Version A)	RX66T (with PGA pseudo-differential input and USB pins)
22	PD3/TMO0/TXD1/SMOSI1/SSDA1	TDO/PD3/GTIOC2A/GTETRGC/GTIOC2A#/ TMO0/TXD1/SMOSI1/SSDA1/TXD11/ SMOSI11/SSDA11
23	PD2/TMCI1/TMO4/SCK5/MOSIA	TRCLK/PD2/A7/GTIOC2B/GTIOC0A/ GTIOC2B#/GTIOC0A#/TMCI1/TMO4/ SCK5/SCK8/MOSIA/USB0_VBUS
24	PD1/TMO2/MISOA	USB0_DM
25	PD0/TMO6/RSPCKA	USB0_DP
26	PB7/SCK5	VCC_USB
27	PB6/RXD5/SMISO5/SSCL5/IRQ5	TRDATA0/PB6/A3/GTIOC2A/GTIOC2A#/ RXD5/SMISO5/SSCL5/RXD11/SMISO11/ SSCL11/RXD12/SMISO12/SSCL12/ RXDX12/CRX0/USB0_OVRCURA/IRQ2
28	PB5/TXD5/SMOSI5/SSDA5	TRSYNC/PB5/A2/GTIOC2B/GTIOC2B#/ TXD5/SMOSI5/SSDA5/TXD11/SMOSI11/ SSDA11/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/CTX0/USB0_VBUSEN
29	VCC	VCC
30	PB4/POE8#/CTS5#/RTS5#/SS5#/IRQ3	PB4/A1/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE8#/CTS5#/RTS5#/SS5#/ SCK11/CTS11#/RTS11#/SS11#/ USB0_OVRCURB/IRQ3_DS
31	VSS	VSS/VSS_USB
32	PB3/MTIOC0A/CACREF/SCK6/RSPCKA	PB3/A7/MTIOC0A/MTIOC0A#/CACREF/ SCK6/RSPCKA/IRQ9
33	PB2/MTIOC0B/TMRI0/ADSM0/TXD6/ SMOSI6/SSDA6/SDA0	PB2/A6/MTIOC0B/MTIOC0B#/GTADSM0/ TMRI0/TXD6/SMOSI6/SSDA6/SDA/ADSM0
34	PB1/MTIOC0C/TMCI0/ADSM1/RXD6/ SMISO6/SSCL6/SCL0	PB1/A5/MTIOC0C/MTIOC0C#/GTADSM1/ TMCI0/RXD6/SMISO6/SSCL6/SCL/IRQ4/ ADSM1
35	PB0/MTIOC0D/TMO0/TXD6/SMOSI6/ SSDA6/MOSIA/ADTRG2#	PB0/A0/A4/BC0#/MTIOC0D/MTIOC0D#/ TMO0/TXD6/SMOSI6/SSDA6/CTS11#/ RTS11#/SS11#/MOSIA/IRQ8/ADTRG2#
36	PA5/MTIOC1A/TMCI3/RXD6/SMISO6/ SSCL6/MISOA/IRQ1/ADTRG1#	PA5/A3/MTIOC1A/MTIOC1A#/TMCI3/ RXD6/SMISO6/SSCL6/RXD8/SMISO8/ SSCL8/MISOA/IRQ1/ADTRG1#
37	PA4/MTIOC1B/TMCI7/SCK6/RSPCKA/ ADTRG0#	PA4/A2/MTIOC1B/MTIOC1B#/TMCI7/ SCK6/TXD8/SMOSI8/SSDA8/RSPCKA/ ADTRG0#
38	PA3/MTIOC2A/TMRI7/SSLA0	PA3/A1/MTIOC2A/MTIOC2A#/GTADSM0/ TMRI7/TXD9/SMOSI9/SSDA9/SCK8/SSLA0
39	PA2/MTIOC2B/TMO7/CTS6#/RTS6#/SS6#/ SSLA1	PA2/A0/BC0#/MTIOC2B/MTIOC2B#/ GTADSM1/TMO7/CTS6#/RTS6#/SS6#/ RXD9/SMISO9/SSCL9/SCK11/SSLA1
40	PA1/MTIOC6A/TMO4/SSLA2/ADTRG0#	PA1/MTIOC6A/MTIOC6A#/TMO4/TXD9/ SMOSI9/SSDA9/RXD11/SMISO11/SSCL11/ SSLA2/CRX0/USB0_ID/USB0_OVRCURA/ IRQ14_DS/ADTRG0#
41	PA0/MTIOC6C/TMO2/SSLA3	PA0/MTIOC6C/MTIOC6C#/TMO2/SCK9/ TXD11/SMOSI11/SSDA11/SSLA3/CTX0/ USB0_EXICEN/USB0_VBUSEN
42	VCC	VCC
43	P96/POE4#/IRQ4	P96/CS0#/WAIT#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE4#/CTS8#/ RTS8#/SS8#/IRQ4_DS

100 Pins	RX24T (Chip Version A)	RX66T (with PGA pseudo-differential input and USB pins)
44	VSS	VSS
45	P95/MTIOC6B	P95/MTIOC6B/MTIOC6B#/GTIOC4A/ GTIOC7A/GTIOC4A#/GTIOC7A#
46	P94/MTIOC7A	P94/MTIOC7A/MTIOC7A#/GTIOC5A/ GTIOC8A/GTIOC5A#/GTIOC8A#
47	P93/MTIOC7B	P93/MTIOC7B/MTIOC7B#/GTIOC6A/ GTIOC9A/GTIOC6A#/GTIOC9A#
48	P92/MTIOC6D	P92/MTIOC6D/MTIOC6D#/GTIOC4B/ GTIOC7B/GTIOC4B#/GTIOC7B#
49	P91/MTIOC7C	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC8B/GTIOC5B#/GTIOC8B#
50	P90/MTIOC7D	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC9B/GTIOC6B#/GTIOC9B#
51	P76/MTIOC4D	P76/D0[A0/D0]/MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC6B/GTIOC2B#/GTIOC6B#
52	P75/MTIOC4C	P75/D1[A1/D1]/MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#
53	P74/MTIOC3D	P74/D2[A2/D2]/MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#
54	P73/MTIOC4B	P73/D3[A3/D3]/MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC6A/GTIOC2A#/GTIOC6A#
55	P72/MTIOC4A	P72/D4[A4/D4]/MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC5A/GTIOC1A#/GTIOC5A#
56	P71/MTIOC3B	P71/D5[A5/D5]/MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC4A/GTIOC0A#/GTIOC4A#
57	P70/POE0#/IRQ5	P70/D6[A6/D6]/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE0#/CTS9#/ RTS9#/SS9#/IRQ5_DS
58	P33/MTIOC3A/MTCLKA/TMO0/SSLA3	P33/D7[A7/D7]/MTIOC3A/MTCLKA/ MTIOC3A#/MTCLKA#/GTIOC3B/ GTIOC3B#/TMO0/SSLA3/IRQ13_DS
59	P32/MTIOC3C/MTCLKB/TMO6/SSLA2	P32/D8[A8/D8]/MTIOC3C/MTCLKB/ MTIOC3C#/MTCLKB#/GTIOC3A/ GTIOC3A#/TMO6/SSLA2/IRQ12_DS
60	VCC	VCC
61	P31/MTIOC0A/MTCLKC/TMRI6/SSLA1/ IRQ6	P31/D9[A9/D9]/MTIOC0A/MTCLKC/ MTIOC0A#/MTCLKC#/TMRI6/SSLA1/IRQ6
62	VSS	VSS
63	P30/MTIOC0B/MTCLKD/TMCI6/SSLA0/ IRQ7/COMP3	P30/D10[A10/D10]/MTIOC0B/MTCLKD/ MTIOC0B#/MTCLKD#/TMCI6/SCK8/ CTS8#/RTS8#/SS8#/SSLA0/IRQ7/COMP3
64	P24/MTIC5U/TMCI2/TMO6/RSPCKA/ COMP0	P27/CS3#/MTIOC1A/MTIOC0C/ MTIOC1A#/MTIOC0C#/POE9#/IRQ15
65	P23/MTIC5V/TMO2/CACREF/MOSIA/ COMP1	P24/D11[A11/D11]/MTIC5U/MTIC5U#/ TMCI2/TMO6/CTS8#/RTS8#/SS8#/SCK8/ RSPCKA/IRQ4/COMP0
66	P22/MTIC5W/TMRI2/TMO4/MISOA/ ADTRG2#/COMP2	P23/D12[A12/D12]/MTIC5V/MTIC5V#/ TMO2/CACREF/TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/SSDA12/TXDX12/ SIOX12/MOSIA/CTX0/IRQ11/COMP1
67	P21/MTCLKA/MTIOC9A/TMCI4/IRQ6/ ADTRG1#/AN116/CVREFC1	P22/D13[A13/D13]/MTIC5W/MTCLKD/ MTIC5W#/MTCLKD#/MTIOC9B/TMRI2/ TMO4/RXD8/SMISO8/SSCL8/RXD12/ SMISO12/SSCL12/RXDX12/MISOA/CRX0/ IRQ10/ADTRG2#/COMP2

100 Pins	RX24T (Chip Version A)	RX66T (with PGA pseudo-differential input and USB pins)
68	P20/MTCLKB/MTIOC9C/TMRI4/IRQ7/ ADTRG0#/AN016/CVREFC0	P21/D14[A14/D14]/MTIOC9A/MTCLKA/ MTIOC9A#/MTCLKA#/TMCI4/TXD8/ SMOSI8/SSDA8/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/MOSIA/ IRQ6_DS/AN217/ADTRG1#/COMP5
69	P65/AN205	P20/D15[A15/D15]/MTIOC9C/MTCLKB/ MTIOC9C#/MTCLKB#/TMRI4/CTS8#/ RTS8#/SS8#/SCK8/RSPCKA/IRQ7_DS/ AN216/ADTRG0#/COMP4
70	P64/AN204	P65/A12/IRQ9/AN211/CMPC53/DA1
71	AVCC2	P64/A13/IRQ8/AN210/CMPC33/DA0
72	VREF	AVCC2
73	AVSS2	AVSS2
74	P63/AN203/IRQ7	P63/A12/A14/IRQ7/AN209/CMPC23
75	P62/AN202/IRQ6	P62/A13/A15/IRQ6/AN208/CMPC43
76	P61/AN201/IRQ5	P61/A14/A16/IRQ5/AN207/CMPC13
77	P60/AN200/IRQ4	P60/A15/A17/IRQ4/AN206/CMPC03
78	P55/AN211/IRQ3	P55/A16/A18/IRQ3/AN203/CMPC32
79	P54/AN210/IRQ2	P54/A17/A19/IRQ2/AN202/CMPC22
80	P53/AN209/IRQ1	P53/A18/A20/IRQ1/AN201/CMPC12
81	P52/AN208/IRQ0	P52/IRQ0/AN200/CMPC02
82	P51/AN207	P47/AN103
83	P50/AN206	P46/AN102/CMPC50/CMPC51
84	P47/AN103	P45/AN101/CMPC40/CMPC41
85	P46/AN102/CMPC12/CMPC13/CMPC30/ CMPC31	P44/AN100/CMPC30/CMPC31
86	P45/AN101/CMPC02/CMPC03/CMPC20/ CMPC21	PH4/AN107/PGAVSS1
87	P44/AN100/CMPC10/CMPC11/CMPC32/ CMPC33	P43/AN003
88	P43/AN003	P42/AN002/CMPC20/CMPC21
89	P42/AN002	P41/AN001/CMPC10/CMPC11
90	P41/AN001	P40/AN000/CMPC00/CMPC01
91	P40/AN000/CMPC00/CMPC01/CMPC22/ CMPC23	PH0/AN007/PGAVSS0
92	AVCC1	AVCC1
93	AVCC0	AVCC0
94	AVSS0	AVSS0
95	AVSS1	AVSS1
96	P82/MTIC5U/TMO4/SCK6	P82/ALE/WAIT#/MTIC5U/MTIC5U#/ TMO4/SCK6/SCK12/IRQ3/COMP5
97	P81/MTIC5V/TMCI4/TXD6/SMOSI6/SSDA6	P81/CS2#/MTIC5V/MTIC5V#/TMCI4/ TXD6/SMOSI6/SSDA6/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/COMP4
98	P80/MTIC5W/TMRI4/RXD6/SMISO6/SSCL6	P80/CS1#/MTIC5W/MTIC5W#/TMRI4/ RXD6/SMISO6/SSCL6/RXD12/SMISO12/ SSCL12/RXDX12/IRQ5/COMP3
99	P11/MTIOC3A/MTCLKC/TMO3/IRQ1	P11/RD#/MTIOC3A/MTCLKC/ MTIOC3A#/MTCLKC#/MTIOC9D/ GTIOC3B/GTETRGA/GTIOC3B#/ GTETRGC/TMO3/POE9#/IRQ1_DS
100	P10/MTIOC9B/MTCLKD/TMRI3/POE12#/ CTS6#/RTS6#/SS6#/IRQ0	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/GTETRGB/GTETRGD/TMRI3/ POE12#/CTS6#/RTS6#/SS6#/IRQ0_DS

3.5 100-Pin Package (RX24T: Chip Version A, RX66T: With PGA Pseudo-Differential Input and Without USB Pins)

Table 3.5 lists Comparison of Pin Functions for 100-Pin Packages (RX24T: Chip Version A, RX66T: With PGA Pseudo-Differential Input and Without USB Pins).

Table 3.5 Comparison of Pin Functions for 100-Pin Packages (RX24T: Chip Version A, RX66T: With PGA Pseudo-Differential Input and Without USB Pins)

100 Pins	RX24T (Chip Version A)	RX66T (with PGA pseudo-differential input and without USB pins)
1	PE5/IRQ0	PE5/BCLK/MTIOC9D/MTIOC9D#/GTIOC3A/ GTETRGB/GTIOC3A#/GTETRGD/SCK9/ CTS9#/RTS9#/SS9#/IRQ0/ADST0
2	P02/MTIOC9D/CTS1#/RTS1#/SS1#/IRQ5/ ADST0	EMLE
3	VSS	VSS
4	P00/IRQ2/ADST1	UB/P00/A11/MTIOC9A/MTIOC9A#/CACREF/ RXD9/SMISO9/SSCL9/RXD12/SMISO12/ SSCL12/RXDX12/IRQ2/ADST1/COMP0
5	VCL	VCL
6	MD/FINED	MD/FINED
7	P01/POE12#/IRQ4/ADST2	P01/A10/MTIOC9C/MTIOC9C#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE12#/ TXD9/SMOSI9/SSDA9/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/IRQ4/ADST2/ COMP1
8	PE4/MTCLKC/POE10#/IRQ1	PE4/A9/MTCLKC/MTCLKC#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE10#/ SCK9/IRQ1
9	PE3/MTCLKD/POE11#/IRQ2	PE3/A8/MTCLKD/MTCLKD#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/POE11#/ CTS9#/RTS9#/SS9#/IRQ2_DS
10	RES#	RES#
11	XTAL/P37	XTAL/P37
12	VSS	VSS
13	EXTAL/P36	EXTAL/P36
14	VCC	VCC
15	PE2/POE10#/NMI	PE2/POE10#/NMI
16	PE1/MTIOC9D/TMO5/CTS5#/RTS5#/SS5#/ SSLA3	PE1/WR0#/WR#/MTIOC9D/MTIOC9D#/ TMO5/CTS5#/RTS5#/SS5#/CTS12#/ RTS12#/SS12#/SSLA3/IRQ15
17	PE0/MTIOC9B/TMCI1/TMCI5/SSLA2	PE0/WR1#/BC1#/WAIT#/MTIOC9B/ MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/ SSCL5/SSLA2/CRX0/IRQ7
18	PD7/MTIOC9A/TMRI1/TMRI5/SSLA1	TRST#/PD7/MTIOC9A/MTIOC9A#/ GTIOC0A/GTIOC3A/GTIOC0A#/ GTIOC3A#/TMRI1/TMRI5/TXD5/SMOSI5/ SSDA5/SSLA1/CTX0/IRQ8
19	PD6/MTIOC9C/TMO1/CTS1#/RTS1#/SS1#/ SSLA0/IRQ5/ADST0	TMS/PD6/MTIOC9C/MTIOC9C#/GTIOC0B/ GTIOC3B/GTIOC0B#/GTIOC3B#/TMO1/ CTS1#/RTS1#/SS1#/CTS11#/RTS11#/ SS11#/SSLA0/IRQ5/ADST0
20	PD5/TMRI0/TMRI6/RXD1/SMISO1/SSCL1/ IRQ3	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/ TMRI0/TMRI6/RXD1/SMISO1/SSCL1/ RXD11/SMISO11/SSCL11/IRQ6
21	PD4/TMCI0/TMCI6/SCK1/IRQ2	TCK/PD4/GTIOC1B/GTETRGB/ GTIOC1B#/TMCI0/TMCI6/SCK1/SCK11/IRQ2

100 Pins	RX24T (Chip Version A)	RX66T (with PGA pseudo-differential input and without USB pins)
22	PD3/TMO0/TXD1/SMOSI1/SSDA1	TDO/PD3/GTIOC2A/GTETRGC/GTIOC2A#/ TMO0/TXD1/SMOSI1/SSDA1/TXD11/ SMOSI11/SSDA11
23	PD2/TMCI1/TMO4/SCK5/MOSIA	TRCLK/PD2/A7/GTIOC2B/GTIOC0A/ GTIOC2B#/GTIOC0A#/TMCI1/TMO4/ SCK5/SCK8/MOSIA
24	PD1/TMO2/MISOA	TRDATA3/PD1/A6/GTIOC3A/GTIOC0B/ GTIOC3A#/GTIOC0B#/TMO2/RXD8/ SMISO8/SSCL8/MISOA
25	PD0/TMO6/RSPCKA	TRDATA2/PD0/A5/GTIOC3B/GTIOC1A/ GTIOC3B#/GTIOC1A#/TMO6/TXD8/ SMOSI8/SSDA8/RSPCKA
26	PB7/SCK5	TRDATA1/PB7/A4/GTIOC1B/GTIOC1B#/ SCK5/SCK11/SCK12
27	PB6/RXD5/SMISO5/SSCL5/IRQ5	TRDATA0/PB6/A3/GTIOC2A/GTIOC2A#/ RXD5/SMISO5/SSCL5/RXD11/SMISO11/ SSCL11/RXD12/SMISO12/SSCL12/ RXDX12/CRX0/IRQ2
28	PB5/TXD5/SMOSI5/SSDA5	TRSYNC/PB5/A2/GTIOC2B/GTIOC2B#/ TXD5/SMOSI5/SSDA5/TXD11/SMOSI11/ SSDA11/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/CTX0
29	VCC	VCC
30	PB4/POE8#/CTS5#/RTS5#/SS5#/IRQ3	PB4/A1/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE8#/CTS5#/RTS5#/SS5#/ SCK11/CTS11#/RTS11#/SS11#/IRQ3_DS
31	VSS	VSS
32	PB3/MTIOC0A/CACREF/SCK6/RSPCKA	PB3/A7(Note 1)/MTIOC0A/MTIOC0A#/CACREF/ SCK6/RSPCKA/IRQ9
33	PB2/MTIOC0B/TMRI0/ADSM0/TXD6/ SMOSI6/SSDA6/SDA0	PB2/A6(Note 1)/MTIOC0B/MTIOC0B#/GTADSM0/ TMRI0/TXD6/SMOSI6/SSDA6/SDA/ADSM0
34	PB1/MTIOC0C/TMCI0/ADSM1/RXD6/ SMISO6/SSCL6/SCL0	PB1/A5(Note 1)/MTIOC0C/MTIOC0C#/GTADSM1/ TMCI0/RXD6/SMISO6/SSCL6/SCL/IRQ4/ ADSM1
35	PB0/MTIOC0D/TMO0/TXD6/SMOSI6/ SSDA6/MOSIA/ADTRG2#	PB0/A0/A4(Note 1)/BC0#/MTIOC0D/MTIOC0D#/ TMO0/TXD6/SMOSI6/SSDA6/CTS11#/ RTS11#/SS11#/MOSIA/IRQ8/ADTRG2#
36	PA5/MTIOC1A/TMCI3/RXD6/SMISO6/ SSCL6/MISOA/IRQ1/ADTRG1#	PA5/A3(Note 1)/MTIOC1A/MTIOC1A#/TMCI3/ RXD6/SMISO6/SSCL6/RXD8/SMISO8/ SSCL8/MISOA/IRQ1/ADTRG1#
37	PA4/MTIOC1B/TMCI7/SCK6/RSPCKA/ ADTRG0#	PA4/A2(Note 1)/MTIOC1B/MTIOC1B#/TMCI7/ SCK6/TXD8/SMOSI8/SSDA8/RSPCKA/ ADTRG0#
38	PA3/MTIOC2A/TMRI7/SSLA0	PA3/A1(Note 1)/MTIOC2A/MTIOC2A#/GTADSM0/ TMRI7/TXD9/SMOSI9/SSDA9/SCK8/SSLA0
39	PA2/MTIOC2B/TMO7/CTS6#/RTS6#/SS6#/ SSLA1	PA2/A0/BC0#/MTIOC2B/MTIOC2B#/ GTADSM1/TMO7/CTS6#/RTS6#/SS6#/ RXD9/SMISO9/SSCL9/SCK11(Note 1)/SSLA1
40	PA1/MTIOC6A/TMO4/SSLA2/ADTRG0#	PA1/MTIOC6A/MTIOC6A#/TMO4/TXD9/ SMOSI9/SSDA9/RXD11/SMISO11/SSCL11/ SSLA2/CRX0/IRQ14_DS/ADTRG0#
41	PA0/MTIOC6C/TMO2/SSLA3	PA0/MTIOC6C/MTIOC6C#/TMO2/SCK9/ TXD11/SMOSI11/SSDA11/SSLA3/CTX0
42	VCC	VCC

100 Pins	RX24T (Chip Version A)	RX66T (with PGA pseudo-differential input and without USB pins)
43	P96/POE4#/IRQ4	P96/CS0#/WAIT#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE4#/CTS8#/ RTS8#/SS8#/IRQ4_DS
44	VSS	VSS
45	P95/MTIOC6B	P95/MTIOC6B/MTIOC6B#/GTIOC4A/ GTIOC7A/GTIOC4A#/GTIOC7A#
46	P94/MTIOC7A	P94/MTIOC7A/MTIOC7A#/GTIOC5A/ GTIOC8A/GTIOC5A#/GTIOC8A#
47	P93/MTIOC7B	P93/MTIOC7B/MTIOC7B#/GTIOC6A/ GTIOC9A/GTIOC6A#/GTIOC9A#
48	P92/MTIOC6D	P92/MTIOC6D/MTIOC6D#/GTIOC4B/ GTIOC7B/GTIOC4B#/GTIOC7B#
49	P91/MTIOC7C	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC8B/GTIOC5B#/GTIOC8B#
50	P90/MTIOC7D	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC9B/GTIOC6B#/GTIOC9B#
51	P76/MTIOC4D	P76/D0[A0/D0]/MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC6B/GTIOC2B#/GTIOC6B#
52	P75/MTIOC4C	P75/D1[A1/D1]/MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#
53	P74/MTIOC3D	P74/D2[A2/D2]/MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#
54	P73/MTIOC4B	P73/D3[A3/D3]/MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC6A/GTIOC2A#/GTIOC6A#
55	P72/MTIOC4A	P72/D4[A4/D4]/MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC5A/GTIOC1A#/GTIOC5A#
56	P71/MTIOC3B	P71/D5[A5/D5]/MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC4A/GTIOC0A#/GTIOC4A#
57	P70/POE0#/IRQ5	P70/D6[A6/D6]/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE0#/CTS9#/ RTS9#/SS9#/IRQ5_DS
58	P33/MTIOC3A/MTCLKA/TMO0/SSLA3	P33/D7[A7/D7]/MTIOC3A/MTCLKA/ MTIOC3A#/MTCLKA#/GTIOC3B/ GTIOC3B#/TMO0/SSLA3/IRQ13_DS
59	P32/MTIOC3C/MTCLKB/TMO6/SSLA2	P32/D8[A8/D8]/MTIOC3C/MTCLKB/ MTIOC3C#/MTCLKB#/GTIOC3A/ GTIOC3A#/TMO6/SSLA2/IRQ12_DS
60	VCC	VCC
61	P31/MTIOC0A/MTCLKC/TMRI6/SSLA1/ IRQ6	P31/D9[A9/D9]/MTIOC0A/MTCLKC/ MTIOC0A#/MTCLKC#/TMRI6/SSLA1/IRQ6
62	VSS	VSS
63	P30/MTIOC0B/MTCLKD/TMCI6/SSLA0/ IRQ7/COMP3	P30/D10[A10/D10]/MTIOC0B/MTCLKD/ MTIOC0B#/MTCLKD#/TMCI6/SCK8/ CTS8#/RTS8#/SS8#/SSLA0/IRQ7/COMP3
64	P24/MTIC5U/TMCI2/TMO6/RSPCKA/ COMP0	P27/CS3#(Note 1)/MTIOC1A/MTIOC0C/ MTIOC1A#/MTIOC0C#/POE9#/IRQ15
65	P23/MTIC5V/TMO2/CACREF/MOSIA/ COMP1	P24/D11[A11/D11]/MTIC5U/MTIC5U#/ TMCI2/TMO6/CTS8#/RTS8#/SS8#/SCK8/ RSPCKA/IRQ4/COMP0
66	P22/MTIC5W/TMRI2/TMO4/MISOA/ ADTRG2#/COMP2	P23/D12[A12/D12]/MTIC5V/MTIC5V#/ TMO2/CACREF/TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/SSDA12/TXDX12/ SIOX12/MOSIA/CTX0/IRQ11/COMP1

100 Pins	RX24T (Chip Version A)	RX66T (with PGA pseudo-differential input and without USB pins)
67	P21/MTCLKA/MTIOC9A/TMCI4/IRQ6/ ADTRG1#/AN116/CVREFC1	P22/D13[A13/D13]/MTIC5W/MTCLKD/ MTIC5W#/MTCLKD#/MTIOC9B/TMRI2/ TMO4/RXD8/SMISO8/SSCL8/RXD12/ SMISO12/SSCL12/RXDX12/MISOA/CRX0/ IRQ10/ADTRG2#/COMP2
68	P20/MTCLKB/MTIOC9C/TMRI4/IRQ7/ ADTRG0#/AN016/CVREFC0	P21/D14[A14/D14]/MTIOC9A/MTCLKA/ MTIOC9A#/MTCLKA#/TMCI4/TXD8/ SMOSI8/SSDA8/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/MOSIA/ IRQ6_DS/AN217/ADTRG1#/COMP5
69	P65/AN205	P20/D15[A15/D15]/MTIOC9C/MTCLKB/ MTIOC9C#/MTCLKB#/TMRI4/CTS8#/ RTS8#/SS8#/SCK8/RSPCKA/IRQ7_DS/ AN216/ADTRG0#/COMP4
70	P64/AN204	P65/A12/IRQ9/AN211/CMPC53/DA1
71	AVCC2	P64/A13/IRQ8/AN210/CMPC33/DA0
72	VREF	AVCC2
73	AVSS2	AVSS2
74	P63/AN203/IRQ7	P63/A12(Note 1)/A14/IRQ7/AN209/CMPC23
75	P62/AN202/IRQ6	P62/A13(Note 1)/A15/IRQ6/AN208/CMPC43
76	P61/AN201/IRQ5	P61/A14(Note 1)/A16/IRQ5/AN207/CMPC13
77	P60/AN200/IRQ4	P60/A15(Note 1)/A17/IRQ4/AN206/CMPC03
78	P55/AN211/IRQ3	P55/A16(Note 1)/A18/IRQ3/AN203/CMPC32
79	P54/AN210/IRQ2	P54/A17(Note 1)/A19/IRQ2/AN202/CMPC22
80	P53/AN209/IRQ1	P53/A18(Note 1)/A20/IRQ1/AN201/CMPC12
81	P52/AN208/IRQ0	P52/IRQ0/AN200/CMPC02
82	P51/AN207	P47/AN103
83	P50/AN206	P46/AN102/CMPC50/CMPC51
84	P47/AN103	P45/AN101/CMPC40/CMPC41
85	P46/AN102/CMPC12/CMPC13/CMPC30/ CMPC31	P44/AN100/CMPC30/CMPC31
86	P45/AN101/CMPC02/CMPC03/CMPC20/ CMPC21	PH4/AN107/PGAVSS1
87	P44/AN100/CMPC10/CMPC11/CMPC32/ CMPC33	P43/AN003
88	P43/AN003	P42/AN002/CMPC20/CMPC21
89	P42/AN002	P41/AN001/CMPC10/CMPC11
90	P41/AN001	P40/AN000/CMPC00/CMPC01
91	P40/AN000/CMPC00/CMPC01/CMPC22/ CMPC23	PH0/AN007/PGAVSS0
92	AVCC1	AVCC1
93	AVCC0	AVCC0
94	AVSS0	AVSS0
95	AVSS1	AVSS1
96	P82/MTIC5U/TMO4/SCK6	P82/ALE/WAIT#/MTIC5U/MTIC5U#/ TMO4/SCK6/SCK12/IRQ3/COMP5
97	P81/MTIC5V/TMCI4/TXD6/SMOSI6/SSDA6	P81/CS2#/MTIC5V/MTIC5V#/TMCI4/ TXD6/SMOSI6/SSDA6/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/COMP4
98	P80/MTIC5W/TMRI4/RXD6/SMISO6/SSCL6	P80/CS1#/MTIC5W/MTIC5W#/TMRI4/ RXD6/SMISO6/SSCL6/RXD12/SMISO12/ SSCL12/RXDX12/IRQ5/COMP3

100 Pins	RX24T (Chip Version A)	RX66T (with PGA pseudo-differential input and without USB pins)
99	P11/MTIOC3A/MTCLKC/TMO3/IRQ1	P11/RD#/MTIOC3A/MTCLKC/ MTIOC3A#/MTCLKC#/MTIOC9D/ GTIOC3B/GTETRGA/GTIOC3B#/ GTETRGC/TMO3/POE9#/IRQ1_DS
100	P10/MTIOC9B/MTCLKD/TMRI3/POE12#/ CTS6#/RTS6#/SS6#/IRQ0	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/GTETRGB/GTETRGD/TMRI3/ POE12#/CTS6#/RTS6#/SS6#/IRQ0_DS

Note 1. These pins are only enabled for products with 128 Kbytes of RAM.

3.6 100-Pin Package (RX24T: Chip Version A, RX66T: Without Both PGA Pseudo-Differential Input and USB Pins)

Table 3.6 lists Comparison of Pin Functions for 100-Pin Package (RX24T: Chip Version A, RX66T: Without Both PGA Pseudo-Differential Input and USB Pins).

Table 3.6 Comparison of Pin Functions for 100-Pin Package (RX24T: Chip Version A, RX66T: Without Both PGA Pseudo-Differential Input and USB Pins)

100 Pins	RX24T (Chip Version A)	RX66T (without both PGA pseudo-differential input and USB)
1	PE5/IRQ0	PE5/BCLK/MTIOC9D/MTIOC9D#/GTIOC3A/GTETRGB/GTIOC3A#/GTETRGD/SCK9/CTS9#/RTS9#/SS9#/IRQ0/ADST0
2	P02/MTIOC9D/CTS1#/RTS1#/SS1#/IRQ5/ADST0	EMLE
3	VSS	VSS
4	P00/IRQ2/ADST1	UB/P00/A11/MTIOC9A/MTIOC9A#/CACREF/RXD9/SMISO9/SSCL9/RXD12/SMISO12/SSCL12/RXDX12/IRQ2/ADST1/COMP0
5	VCL	VCL
6	MD/FINED	MD/FINED
7	P01/POE12#/IRQ4/ADST2	P01/A10/MTIOC9C/MTIOC9C#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE12#/TXD9/SMOSI9/SSDA9/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/IRQ4/ADST2/COMP1
8	PE4/MTCLKC/POE10#/IRQ1	PE4/A9/MTCLKC/MTCLKC#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE10#/SCK9/IRQ1
9	PE3/MTCLKD/POE11#/IRQ2	PE3/A8/MTCLKD/MTCLKD#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE11#/CTS9#/RTS9#/SS9#/IRQ2_DS
10	RES#	RES#
11	XTAL/P37	XTAL/P37
12	VSS	VSS
13	EXTAL/P36	EXTAL/P36
14	VCC	VCC
15	PE2/POE10#/NMI	PE2/POE10#/NMI
16	PE1/MTIOC9D/TMO5/CTS5#/RTS5#/SS5#/SSLA3	PE1/WR0#/WR#/MTIOC9D/MTIOC9D#/TMO5/CTS5#/RTS5#/SS5#/CTS12#/RTS12#/SS12#/SSLA3/IRQ15
17	PE0/MTIOC9B/TMCI1/TMCI5/SSLA2	PE0/WR1#/BC1#/WAIT#/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/SSCL5/SSLA2/CRX0/IRQ7
18	PD7/MTIOC9A/TMRI1/TMRI5/SSLA1	TRST#/PD7/MTIOC9A/MTIOC9A#/GTIOC0A/GTIOC3A/GTIOC0A#/GTIOC3A#/TMRI1/TMRI5/TXD5/SMOSI5/SSDA5/SSLA1/CTX0/IRQ8
19	PD6/MTIOC9C/TMO1/CTS1#/RTS1#/SS1#/SSLA0/IRQ5/ADST0	TMS/PD6/MTIOC9C/MTIOC9C#/GTIOC0B/GTIOC3B/GTIOC0B#/GTIOC3B#/TMO1/CTS1#/RTS1#/SS1#/CTS11#/RTS11#/SS11#/SSLA0/IRQ5/ADST0
20	PD5/TMRI0/TMRI6/RXD1/SMISO1/SSCL1/IRQ3	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/TMRI0/TMRI6/RXD1/SMISO1/SSCL1/RXD11/SMISO11/SSCL11/IRQ6

100 Pins	RX24T (Chip Version A)	RX66T (without both PGA pseudo-differential input and USB)
21	PD4/TMCI0/TMCI6/SCK1/IRQ2	TCK/PD4/GTIOC1B/GTETRGB/ GTIOC1B#/TMCI0/TMCI6/SCK1/SCK11/IRQ2
22	PD3/TMO0/TXD1/SMOSI1/SSDA1	TDO/PD3/GTIOC2A/GTETRGC/GTIOC2A#/ TMO0/TXD1/SMOSI1/SSDA1/TXD11/ SMOSI11/SSDA11
23	PD2/TMCI1/TMO4/SCK5/MOSIA	TRCLK/PD2/A7/GTIOC2B/GTIOC0A/ GTIOC2B#/GTIOC0A#/TMCI1/TMO4/ SCK5/SCK8/MOSIA
24	PD1/TMO2/MISOA	TRDATA3/PD1/A6/GTIOC3A/GTIOC0B/ GTIOC3A#/GTIOC0B#/TMO2/RXD8/ SMISO8/SSCL8/MISOA
25	PD0/TMO6/RSPCKA	TRDATA2/PD0/A5/GTIOC3B/GTIOC1A/ GTIOC3B#/GTIOC1A#/TMO6/TXD8/ SMOSI8/SSDA8/RSPCKA
26	PB7/SCK5	TRDATA1/PB7/A4/GTIOC1B/GTIOC1B#/ SCK5/SCK11/SCK12
27	PB6/RXD5/SMISO5/SSCL5/IRQ5	TRDATA0/PB6/A3/GTIOC2A/GTIOC2A#/ RXD5/SMISO5/SSCL5/RXD11/SMISO11/ SSCL11/RXD12/SMISO12/SSCL12/ RXDX12/CRX0/IRQ2
28	PB5/TXD5/SMOSI5/SSDA5	TRSYNC/PB5/A2/GTIOC2B/GTIOC2B#/ TXD5/SMOSI5/SSDA5/TXD11/SMOSI11/ SSDA11/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/CTX0
29	VCC	VCC
30	PB4/POE8#/CTS5#/RTS5#/SS5#/IRQ3	PB4/A1/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE8#/CTS5#/RTS5#/SS5#/ SCK11/CTS11#/RTS11#/SS11#/IRQ3_DS
31	VSS	VSS
32	PB3/MTIOC0A/CACREF/SCK6/RSPCKA	PB3/A7(Note 1)/MTIOC0A/MTIOC0A#/ CACREF/SCK6/RSPCKA/IRQ9
33	PB2/MTIOC0B/TMRI0/ADSM0/TXD6/ SMOSI6/SSDA6/SDA0	PB2/A6(Note 1)/MTIOC0B/MTIOC0B#/ GTADSM0/TMRI0/TXD6/SMOSI6/SSDA6/ SDA/ADSM0
34	PB1/MTIOC0C/TMCI0/ADSM1/RXD6/ SMISO6/SSCL6/SCL0	PB1/A5(Note 1)/MTIOC0C/MTIOC0C#/ GTADSM1/TMCI0/RXD6/SMISO6/SSCL6/ SCL/IRQ4/ADSM1
35	PB0/MTIOC0D/TMO0/TXD6/SMOSI6/ SSDA6/MOSIA/ADTRG2#	PB0/A0/A4(Note 1)/BC0#/MTIOC0D/MTIOC0D#/ TMO0/TXD6/SMOSI6/SSDA6/CTS11#/ RTS11#/SS11#/MOSIA/IRQ8/ADTRG2#
36	PA5/MTIOC1A/TMCI3/RXD6/SMISO6/ SSCL6/MISOA/IRQ1/ADTRG1#	PA5/A3(Note 1)/MTIOC1A/MTIOC1A#/TMCI3/ RXD6/SMISO6/SSCL6/RXD8/SMISO8/ SSCL8/MISOA/IRQ1/ADTRG1#
37	PA4/MTIOC1B/TMCI7/SCK6/RSPCKA/ ADTRG0#	PA4/A2(Note 1)/MTIOC1B/MTIOC1B#/TMCI7/ SCK6/TXD8/SMOSI8/SSDA8/RSPCKA/ ADTRG0#
38	PA3/MTIOC2A/TMRI7/SSLA0	PA3/A1(Note 1)/MTIOC2A/MTIOC2A#/ GTADSM0/TMRI7/TXD9/SMOSI9/SSDA9/ SCK8/SSLA0
39	PA2/MTIOC2B/TMO7/CTS6#/RTS6#/SS6#/ SSLA1	PA2/A0/BC0#/MTIOC2B/MTIOC2B#/ GTADSM1/TMO7/CTS6#/RTS6#/SS6#/ RXD9/SMISO9/SSCL9/SCK11(Note 1)/SSLA1

100 Pins	RX24T (Chip Version A)	RX66T (without both PGA pseudo-differential input and USB)
40	PA1/MTIOC6A/TMO4/SSLA2/ADTRG0#	PA1/MTIOC6A/MTIOC6A#/TMO4/TXD9/ SMOSI9/SSDA9/RXD11/SMISO11/SSCL11/ SSLA2/CRX0/IRQ14_DS/ADTRG0#
41	PA0/MTIOC6C/TMO2/SSLA3	PA0/MTIOC6C/MTIOC6C#/TMO2/SCK9/ TXD11/SMOSI11/SSDA11/SSLA3/CTX0
42	VCC	VCC
43	P96/POE4#/IRQ4	P96/CS0#/WAIT#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/ POE4#/CTS8#/RTS8#/SS8#/IRQ4_DS
44	VSS	VSS
45	P95/MTIOC6B	P95/MTIOC6B/MTIOC6B#/GTIOC4A/ GTIOC7A/GTIOC4A#/GTIOC7A#
46	P94/MTIOC7A	P94/MTIOC7A/MTIOC7A#/GTIOC5A/ GTIOC8A/GTIOC5A#/GTIOC8A#
47	P93/MTIOC7B	P93/MTIOC7B/MTIOC7B#/GTIOC6A/ GTIOC9A/GTIOC6A#/GTIOC9A#
48	P92/MTIOC6D	P92/MTIOC6D/MTIOC6D#/GTIOC4B/ GTIOC7B/GTIOC4B#/GTIOC7B#
49	P91/MTIOC7C	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC8B/GTIOC5B#/GTIOC8B#
50	P90/MTIOC7D	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC9B/GTIOC6B#/GTIOC9B#
51	P76/MTIOC4D	P76/D0[A0/D0]/MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC6B/GTIOC2B#/GTIOC6B#
52	P75/MTIOC4C	P75/D1[A1/D1]/MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#
53	P74/MTIOC3D	P74/D2[A2/D2]/MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#
54	P73/MTIOC4B	P73/D3[A3/D3]/MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC6A/GTIOC2A#/GTIOC6A#
55	P72/MTIOC4A	P72/D4[A4/D4]/MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC5A/GTIOC1A#/GTIOC5A#
56	P71/MTIOC3B	P71/D5[A5/D5]/MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC4A/GTIOC0A#/GTIOC4A#
57	P70/POE0#/IRQ5	P70/D6[A6/D6]/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE0#/CTS9#/ RTS9#/SS9#/IRQ5_DS
58	P33/MTIOC3A/MTCLKA/TMO0/SSLA3	P33/D7[A7/D7]/MTIOC3A/MTCLKA/ MTIOC3A#/MTCLKA#/GTIOC3B/ GTIOC3B#/TMO0/SSLA3/IRQ13_DS
59	P32/MTIOC3C/MTCLKB/TMO6/SSLA2	P32/D8[A8/D8]/MTIOC3C/MTCLKB/ MTIOC3C#/MTCLKB#/GTIOC3A/ GTIOC3A#/TMO6/SSLA2/IRQ12_DS
60	VCC	VCC
61	P31/MTIOC0A/MTCLKC/TMRI6/SSLA1/ IRQ6	P31/D9[A9/D9]/MTIOC0A/MTCLKC/ MTIOC0A#/MTCLKC#/TMRI6/SSLA1/IRQ6
62	VSS	VSS
63	P30/MTIOC0B/MTCLKD/TMCI6/SSLA0/ IRQ7/COMP3	P30/D10[A10/D10]/MTIOC0B/MTCLKD/ MTIOC0B#/MTCLKD#/TMCI6/SCK8/ CTS8#/RTS8#/SS8#/SSLA0/IRQ7/COMP3
64	P24/MTIC5U/TMCI2/TMO6/RSPCKA/ COMP0	P24/D11[A11/D11]/MTIC5U/MTIC5U#/ TMCI2/TMO6/CTS8#/RTS8#/SS8#/SCK8/ RSPCKA/IRQ4/COMP0

100 Pins	RX24T (Chip Version A)	RX66T (without both PGA pseudo-differential input and USB)
65	P23/MTIC5V/TMO2/CACREF/MOSIA/ COMP1	P23/D12[A12/D12]/MTIC5V/MTIC5V#/ TMO2/CACREF/TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/SSDA12/TXDX12/ SIOX12/MOSIA/CTX0/IRQ11/COMP1
66	P22/MTIC5W/TMRI2/TMO4/MISOA/ ADTRG2#/COMP2	P22/D13[A13/D13]/MTIC5W/MTCLKD/ MTIC5W#/MTCLKD#/MTIOC9B/TMRI2/ TMO4/RXD8/SMISO8/SSCL8/RXD12/ SMISO12/SSCL12/RXDX12/MISOA/CRX0/ IRQ10/ADTRG2#/COMP2
67	P21/MTCLKA/MTIOC9A/TMCI4/IRQ6/ ADTRG1#/AN116/CVREFC1	P21/D14[A14/D14]/MTIOC9A/MTCLKA/ MTIOC9A#/MTCLKA#/TMCI4/TXD8/ SMOSI8/SSDA8/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/MOSIA/ IRQ6_DS/AN217/ADTRG1#/COMP5
68	P20/MTCLKB/MTIOC9C/TMRI4/IRQ7/ ADTRG0#/AN016/CVREFC0	P20/D15[A15/D15]/MTIOC9C/MTCLKB/ MTIOC9C#/MTCLKB#/TMRI4/CTS8#/ RTS8#/SS8#/SCK8/RSPCKA/IRQ7_DS/ AN216/ADTRG0#/COMP4
69	P65/AN205	P65/A12/IRQ9/AN211/CMPC53/DA1
70	P64/AN204	P64/A13/IRQ8/AN210/CMPC33/DA0
71	AVCC2	AVCC2
72	VREF	AVCC2
73	AVSS2	AVSS2
74	P63/AN203/IRQ7	P63/A12(Note 1)/A14/IRQ7/AN209/CMPC23
75	P62/AN202/IRQ6	P62/A13(Note 1)/A15/IRQ6/AN208/CMPC43
76	P61/AN201/IRQ5	P61/A14(Note 1)/A16/IRQ5/AN207/CMPC13
77	P60/AN200/IRQ4	P60/A15(Note 1)/A17/IRQ4/AN206/CMPC03
78	P55/AN211/IRQ3	P55/A16(Note 1)/A18/IRQ3/AN203/CMPC32
79	P54/AN210/IRQ2	P54/A17(Note 1)/A19/IRQ2/AN202/CMPC22
80	P53/AN209/IRQ1	P53/A18(Note 1)/A20/IRQ1/AN201/CMPC12
81	P52/AN208/IRQ0	P52/IRQ0/AN200/CMPC02
82	P51/AN207	P51/AN205/CMPC52
83	P50/AN206	P50/AN204/CMPC42
84	P47/AN103	P47/AN103
85	P46/AN102/CMPC12/CMPC13/CMPC30/ CMPC31	P46/AN102/CMPC50/CMPC51
86	P45/AN101/CMPC02/CMPC03/CMPC20/ CMPC21	P45/AN101/CMPC40/CMPC41
87	P44/AN100/CMPC10/CMPC11/CMPC32/ CMPC33	P44/AN100/CMPC30/CMPC31
88	P43/AN003	P43/AN003
89	P42/AN002	P42/AN002/CMPC20/CMPC21
90	P41/AN001	P41/AN001/CMPC10/CMPC11
91	P40/AN000/CMPC00/CMPC01/CMPC22/ CMPC23	P40/AN000/CMPC00/CMPC01
92	AVCC1	AVCC1
93	AVCC0	AVCC0
94	AVSS0	AVSS0
95	AVSS1	AVSS1
96	P82/MTIC5U/TMO4/SCK6	P82/ALE/WAIT#/MTIC5U/MTIC5U#/ TMO4/SCK6/SCK12/IRQ3/COMP5

100 Pins	RX24T (Chip Version A)	RX66T (without both PGA pseudo-differential input and USB)
97	P81/MTIC5V/TMCI4/TXD6/SMOSI6/SSDA6	P81/CS2#/MTIC5V/MTIC5V#/TMCI4/ TXD6/SMOSI6/SSDA6/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/COMP4
98	P80/MTIC5W/TMRI4/RXD6/SMISO6/SSCL6	P80/CS1#/MTIC5W/MTIC5W#/TMRI4/ RXD6/SMISO6/SSCL6/RXD12/SMISO12/ SSCL12/RXDX12/IRQ5/COMP3
99	P11/MTIOC3A/MTCLKC/TMO3/IRQ1	P11/RD#/MTIOC3A/MTCLKC/ MTIOC3A#/MTCLKC#/MTIOC9D/ GTIOC3B/GTETRGA/GTIOC3B#/ GTETRGC/TMO3/POE9#/IRQ1_DS
100	P10/MTIOC9B/MTCLKD/TMRI3/POE12#/ CTS6#/RTS6#/SS6#/IRQ0	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/GTETRGB/GTETRGD/TMRI3/ POE12#/CTS6#/RTS6#/SS6#/IRQ0_DS

Note 1. These pins are only enabled for products with 128 Kbytes of RAM.

3.7 80-Pin Package

Table 3.7 lists Comparison of Pin Functions for 80-Pin Package.

Table 3.7 Comparison of Pin Functions for 80-Pin Package

80Pins	RX24T	RX66T (with PGA pseudo-differential input and without USB pins)
1	P02/MTIOC9D/CTS1#/RTS1#/SS1#/IRQ5/ADST0	EMLE
2	VSS	VSS
3	P00/IRQ2/ADST1	UB/P00/MTIOC9A/MTIOC9A#/CACREF/RXD9/SMISO9/SSCL9/RXD12/SMISO12/SSCL12/RXDX12/IRQ2/ADST1/COMP0
4	VCL	VCL
5	MD/FINED	MD/FINED
6	P01/POE12#/IRQ4/ADST2	P01/MTIOC9C/MTIOC9C#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE12#/TXD9/SMOSI9/SSDA9/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/IRQ4/ADST2/COMP1
7	PE4/MTCLKC/POE10#/IRQ1	PE4/MTCLKC/MTCLKC#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE10#/SCK9/IRQ1
8	PE3/MTCLKD/POE11#/IRQ2	PE3/MTCLKD/MTCLKD#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE11#/CTS9#/RTS9#/SS9#/IRQ2_DS
9	RES#	RES#
10	XTAL/P37	XTAL/P37
11	VSS	VSS
12	EXTAL/P36	EXTAL/P36
13	VCC	VCC
14	PE2/POE10#/NMI	PE2/POE10#/NMI
15	PD7/MTIOC9A/TMRI1/TMRI5/SSLA1	TRST#/PD7/MTIOC9A/MTIOC9A#/GTIOC0A/GTIOC3A/GTIOC0A#/GTIOC3A#/TMRI1/TMRI5/TXD5/SMOSI5/SSDA5/SSLA1/CTX0/IRQ8
16	PD6/MTIOC9C/TMO1/CTS1#/RTS1#/SS1#/SSLA0/IRQ5/ADST0	TMS/PD6/MTIOC9C/MTIOC9C#/GTIOC0B/GTIOC3B/GTIOC0B#/GTIOC3B#/TMO1/CTS1#/RTS1#/SS1#/CTS11#/RTS11#/SS11#/SSLA0/IRQ5/ADST0
17	PD5/TMRI0/TMRI6/RXD1/SMISO1/SSCL1/IRQ3	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/TMRI0/TMRI6/RXD1/SMISO1/SSCL1/RXD11/SMISO11/SSCL11/IRQ6
18	PD4/TMCI0/TMCI6/SCK1/IRQ2	TCK/PD4/GTIOC1B/GTETRGB/GTIOC1B#/TMCI0/TMCI6/SCK1/SCK11/IRQ2
19	PD3/TMO0/TXD1/SMOSI1/SSDA1	TDO/PD3/GTIOC2A/GTETRGC/GTIOC2A#/TMO0/TXD1/SMOSI1/SSDA1/TXD11/SMOSI11/SSDA11
20	PD2/TMCI1/TMO4/SCK5/MOSIA	PD2/GTIOC2B/GTIOC0A/GTIOC2B#/GTIOC0A#/TMCI1/TMO4/SCK5/SCK8/MOSIA
21	PB6/RXD5/SMISO5/SSCL5/IRQ5	PB6/GTIOC2A/GTIOC2A#/RXD5/SMISO5/SSCL5/RXD11/SMISO11/SSCL11/RXD12/SMISO12/SSCL12/RXDX12/CRX0/IRQ2
22	PB5/TXD5/SMOSI5/SSDA5	PB5/GTIOC2B/GTIOC2B#/TXD5/SMOSI5/SSDA5/TXD11/SMOSI11/SSDA11/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/CTX0
23	VCC	VCC

80Pins	RX24T	RX66T (with PGA pseudo-differential input and without USB pins)
24	PB4/POE8#/CTS5#/RTS5#/SS5#/IRQ3	PB4/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE8#/CTS5#/RTS5#/SS5#/SCK11/CTS11#/RTS11#/SS11#/IRQ3_DS
25	VSS	VSS
26	PB3/MTIOC0A/CACREF/SCK6/RSPCKA	PB3/MTIOC0A/MTIOC0A#/CACREF/SCK6/RSPCKA/IRQ9
27	PB2/MTIOC0B/TMRI0/ADSM0/TXD6/SMOSI6/SSDA6/SDA0	PB2/MTIOC0B/MTIOC0B#/GTADSM0/TMRI0/TXD6/SMOSI6/SSDA6/SDA/ADSM0
28	PB1/MTIOC0C/TMCI0/ADSM1/RXD6/SMISO6/SSCL6/SCL0	PB1/MTIOC0C/MTIOC0C#/GTADSM1/TMCI0/RXD6/SMISO6/SSCL6/SCL/IRQ4/ADSM1
29	PB0/MTIOC0D/TMO0/TXD6/SMOSI6/SSDA6/MOSIA/ADTRG2#	PB0/MTIOC0D/MTIOC0D#/TMO0/TXD6/SMOSI6/SSDA6/CTS11#/RTS11#/SS11#/MOSIA/IRQ8/ADTRG2#
30	PA5/MTIOC1A/TMCI3/RXD6/SMISO6/SSCL6/MISOA/IRQ1/ADTRG1#	PA5/MTIOC1A/MTIOC1A#/TMCI3/RXD6/SMISO6/SSCL6/RXD8/SMISO8/SSCL8/MISOA/IRQ1/ADTRG1#
31	PA3/MTIOC2A/TMRI7/SSLA0	PA3/MTIOC2A/MTIOC2A#/GTADSM0/TMRI7/TXD9/SMOSI9/SSDA9/SCK8/SSLA0
32	VCC	VCC
33	P96/POE4#/IRQ4	P96/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE4#/CTS8#/RTS8#/SS8#/IRQ4_DS
34	VSS	VSS
35	P95/MTIOC6B	P95/MTIOC6B/MTIOC6B#/GTIOC4A/GTIOC7A/GTIOC4A#/GTIOC7A#
36	P94/MTIOC7A	P94/MTIOC7A/MTIOC7A#/GTIOC5A/GTIOC8A/GTIOC5A#/GTIOC8A#
37	P93/MTIOC7B	P93/MTIOC7B/MTIOC7B#/GTIOC6A/GTIOC9A/GTIOC6A#/GTIOC9A#
38	P92/MTIOC6D	P92/MTIOC6D/MTIOC6D#/GTIOC4B/GTIOC7B/GTIOC4B#/GTIOC7B#
39	P91/MTIOC7C	P91/MTIOC7C/MTIOC7C#/GTIOC5B/GTIOC8B/GTIOC5B#/GTIOC8B#
40	P90/MTIOC7D	P90/MTIOC7D/MTIOC7D#/GTIOC6B/GTIOC9B/GTIOC6B#/GTIOC9B#
41	P76/MTIOC4D	P76/MTIOC4D/MTIOC4D#/GTIOC2B/GTIOC6B/GTIOC2B#/GTIOC6B#
42	P75/MTIOC4C	P75/MTIOC4C/MTIOC4C#/GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#
43	P74/MTIOC3D	P74/MTIOC3D/MTIOC3D#/GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#
44	P73/MTIOC4B	P73/MTIOC4B/MTIOC4B#/GTIOC2A/GTIOC6A/GTIOC2A#/GTIOC6A#
45	P72/MTIOC4A	P72/MTIOC4A/MTIOC4A#/GTIOC1A/GTIOC5A/GTIOC1A#/GTIOC5A#
46	P71/MTIOC3B	P71/MTIOC3B/MTIOC3B#/GTIOC0A/GTIOC4A/GTIOC0A#/GTIOC4A#
47	P70/POE0#/IRQ5	P70/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE0#/CTS9#/RTS9#/SS9#/IRQ5_DS
48	VCC	VCC
49	P31/MTIOC0A/MTCLKC/TMRI6/SSLA1/IRQ6	P31/MTIOC0A/MTCLKC/MTIOC0A#/MTCLKC#/TMRI6/SSLA1/IRQ6
50	VSS	VSS

80Pins	RX24T	RX66T (with PGA pseudo-differential input and without USB pins)
51	P30/MTIOC0B/MTCLKD/TMCI6/SSLA0/ IRQ7/COMP3	P30/MTIOC0B/MTCLKD/MTIOC0B#/ MTCLKD#/TMCI6/SCK8/CTS8#/RTS8#/ SS8#/SSLA0/IRQ7/COMP3
52	P24/MTIC5U/TMCI2/TMO6/RSPCKA/ COMP0	P27/MTIOC1A/MTIOC0C/MTIOC1A#/ MTIOC0C#/POE9#/IRQ15
53	P23/MTIC5V/TMO2/CACREF/MOSIA/ COMP1	P22/MTIC5W/MTCLKD/MTIC5W#/MTCLKD#/ MTIOC9B/TMRI2/TMO4/RXD8/SMISO8/ SSCL8/RXD12/SMISO12/SSCL12/RXDX12/ MISOA/CRX0/IRQ10/ADTRG2#/COMP2
54	P22/MTIC5W/TMRI2/TMO4/MISOA/ ADTRG2#/COMP2	P21/MTIOC9A/MTCLKA/MTIOC9A#/ MTCLKA#/TMCI4/TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ MOSIA/IRQ6_DS/AN217/ADTRG1#/COMP5
55	P21/MTCLKA/MTIOC9A/TMCI4/IRQ6/ ADTRG1#/AN116/CVREFC1	P20/MTIOC9C/MTCLKB/MTIOC9C#/ MTCLKB#/TMRI4/CTS8#/RTS8#/SS8#/ SCK8/RSPCKA/IRQ7_DS/AN216/ ADTRG0#/COMP4
56	P20/MTCLKB/MTIOC9C/TMRI4/IRQ7/ ADTRG0#/AN016/CVREFC0	P65/IRQ9/AN211/CMPC53/DA1
57	AVCC2	P64/IRQ8/AN210/CMPC33/DA0
58	VREF	AVCC2
59	AVSS2	AVSS2
60	P62/AN202/IRQ6	P62/IRQ6/AN208/CMPC43
61	P55/AN211/IRQ3	P55/IRQ3/AN203/CMPC32
62	P54/AN210/IRQ2	P54/IRQ2/AN202/CMPC22
63	P53/AN209/IRQ1	P53/IRQ1/AN201/CMPC12
64	P52/AN208/IRQ0	P52/IRQ0/AN200/CMPC02
65	P51/AN207	P47/AN103
66	P50/AN206	P46/AN102/CMPC50/CMPC51
67	P47/AN103	P45/AN101/CMPC40/CMPC41
68	P46/AN102/CMPC12/CMPC13/CMPC30/ CMPC31	P44/AN100/CMPC30/CMPC31
69	P45/AN101/CMPC02/CMPC03/CMPC20/ CMPC21	PH4/AN107/PGAVSS1
70	P44/AN100/CMPC10/CMPC11/CMPC32/ CMPC33	P43/AN003
71	P43/AN003	P42/AN002/CMPC20/CMPC21
72	P42/AN002	P41/AN001/CMPC10/CMPC11
73	P41/AN001	P40/AN000/CMPC00/CMPC01
74	P40/AN000/CMPC00/CMPC01/CMPC22/ CMPC23	PH0/AN007/PGAVSS0
75	AVCC1	AVCC1
76	AVCC0	AVCC0
77	AVSS0	AVSS0
78	AVSS1	AVSS1
79	P11/MTIOC3A/MTCLKC/TMO3/IRQ1	P11/MTIOC3A/MTCLKC/MTIOC3A#/ MTCLKC#/MTIOC9D/GTIOC3B/GTETRGA/ GTIOC3B#/GTETRGC/TMO3/POE9#/ IRQ1_DS
80	P10/MTIOC9B/MTCLKD/TMRI3/POE12#/ CTS6#/RTS6#/SS6#/IRQ0	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/GTETRGB/GTETRGD/TMRI3/ POE12#/CTS6#/RTS6#/SS6#/IRQ0_DS

3.8 64-Pin Package

Table 3.8 lists Comparison of Pin Functions for 64-Pin Package.

Table 3.8 Comparison of Pin Functions for 64-Pin Package

64Pins	RX24T	RX66T (with PGA pseudo-differential input and without USB pins)
1	P02/MTIOC9D/CTS1#/RTS1#/SS1#/IRQ5/ ADST0	EMLE
2	P00/IRQ2/ADST1	UB/P00/MTIOC9A/MTIOC9A#/CACREF/ RXD9/SMISO9/SSCL9/RXD12/SMISO12/ SSCL12/RXDX12/IRQ2/ADST1/COMP0
3	VCL	VCL
4	MD/FINED	MD/FINED
5	P01/POE12#/IRQ4/ADST2	P01/MTIOC9C/MTIOC9C#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/ POE12#/TXD9/SMOSI9/SSDA9/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ IRQ4/ADST2/COMP1
6	RES#	RES#
7	XTAL/P37	XTAL/P37
8	VSS	VSS
9	EXTAL/P36	EXTAL/P36
10	VCC	VCC
11	PE2/POE10#/NMI	PE2/POE10#/NMI
12	PD7/MTIOC9A/TMRI1/TMRI5/SSLA1	TRST#/PD7/MTIOC9A/MTIOC9A#/ GTIOC0A/GTIOC3A/GTIOC0A#/ GTIOC3A#/TMRI1/TMRI5/TXD5/ SMOSI5/SSDA5/SSLA1/CTX0/IRQ8
13	PD6/MTIOC9C/TMO1/CTS1#/RTS1#/SS1#	TMS/PD6/MTIOC9C/MTIOC9C#/GTIOC0B/ GTIOC3B/GTIOC0B#/GTIOC3B#/TMO1/ CTS1#/RTS1#/SS1#/CTS11#/RTS11#/ SS11#/SSLA0/IRQ5/ADST0
14	PD5/TMRI0/TMRI6/RXD1/SMISO1/SSCL1	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/ TMRI0/TMRI6/RXD1/SMISO1/SSCL1/ RXD11/SMISO11/SSCL11/IRQ6
15	PD4/TMCI0/TMCI6/SCK1/IRQ2	TCK/PD4/GTIOC1B/GTETRGB/ GTIOC1B#/TMCI0/TMCI6/SCK1/SCK11/IRQ2
16	PD3/TMO0/TXD1/SMOSI1/SSDA1	TDO/PD3/GTIOC2A/GTETRGC/ GTIOC2A#/TMO0/TXD1/SMOSI1/ SSDA1/TXD11/SMOSI11/SSDA11
17	PB6/RXD5/SMISO5/SSCL5/IRQ5	PB6/GTIOC2A/GTIOC2A#/RXD5/SMISO5/ SSCL5/RXD11/SMISO11/SSCL11/RXD12/ SMISO12/SSCL12/RXDX12/CRX0/IRQ2
18	PB5/TXD5/SMOSI5/SSDA5	PB5/GTIOC2B/GTIOC2B#/TXD5/SMOSI5/ SSDA5/TXD11/SMOSI11/SSDA11/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/CTX0
19	PB4/POE8#/CTS5#/RTS5#/SS5#/IRQ3	PB4/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE8#/CTS5#/RTS5#/SS5#/ SCK11/CTS11#/RTS11#/SS11#/IRQ3_DS
20	PB3/MTIOC0A/CACREF/SCK6/RSPCKA	PB3/MTIOC0A/MTIOC0A#/CACREF/SCK6/ RSPCKA/IRQ9
21	PB2/MTIOC0B/TMRI0/ADSM0/TXD6/ SMOSI6/SSDA6/SDA0	PB2/MTIOC0B/MTIOC0B#/GTADSM0/ TMRI0/TXD6/SMOSI6/SSDA6/SDA/ADSM0
22	PB1/MTIOC0C/TMCI0/ADSM1/RXD6/ SMISO6/SSCL6/SCL0	PB1/MTIOC0C/MTIOC0C#/GTADSM1/ TMCI0/RXD6/SMISO6/SSCL6/SCL/ IRQ4/ADSM1

64Pins	RX24T	RX66T (with PGA pseudo-differential input and without USB pins)
23	VCC	PB0/MTIOC0D/MTIOC0D#/TMO0/TXD6/ SMOSI6/SSDA6/CTS11#/RTS11#/SS11#/ MOSIA/IRQ8/ADTRG2#
24	P96/POE4#/IRQ4	VCC
25	VSS	P96/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE4#/CTS8#/RTS8#/ SS8#/IRQ4_DS
26	P95/MTIOC6B	VSS
27	P94/MTIOC7A	P95/MTIOC6B/MTIOC6B#/GTIOC4A/ GTIOC7A/GTIOC4A#/GTIOC7A#
28	P93/MTIOC7B	P94/MTIOC7A/MTIOC7A#/GTIOC5A/ GTIOC8A/GTIOC5A#/GTIOC8A#
29	P92/MTIOC6D	P93/MTIOC7B/MTIOC7B#/GTIOC6A/ GTIOC9A/GTIOC6A#/GTIOC9A#
30	P91/MTIOC7C	P92/MTIOC6D/MTIOC6D#/GTIOC4B/ GTIOC7B/GTIOC4B#/GTIOC7B#
31	P90/MTIOC7D	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC8B/GTIOC5B#/GTIOC8B#
32	P76/MTIOC4D	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC9B/GTIOC6B#/GTIOC9B#
33	P75/MTIOC4C	P76/MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC6B/GTIOC2B#/GTIOC6B#
34	P74/MTIOC3D	P75/MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC5B/GTIOC1B#/GTIOC5B#
35	P73/MTIOC4B	P74/MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC4B/GTIOC0B#/GTIOC4B#
36	P72/MTIOC4A	P73/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC6A/GTIOC2A#/GTIOC6A#
37	P71/MTIOC3B	P72/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC5A/GTIOC1A#/GTIOC5A#
38	P70/POE0#/IRQ5	P71/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC4A/GTIOC0A#/GTIOC4A#
39	VCC	P70/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE0#/CTS9#/RTS9#/ SS9#/IRQ5_DS
40	P31/MTIOC0A/MTCLKC/TMRI6/SSLA1/IRQ6	VCC
41	VSS	VSS
42	P30/MTIOC0B/MTCLKD/TMCI6/SSLA0/ IRQ7/COMP3	P22/MTIC5W/MTCLKD/MTIC5W#/ MTCLKD#/MTIOC9B/TMRI2/TMO4/ RXD8/SMISO8/SSCL8/RXD12/SMISO12/ SSCL12/RXDX12/MISOA/CRX0/IRQ10/ ADTRG2#/COMP2
43	P24/MTIC5U/TMCI2/TMO6/RSPCKA/ COMP0	P21/MTIOC9A/MTCLKA/MTIOC9A#/ MTCLKA#/TMCI4/TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ MOSIA/IRQ6_DS/AN217/ADTRG1#/COMP5
44	P23/MTIC5V/TMO2/CACREF/MOSIA/ COMP1	P20/MTIOC9C/MTCLKB/MTIOC9C#/ MTCLKB#/TMRI4/CTS8#/RTS8#/SS8#/ SCK8/RSPCKA/IRQ7_DS/AN216/ ADTRG0#/COMP4
45	P22/MTIC5W/TMRI2/TMO4/MISOA/ ADTRG2#/COMP2	P65/IRQ9/AN211/CMPC53/DA1
46	P21/MTCLKA/MTIOC9A/TMCI4/IRQ6/ ADTRG1#/AN116/CVREFC1	P64/IRQ8/AN210/CMPC33/DA0
47	AVCC2/VREF	AVCC2

64Pins	RX24T	RX66T (with PGA pseudo-differential input and without USB pins)
48	AVSS2	AVSS2
49	P54/AN210/IRQ2	P54/IRQ2/AN202/CMPC22
50	P53/AN209/IRQ1	P53/IRQ1/AN201/CMPC12
51	P52/AN208/IRQ0	P52/IRQ0/AN200/CMPC02
52	P51/AN207	P46/AN102/CMPC50/CMPC51
53	P50/AN206	P45/AN101/CMPC40/CMPC41
54	P46/AN102/CMPC12/CMPC13/CMPC30/ CMPC31	P44/AN100/CMPC30/CMPC31
55	P45/AN101/CMPC02/CMPC03/CMPC20/ CMPC21	PH4/AN107/PGAVSS1
56	P44/AN100/CMPC10/CMPC11/CMPC32/ CMPC33	P42/AN002/CMPC20/CMPC21
57	P42/AN002	P41/AN001/CMPC10/CMPC11
58	P41/AN001	P40/AN000/CMPC00/CMPC01
59	P40/AN000/CMPC00/CMPC01/CMPC22/ CMPC23	PH0/AN007/PGAVSS0
60	AVCC1	AVCC1
61	AVCC0	AVCC0
62	AVSS0	AVSS0
63	AVSS1	AVSS1
64	P11/MTIOC3A/MTCLKC/TMO3/IRQ1	P11/MTIOC3A/MTCLKC/MTIOC3A#/ MTCLKC#/MTIOC9D/GTIOC3B/ GTETRGA/GTIOC3B#/GTETRGC/ TMO3/POE9#/IRQ1_DS

4. Important Information when Replacing the MCU

This section provides the important information regarding differences between the RX66T Group and the RX24T Group. 4.1 Notes on Pin Design describes notes regarding the hardware and 4.2 Notes on Functional Design describes notes regarding the software.

4.1 Notes on Pin Design

Migration between the RX24T Group (100 pins: Chip Version B) and the RX66T Group (100 pins: without both PGA pseudo-differential input and USB) can easily be achieved since they are pin to pin compatible except some pins. Please note that some pins need to be handled differently between Groups. Refer to 3.3 100-Pin Package (RX24T: Chip Version B, RX66T: Without Both PGA Pseudo-Differential Input and USB Pins) for details.

4.1.1 VCL Pin (External Capacity)

When using a smoothing capacitor connected to the VCL pin for stabilizing internal power supply, use 4.7 μF on the RX24T Groups, and 0.47 μF on the RX66T Group.

4.1.2 Pins for Setting Modes

On the RX24T Group the mode-setting pin on release from the reset state is MD, but on the RX66T Group there are two mode-setting pins: MD and UB (function-multiplexed with P00).

4.1.3 General I/O Ports

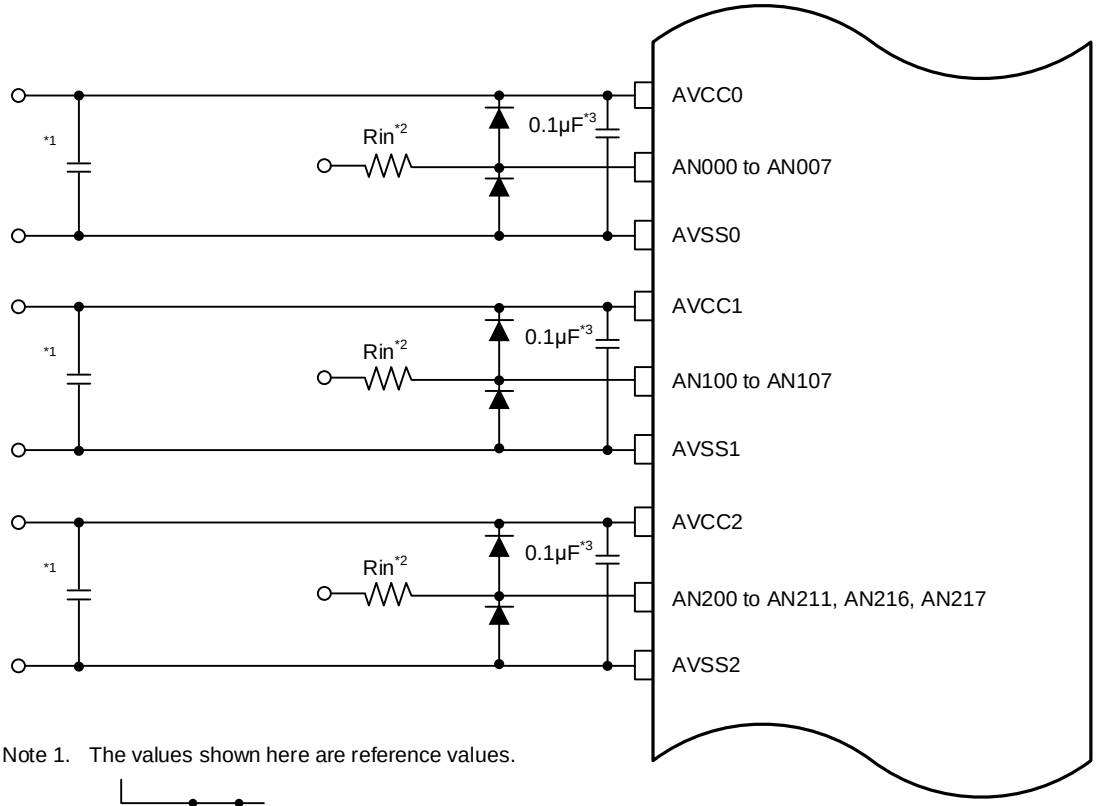
Ports 4 to 6 on the RX24T Groups, and ports 4 to 6 and H (other than PH0 or PH4) on the RX66T Group are I/O ports dependent on AVCC. Thus these ports need to be handled carefully. When not using these ports, set them to input, and connect them to AVCC via resistor for each pin (pull-up) or connect them to AVSS via resistor for each pin (pull-down). Otherwise, set these pins to output and release them.
When these ports are set to output and released, power supply current might be increased after a reset is released. This is because these pins are set to input immediately after a reset is released and the voltage level for the pins are unstable while the pins are set to input.

4.1.4 PGA Pseudo-Differential Input–Related Pins (P40 to P42, P44 to P46, PH0, and PH4)

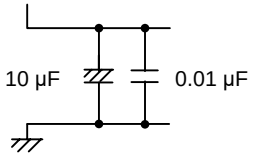
On the RX66T Group a negative voltage may be input on the PGA pseudo-differential input pins from the reset state. Therefore, regardless of whether or not the PGA is used, it is necessary to change the settings of the PGA-related registers in order to use the pin functions of P40 to P42, P44 to P46, PH0, and PH4 after release from the reset state. For details, refer to the descriptions of the VOLSR.PGAVLS bit, the initial setting sequence of the A/D converter, and the PIDR register in RX66T Group: User's Manual: Hardware.
Note that the above-mentioned setting changes are necessary even on products not equipped with PGA pseudo-differential input.

4.1.5 Inserting Decoupling Capacitors between AVCC and AVSS Pins

To prevent destruction of the analog input pins (AN000 to AN007, AN100 to AN107, AN200 to AN211, AN216, and AN217) by abnormal voltage such as an excessive surge, insert capacitors between AVCCn and AVSSn as shown in the figure below, and connect a protective circuit to protect the analog input pins (AN000 to AN007, AN100 to AN107, AN200 to AN211, AN216, and AN217).



Note 1. The values shown here are reference values.



Note 2. Rin: Signal source impedance

Note 3. Place the capacitors to be placed between the power supply pins AVCC0 and AVSS0, AVCC1 and AVSS1, and AVCC2 and AVSS2 as close to the pins as possible to improve the precision of A/D conversion.
When using the A/D converter with a higher operating frequency than 40 MHz, take the following steps to satisfy the electrical characteristics requirements.
(1) Add a 1000-pF capacitor to the 0.1-μF capacitor.
(2) Place the 1000-pF capacitor closer to the MCU than the 0.1-μF capacitor.
(3) Place the capacitor on the AVCC1 side closer to the MCU than that on the AVCC0 side.

4.2 Notes on Functional Design

Software operating on the RX24T Groups are compatible with some software on the RX66T Group. However, careful evaluation is required since specifications such as operating timing and electrical characteristics are different between the Groups.
This section describes notes on software regarding settings of functions that are different between the RX66T Group and the RX24T Groups.
For differences in modules and functions, refer to 2.Comparison of Specifications Overview. For further information, refer to the User's Manual: Hardware listed in 5.Reference Documents.

4.2.1 RIIC Operating Voltage Setting

When using the RIIC on the RX66T Group, it is necessary to specify the power supply voltage range in order to maintain the proper slope characteristics.
The initial setting is VCC = 4.5 V or greater. If a power supply voltage lower than 4.5 V will be used, change the voltage range setting before starting RIIC operation.
For details, refer to the description of the VOLSR.RICVLS bit in RX66T Group: User's Manual: Hardware.

4.2.2 USB Operating Voltage Setting

When using the USB on the RX66T Group, it is necessary to set the UBS power supply control bit to 1 before starting USB operation.
For details, refer to the description of the VOLSR.USBVON bit in RX66T Group: User's Manual: Hardware.

4.2.3 Voltage Level Setting

On the RX66T Group, values for the voltage level setting register (VOLSR) of operating modes, voltage detection level select register (LVDLVLR) of the voltage detection circuit, and option function select register 1 (OFS1) of the option-setting memory need to be changed to appropriate values depending on the operating voltage. Make sure to set these values by a program.

4.2.4 Option-Setting Memory

ID code protection and ID code protection of the on-chip debugger are located in the ROM on the RX24T Groups, and in the option-setting memory on the RX66T Group. Note that setting procedures are different between the Groups.

4.2.5 Clock Frequency Setting

On the RX24T Groups, the restrictions on setting clock frequency is ICLK ≥ PCLK.
On the RX66T Group, set as follows:

Restrictions on setting clock frequency: ICLK ≥ BCLK, PCLKC ≥ PCLKA ≥ PCLKB
Restrictions on clock frequency ratio: (N: integer)
ICLK:FCLK = N:1 or 1:N;
ICLK:PCLKA = N:1 or 1:N;
ICLK:PCLKB = N:1 or 1:N;
ICLK:PCLKC = N:1 or 1:N;
ICLK:PCLKD = N:1 or 1:N;
PCLKA:PCLKC = 1:1 or 1:2,
PCLKB:PCLKD = 1:1, 2:1, 4:1, 1:2

Also, on the RX66T Group, when setting the frequency of ICLK to faster than 120 MHz, the value of the MEMWAIT register needs to be changed.

4.2.6 Main Clock Oscillator

On the RX24T Group the main clock starts oscillating after a reset is released, but on the RX66T Group the LOCO clock is used for operation after a reset is released, so oscillation by the main clock must be started by a program.

4.2.7 PLL Circuit

On the RX24T Group the multiplication factor setting range of the PLL circuit is 4× to 15.5× (in 0.5× increments), but on the RX66T Group it is 10× to 30× (in 0.5× increments). Change the setting to an appropriate value when using the PLL circuit. Also, on the RX66T Group use a program to switch the PLL clock.

4.2.8 All-Module Clock Stop Mode

The RX24T Group does not have an all-module clock stop mode.
On the RX66T Group, when transition is made to all-module clock stop mode, 1 must be written to MSTPA24, MSTPA27, MSTPA29, and MSTPD0 to MSTPD7.

4.2.9 Software Configurable Interrupt

On the RX24T Group the interrupt sources have fixed vector numbers, but on the RX66T Group the MTU and GPTW interrupt sources are classified as selectable interrupt A and set in selectable interrupt A source select register n (SLIARn), allowing interrupt sources to be allocated to 208 to 255 in the interrupt vector table.

4.2.10 Operating Frequencies of the GPTW and MTU3d

On the RX66T Group, the count clock for the GPTW and MTU3d is PCLKC while the bus clock is PCLKA. Note that restrictions may apply depending on a combination of frequencies used.

4.2.11 DMAC Trigger by the MTU

On the RX66T group, if a DMA transfer is initiated by the MTU, the trigger signal is cleared when the DMAC requests ownership of the internal bus. Accordingly, the state of the internal bus may lead to a wait for the start of DMA transfer.

4.2.12 Port Output Enable

Registers for the port output enable on the RX66T Group are quite different from those on the RX24T Groups. Note that compatibility is low in this function.

4.2.13 General PWM Timer

Registers for the general PWM timer on the RX66T Group are quite different from those on the RX24T Groups. Note that compatibility is low in this function.

4.2.14 CAN Module

Registers for the CAN Module on the RX66T Group are quite different from those on the RX24T Groups. Note that compatibility is low in this function.

4.2.15 12-Bit A/D Converter

Registers for the 12-bit A/D converter on the RX66T Group are quite different from those on the RX24T Groups. Note that compatibility is low in this function.

4.2.16 ROM Cache

The RX66T Group has an 8 KB ROM cache, and ROM cache operation is disabled after a reset is released.
To use the ROM cache, set the ROMCE.ROMCEN bit to 1.

4.2.17 Using Commands in the Flash Memory

On the RX24T Group it is possible to program and erase the flash memory by issuing software commands after putting the sequencer into the dedicated mode for ROM programming and erasing. On the RX66T Group, programming and erasing the flash memory are performed by controlling the FCU with the FACI commands specified in the FACI command issuing area.
Table 4.1 lists Comparison of Specifications Between Software and FACI Commands.

Table 4.1 Comparison of Specifications Between Software and FACI Commands

Item	Software Command (RX24T)	FACI Command (RX66T)
Available command	• Program • Block erase • All-block erase • Blank check • Start-up area information program • Access window information program	• Programming • Block erase • P/E suspend • P/E resume • Status clear • Forced stop • Lock-bit read • Blank check • Configuration setting • Lock-bit programming

5. Reference Documents

User's Manual: Hardware

RX24T Group User's Manual: Hardware Rev.2.00 (R01UH0576)
(The latest version can be downloaded from the Renesas Electronics website.)

RX66T Group User's Manual: Hardware Rev.1.00 (R01UH0749)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News
(The latest version can be downloaded from the Renesas Electronics website.)

Related Technical Updates

This module reflects the content of the following technical updates.

- TN-RX*-A173A/E
- TN-RX*-A175A/E
- TN-RX*-A190A/E
- TN-RX*-A193A/E
- TN-RX*-A194A/E
- TN-RX*-A200A/E

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Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Sep. 20, 2018	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   ¾ The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   ¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   ¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   ¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   ¾ The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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